Optimal IMC-based control design of a 3-phase buck Power Factor Correction converter

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***Abstract*—The Swiss Rectifier exploits double-loop control to regulate output voltage and inductor current. To simplify and speed up the control design, proportional-integral regulators are commonly used, but they do not achieve optimal regulation, especially under dynamic conditions or when the converter plant is affected by delays and uncertainties. We propose an optimal control design based on the Internal Model Control (IMC) theory, able to reduce the impact of plant inaccuracies and fulfill static and dynamic specifications. The plant model is accurately obtained through PLECS simulations, including system delays, and it is used to design the controllers. The simulations show the superiority of the proposed control, that was also implemented on a microcontroller and tested on an 8-kW PFC converter prototype.**

***Index Terms*—Power factor correction, Internal model control, Swiss rectifier**

I. Introduction

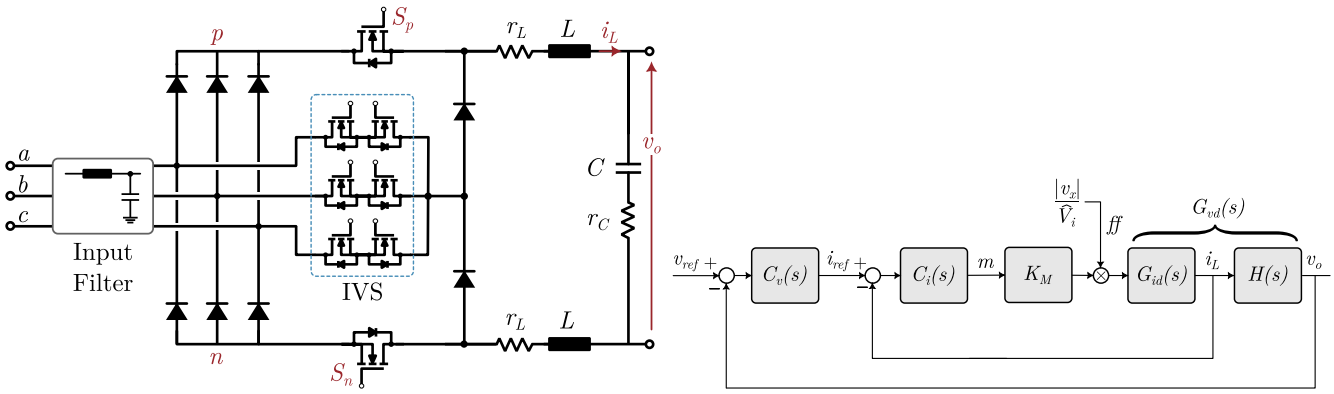
Power Factor Correction (PFC) is necessary when interfacing electronic systems to the electrical grid to reduce the reactive power on the power lines and improve the quality of the current in terms of Total Harmonic Distortion (THD). While single-phase PFC converters find space in low-power applications, three-phase PFC converters are commonly adopted in fast chargers for electric vehicles, energy storage systems and power supply systems for data centers, that require higher power levels [1]–[3].

Among three-phase converters, the "Swiss" PFC Rectifier can be employed when the required bus voltage is lower than the rectified 3-phase voltage. This enables the use of lower voltage rating power devices, enabling the achievement of high efficiency and high power density, even due to the use of Silicon Carbide (SiC) technology [1], [4]. The Swiss Rectifier topology is based on a buck configuration, allowing for a DC output voltage regulation, while actively controlling the input current to ensure a high PFC. Its operation relies on pulse-width modulation (PWM) applied to the buck switches to shape the input currents sinusoidally and in phase with their respective grid voltages. As the main drawback, it is a hard-switched topology characterized by a complex control, requiring two nested feedback loops for the output voltage and the inductor current, and a feed-forward action for shaping the input current. Moreover, due to the discontinuous input current, the presence of a large EMI filter is mandatory to reduce emissions injected into the grid [5].

Other topologies have been investigated in the literature to introduce soft-switching capability in the PFC converter, adopting phase-shifted full-bridge [6] and a mid-point clamped full-bridge [7], providing also galvanic isolation between input and output.

Regarding the control, the voltage and current controllers are usually PI or PID regulators, that are often tuned iteratively and empirically, also due to the uncertainty in determining the converter plant model. The use of PID regulators can lead to deteriorated performances of the converter, since the optimal parameters of a PID controller are specific to a given operating point and a particular set of system parameters (e.g. inductances, capacitances). Variations in these parameters (due to temperature, aging, etc.) or the presence of noise in measurements can compromise PID performance, necessitating further tuning procedures or the adoption of complex control strategies [8], [9]. To overcome these limitations, advanced control logics such as model predictive control (MPC), adaptive control, sliding mode control, or artificial intelligence-based approaches(e.g., neural networks, fuzzy logic) have been proposed [10], [11]. These methodologies offer the potential for improved robustness, faster dynamic response, and more effective management of non-linearities and operational constraints, despite a much more complex implementation.

In this article, we propose a simulation-aided procedure to optimally design the control of the 3-phase buck-PFC converter and fulfill static and dynamic requirements also in the presence of uncertainty in the converter plant due to parameter variation or delays. After determining the control-to-output transfer function through PLECS simulations, we designed an optimal controller using the theory of Internal



(a) (b)

Fig. 1: Schematic of the 3-phase buck PFC "Swiss" converter (a) and its control system (b).

Model Control (IMC) [12], allowing to largely absorb the aforementioned uncertainties. We provide the analytical design of the controllers and verify the results in simulation. Finally, the digital control was implemented into a microcontroller for the experimental verification on a 8 kW prototype.

II. IMC-BASED CONTROL DESIGN

Fig. 1(a) shows the schematic of the 3-phase buck PFC "Swiss" converter, whose main sections are *(a)* the input filter, *(b)* the diode rectifier, *(c)* the Input Voltage Selector (IVS) and *(d)* the buck converter. The general control diagram is shown in Fig. 1(b) and it consists of an inner loop to regulate the inductor current i_L and an outer loop that regulates the output voltage v_o. $C_v(s)$ and $C_i(s)$ are generic voltage and current controllers for the two feedback loops, respectively, expressed in the Laplace domain, with $s \in \mathbb{C}$. The coefficient $K_M = 2/(3\hat{V}_i)$ is a constant dependent on the amplitude of the input phase voltage $\hat{V}_i$, whereas v_x is the voltage providing the feedforward action (*ff*) to the modulating signals of switches S_p and S_n, and it is equal to the voltage at node p of the rectifier for driving S_p and the voltage at node n for driving S_n. Finally, $G_{id}(s)$ is the control-to-i_L transfer function representing the plant for the inner loop, $H(s)$ is the i_L-to-v_o transfer function, determined analytically in (1) considering a resistive load R, $\tau_z = r_C C$, $\tau_p = (r_C + R)C$. Finally, $G_{vd}(s) = G_{id}(s)H(s)$ is the control-to-v_o transfer function. The transducers are considered ideal in first approximation and are not represented in Fig. 1(b). Their impact will be discussed in Section III.

$$H(s) = \frac{v_o(s)}{i_L(s)} = \frac{R(1 + r_C C s)}{1 + (r_C + R)Cs} = \frac{H_0(1 + \tau_z s)}{1 + \tau_p s} \quad (1)$$

The plant $G_{vd}(s)$ is representative of the converter operation and in general its determination is made very challenging: although it can be determined analytically through state-space-averaging, the uncertainty in the components, as well as delays and high-order effects cannot be easily included. Here, a highly accurate simulation model of the converter is realized using PLECS, so that an estimation $\tilde{G}_{vd}(s)$ of the plant transfer function can be obtained from the small-signal analysis. This analysis was conducted exploiting the "multi-tone analysis" tool provided by PLECS simulator, consisting of applying a single signal composed of multiple sinusoidal signals at different frequencies to the system and analyzing its response. Compared to classical AC sweep, the multitone analysis can be more efficient because instead of sweeping through frequencies one at a time, the response to a multitone signal contains all the frequencies of interest simultaneously.

TABLE I: Specifications of the PFC converter under study.

Input voltage (3-ph)	400 V, 50 Hz
Output voltage	300 V
Maximum power	8 kW
Switching frequency	45 kHz
Output filter	$L = 253$ μH, $r_L = 0.1$ Ω
	$C = 560$ μF, $r_C = 0.01$ Ω
Input filter	$L_f = 375$ μH, $r_{L_f} = 2.15$ Ω
	$C_f = 6.8$ μF
Power devices	Rectifier: GC50MPS12
	IVS and Buck: G3R12MT12K

The simulated converter is designed based on [4] and replicates with high-fidelity an existing experimental prototype realized previously. SiC MOSFETs and diodes are employed in the converter and their manufacturer's models are used in the simulation. The main specifications of the PFC converter are summarized in Table I.

The design of the controllers is conducted without considering the feedforward action, that is independent on the output quantities v_o and i_L, and starting from the inner current loop to progressively simplify the block diagram of Fig. 1(b). The Bode diagram of $G_{vd}(s)$ was obtained from the PLECS small-signal analysis by operating the converter in open-loop at maximum load, using a fixed value of the control variable m, to which is added the small-signal perturbation.

The obtained Bode diagram of $G_{vd}(s)$ is reported in Fig. 2 and is used to determine the analytical transfer function $\tilde{G}_{vd}(s)$ that better approximates the response. This is a generic two-poles transfer function with resonance angular frequency $\omega_r = 2\pi \cdot 250$ rad/s, damping factor $\zeta = 0.167$ and dc-gain

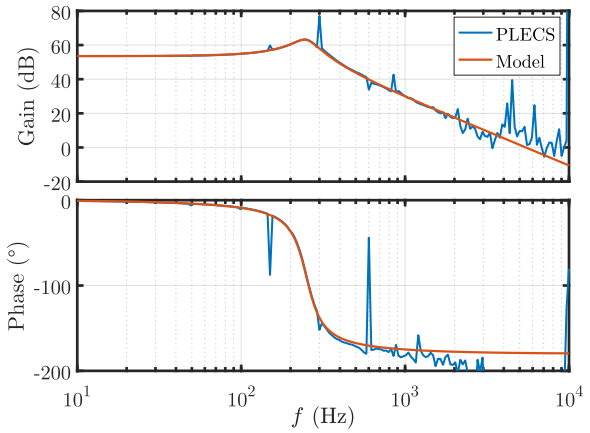


Fig. 2: Comparison of Bode diagrams of $G_{vd}(s)$ at maximum load obtained from PLECS and from the analytical model expressed by (2).

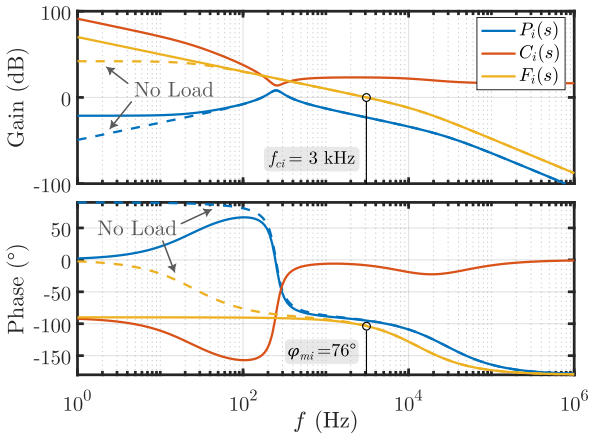


Fig. 3: Bode diagrams of $\tilde{P}_i(s)$, $C_i(s)$ and the open-loop transfer function $F_i(s)$ of the inner loop at maximum load and no load.

$G_0 = 475$ V, as defined in (2). As can be noted in Fig. 2, the analytical model (2) describes accurately the control-to-v_o frequency response of the converter up to 3 kHz, where an increase in the effect of noise begins to appear.

$$\tilde{G}_{vd}(s) = \frac{G_0\omega_r^2}{s^2 + 2\zeta\omega_r s + \omega_r^2} \tag{2}$$

Hence, considering that $\tilde{G}_{id}(s) = \tilde{G}_{vd}(s)/H(s)$, an estimation of the plant transfer function for the inner loop can be obtained as in (3).

$$\tilde{P}_i(s) = \frac{i_L(s)}{m(s)} = \frac{K_M\tilde{G}_{vd}(s)}{H(s)} \tag{3}$$

Therefore $\tilde{P}_i(s)$ is an estimation of the real controlled process, it has $n_z = 1$ zeros and $n_p = 3$ poles, and it is a system with minimal phase, i.e. it has no time delays or right-half plane zeros.

According to the theory of Internal Model Control (IMC) [12], [13], the perfect controller is given by $C_{imc}(s) = \tilde{P}_i(s)^{-1}\Gamma(s)$, where $\Gamma(s)$ is a corrective term that makes $C_{imc}(s)$ a causal system ($n_p \geq n_z$). In this case the IMC can be used to determine the equivalent controller $C_i(s)$ that minimizes the effect of the real plant $P_i(s)$ on the controlled variable, achieving optimal performances. It is given by (4).

$$C_i(s) = \frac{C_{imc}(s)}{1 - C_{imc}(s)\tilde{P}_i(s)} \tag{4}$$

Since $\tilde{P}_i(s)$ has a relative grade $n_p - n_z = 2$, the corrective term $\Gamma(s)$ must have the form defined in (5), where $\tau_i = 25$ μs is chosen to have two identical high-frequency real poles.

$$\Gamma(s) = \frac{1}{(1 + \tau_i s)^2} \tag{5}$$

The selection of τ_i directly impacts the performance of the controller. In fact, assuming a perfect estimation of the plant $\tilde{P}_i(s) = P_i(s)$, the final expression for $C_i(s)$ would be equal to (6).

$$C_i(s) = \frac{1}{\tau_i s(\tau_i s + 2)}\frac{1}{\tilde{P}_i(s)} \tag{6}$$

The Bode diagrams of $\tilde{P}_i(s)$, $C_i(s)$ and the open-loop transfer function of the current loop $F_i(s) = C_i(s)\tilde{P}_i(s)$ are shown in Fig. 3, where it is evident how the control perfectly "cancels" the estimated plant. This effect cannot be obtained when using standard controllers as PID regulators. Equation (6) and Fig. 3 also highlight that the controller automatically establishes a pole in zero in the open-loop transfer function when the load is present, ensuring the perfect tracking of the setpoint. At no load, this effect is lost and further analysis on the stability and steady-state error must be conducted to achieve regulation.

For this specific design, a crossing frequency $f_{ci} = 3$ kHz was selected, with a phase-margin $\varphi_{mi} = 76°$. Therefore, the closed-loop transfer function of the inner loop, defined in (7), is asymptotically stable, with a control bandwidth $f_{bw,i} = 4.1$ kHz.

$$W_i(s) = \frac{i_L(s)}{i_{ref}(s)} = \frac{F_i(s)}{1 + F_i(s)} \tag{7}$$

Therefore, the inner current loop can be represented through its closed-loop transfer function $W_i(s)$, and the plant of the voltage loop can be defined as $P_v(s) = W_i(s)H(s)$. However, since the voltage regulator must work at a frequency lower than $f_{bw,i}$, it is reasonable to consider $W_i(s) \approx 1$, because $F_i(s) \gg 1$. So, the plant of the voltage loop can be adequately approximated with $H(s)$, simplifying the design of $C_v(s)$. Using the IMC approach as before, the obtained regulator is expressed by (8).

$$C_v(s) = \left(K_p + \frac{K_i}{s}\right)\frac{1}{\tau_v s + 1} \tag{8}$$

It is equivalent to a PI regulator with $K_p = \tau_p/(H_0\tau_v)$ and $K_i = 1/(H_0\tau_v)$, followed by a cascaded low-pass filter. The

time-constant τ_v was chosen in order to have a pole at a frequency lower than $f_{bw,i}$, and in this design $\tau_v = 500$ μs.

In this way, the closed-loop transfer function of the whole system results asymptotically stable, with a phase-margin $\varphi_{mv} = 83°$ and a bandwidth $f_{bw,v} = 330$ Hz.

III. Effect of System Delays and Uncertainties

The controllers designed in the previous section can be adopted even if the estimation of the plant is not perfectly representative of the actual one, i.e. if $\tilde{P}_i(s) \neq P_i(s)$. If so, and this is the case in real applications, the IMC-based controller can still provide benefits in the regulation.

Suppose that the actual plant $P_i(s)$ contains delays, e.g. due to the current and voltage transducers and to the digital microcontroller, and also uncertainty in the exact value of some parameters, such as the output inductor L or the capacitor C. It is possible to write the actual plant as $P_i(s) = \tilde{P}_i(s)P_x(s)$, where $P_x(s)$ represents the non-estimated contribution of the actual system. Under this condition, (6) can still be applied to design $C_i(s)$, but the open-loop and closed-loop transfer functions are now expressed by (9) and (10), respectively, and contain the contributions of the non-estimated part of the plant.

$$F_i(s) = C_i(s)\tilde{P}_i(s)P_x(s) = \frac{P_x(s)}{\tau_i s(\tau_i s + 2)} \tag{9}$$

$$W_i(s) = \frac{P_x(s)}{P_x(s) + \tau_i s(\tau_i s + 2)} \tag{10}$$

To provide a numeric example of the impact of non-perfect estimation of the plant, we performed a PLECS simulation adding a delay T_d in the control system and considering a -10% variation of the output capacitor C. It was chosen $T_d = 50$ μs in order to include the delay caused by the actuation of the digital control, usually equal to $1/f_s$, and the delay caused by the transducers.

The variation of the output capacitor affects both $G_{vd}(s)$, by changing ω_r, and $H(s)$. Assuming in general the variation of the capacitor as $C' = (1+k)C$, with $k = -0.1$ in the case under study, the variation in the resonance angular frequency can be expressed as $\omega_r' = \omega_r/\sqrt{1+k}$. The actual plant can be written as in (11), where $G_{vd}'(s)$ and $H'(s)$ are computed using C'.

$$P_i(s) = \frac{K_M G_{vd}'(s) e^{-sT_d}}{H'(s)} \tag{11}$$

Assuming that the same estimation $\tilde{P}_i(s)$ as defined in (3) is adopted to design $C_i(s)$, the bode diagram of the actual plant, the estimated one and the open-loop transfer function are shown in Fig. 4. The error in estimating the actual plant mainly causes two effects: the non perfect cancellation between the controller and the plant and a reduction of the phase margin due to the presence of delay. However, the open-loop transfer function is still made stable using the IMC-based controller $C_i(s)$, with a phase-margin of about 32° and a gain-margin of 1.35.

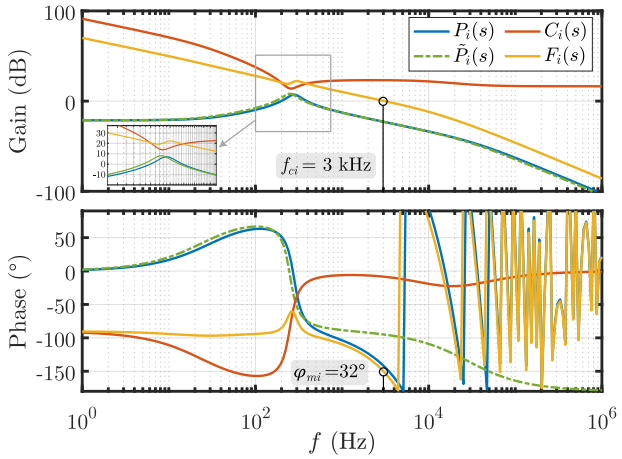


Fig. 4: Bode diagrams of the controller $C_i(s)$, designed in presence of non-estimated delay and parameter variation in the actual plant $P_i(s)$, and the open-loop transfer function $F_i(s)$ of the inner loop at maximum load. The estimated plant $\tilde{P}_i(s)$ is also reported for comparison.

IV. Simulation Results

PLECS simulations were performed to compare the performances of the designed controllers with standard PI regulators and to verify the behavior of the PFC converter under dynamic load variations. In the simulation environment, the voltage and current controllers were discretized using the Backward Euler method, considering a discretization step $T_z = 1/(2f_s)$ so that the control action is applied twice during the switching period of the buck switches S_p and S_n. This choice has also a beneficial impact in the actual implementation of the control algortihm, as it allows to reduce the delay between the computation and the actuation of the new duty-cycle value for each control cycle. Basically, this choice halves the delay caused by the digital controller in the system.

The reference output voltage was set to 300 V, and a saturation action was also set for both controllers to limit i_{ref} between $[0 - 40]$ A and the duty-cycle between $[0 - 1]$. The simulation results for a load variation from half power (4 kW) to full power (8 kW) are shown in Fig. 5, comparing the waveforms of v_o and i_L obtained using the proposed control and those obtained using discrete PI control. The parameters of the PI controllers were chosen to have similar characteristics in terms of bandwidth and phase margin to the proposed control.

From Fig. 5(a), it is evident how the PI control is unable to compensate the sudden load variation and v_o deviates from the setpoint, maintaining an error of about 50 V. Instead, the proposed control achieves optimal regulation of v_o, with a settlement time of about 5 ms and maximum error of 10 V during the transient. Considering Fig. 5(b), when using the PI controllers i_L shows undershoot after the soft-start at about 0.01 s and ringing at 0.06 s, causing larger EMI. With the proposed IMC-based controllers i_L shows smooth transitions after the soft-start and the load variation. For completeness, Fig. 5(c) and (d) show the phase voltages and current, respec-

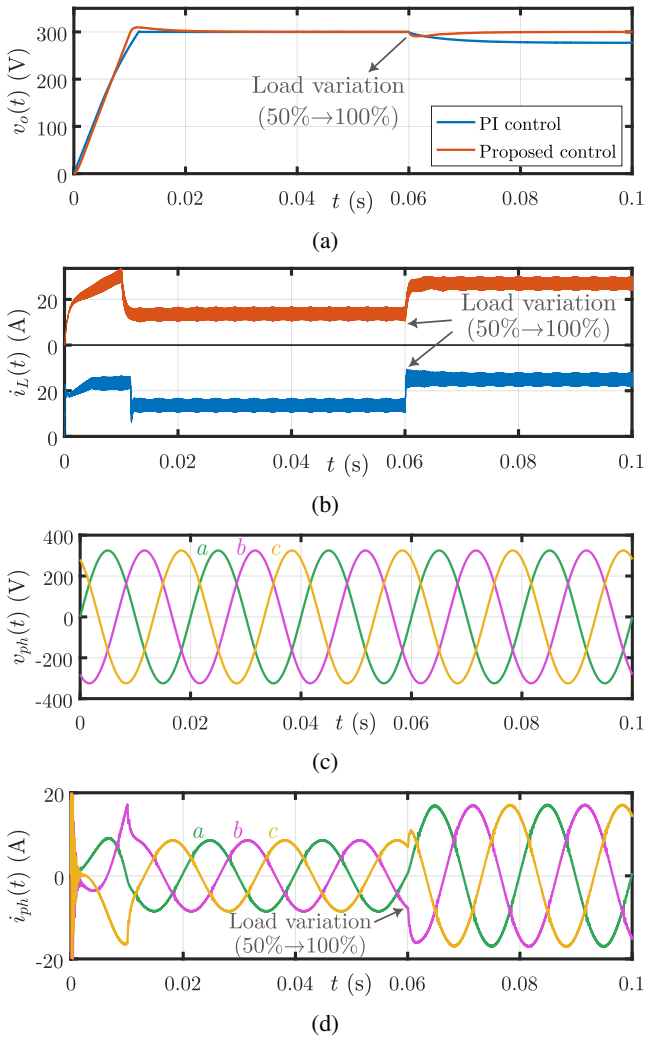


Fig. 5: Results of PLECS simulations during the startup of the converter and for a load variation from 50% to 100% of the rated power, adopting the proposed controllers and standard PI regulators: (a) output voltage; (b) inductor current; (c) phase voltages; (d) phase currents.

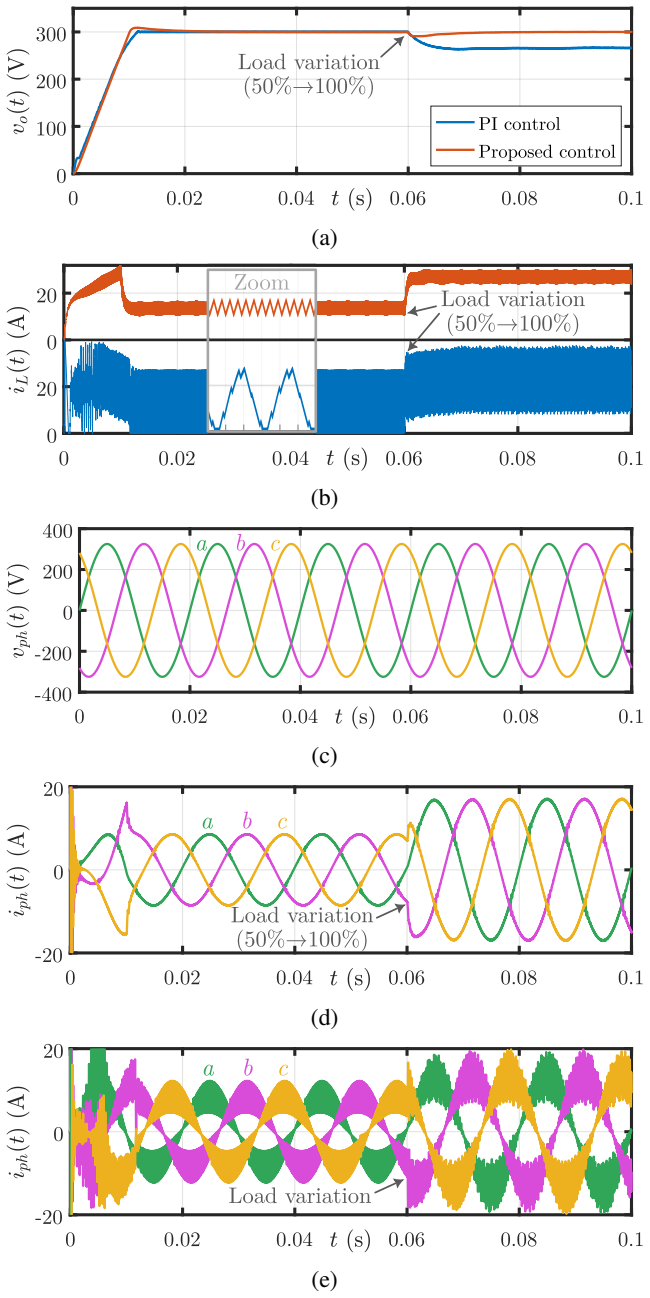


Fig. 6: Results of PLECS simulations in the presence of a delay $T_d = 20$ μs in the control system and with a -10% variation of the output capacitance, for a load variation from 50% to 100% of the rated power: (a) output voltage; (b) inductor current; (c) phase voltages; (d) phase currents with proposed control; (e) phase currents with standard PI control.

tively. However, the phase currents do not exhibit significant differences when using PI regulators or the proposed controller under this operating conditions.

A second series of simulations was conducted to verify the robustness of the control with respect to the uncertainty of converter parameters and system delays. As in Section III, a 10% reduction of the output capacitance was considered. This is also a realistic scenario which may occur due to aging and degradation of the capacitor [14]. The presence of delays was simulated considering the effect of transducers and analog-to-digital conversion, introducing a transport delay on the feedback quantities (v_o, i_L, phase voltages) in PLECS. The delay in the actuation of the duty-cycle, typical of MCU-based control, was included delaying by one control cycle the application of the new computed value. The total delay in simulation was 20 μs, considering $T_z = 1/(2f_s) \approx 11$ μs.

The simulation results under the described conditions are reported in Fig. 6. From Fig. 6(b), it must be noted that the PI control causes the instability of the inductor current, that shows an oscillation frequency of 7.5 kHz. This has also an impact on the phase currents (Fig. 6(e)), that are affected by the same oscillations and cause higher EMI emissions injected into the grid. The output voltage shows a steady-state error of

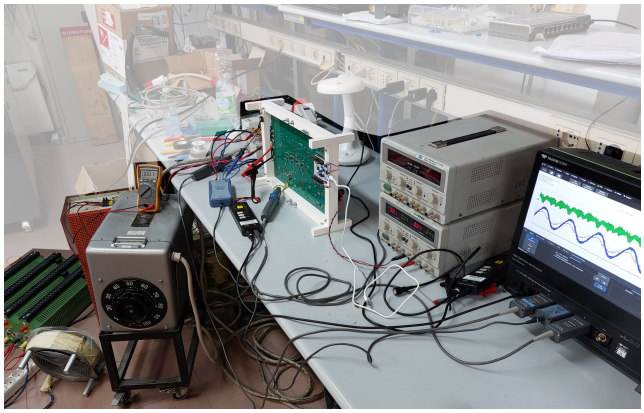


Fig. 7: Picture of the experimental setup.

about 50 V using the PI control when a 50% to 100% load variation happens. If the IMC-based controller is adopted, the converter operation is not affected by neither the presence of the delay nor the output capacitance variation. In fact, as noted in Fig. 6(a) and (b), the output voltage is regulated to the setpoint of 300 V and recovers from the load variation in about 4 ms, the inductor current is stable and only contains the expected switching ripple. The phase currents, visible in Fig. 6(d), show unitary power factor and reduced ripple, as expected from the normal operation of the PFC converter.

V. Experimental validation

The control logic was implemented into a STM32G474 microcontroller (MCU) to verify the performances of the proposed control. A picture of the experimental setup is shown in Fig. 7. The tests were conducted under two load conditions, namely 1.5 kW and 3.0 kW, and using both PI regulators and the proposed controllers for voltage and current loops.

The ADC peripheral of the MCU was used in direct memory access mode to speed up the conversion. The sampling instants were synchronized with the PWM timer to happen when the counter is equal to zero and to the maximum counter value, dependent on the PWM switching frequency. Under this condition, the ADC is triggered twice during the PWM period, replicating the scenario described in IV. Therefore, the control action is computed with a fixed period $T_z = 1/(2f_s)$. The IVS is driven by another PWM peripheral, that senses the zero-crossing of phase voltage a and establishes the control signals for all switches of the IVS. Both PI and proposed controllers were implemented using T_z as a discretization step, using the same parameters determined in II through the design procedure.

The experimental results at 400 V input and 1.5 kW output power are provided in Fig. 8(a), showing v_o, i_L, and voltage and current of phase a (v_a and i_a). The control achieves voltage regulation at 300 V and a quasi-sinusoidal input current, with a power factor of 0.981. However, the phase current is very sensitive to the IVS transitions, causing the increase of THD, that was computed after performing a DFT analysis and was equal to 12%. The results under the same

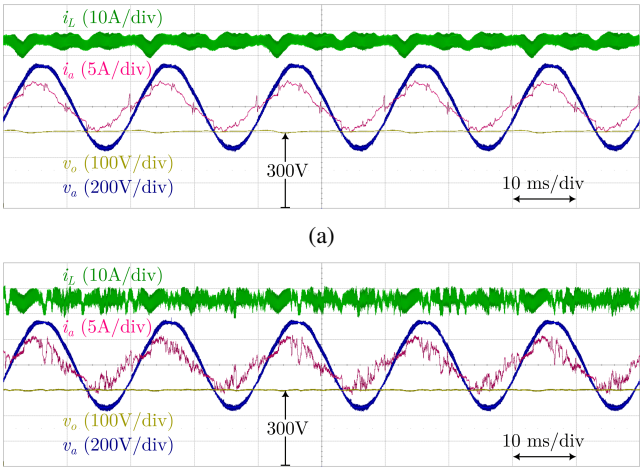


Fig. 8: Experimental results at 400 V input and $P_o = 1.5$ kW using the proposed IMC-based controller (a) and the conventional PI controller (b).

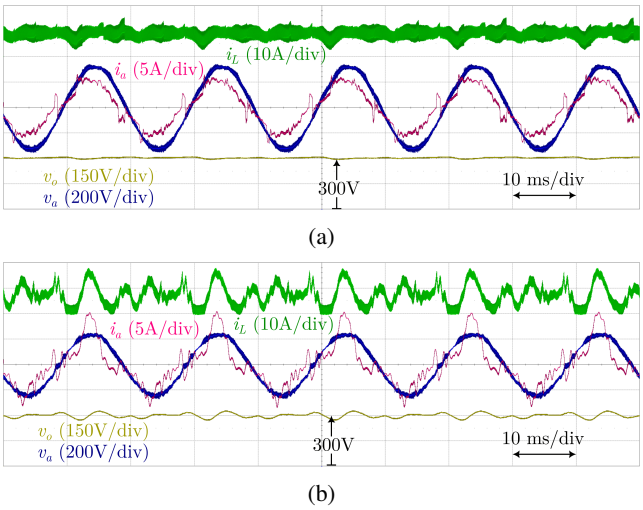


Fig. 9: Experimental results at 400 V input and $P_o = 3.0$ kW using the proposed IMC-based controller (a) and the conventional PI controller (b).

conditions but using the PI regulators are shown in Fig. 8(b). In this case, an evident instability appeared on i_L, reflecting also on v_o and i_a, and worsening the performances of the PFC converter in terms of THD of the phase current, which is about 27%.

Fig. 9(a) and (b) show the experimental results at 3 kW output power using the IMC-based controllers and the PI controllers, respectively. As in the previous case, the proposed controller allows to achieve v_o regulation at 300 V and an input current with power factor 0.985 and THD= 11%. Instead, the adoption of PI regulators causes the instability of i_L, impacting both the output voltage and the input current. In fact, the output voltage shows visible oscillations at low-frequency around the setpoint, while the phase current shows a THD of 31%.

The analyzed scenarios, although in static conditions, verify the superiority of the proposed IMC approach with respect conventional PI regulator in achieving voltage and power factor regulation for the Swiss Rectifier. Further tests will be conducted in the future to verify also dynamic performances of the PFC converter with the proposed control.

VI. Conclusion

The Internal Model Control was used to design the voltage and current controllers of the PFC Swiss Rectifier. The theoretical analysis showed the superior capability of this approach in absorbing uncertainties in the converter plant due to parameter variations and system delays, that often make the tuning process of PI regulators inadequate. PLECS simulations were used to analyze the impact of delays in the control loop and variation of the output capacitance, verifying the theoretical analysis. Finally, measurements on an experimental prototype of the Swiss rectifier were conducted at 1.5 kW and 3.0 kW output power. While the conventional PI regulators made the system unstable, the proposed control approach achieved static output voltage regulation and power factor of 0.985, with a 12% THD of the input current.

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