A Behavioral Model for Short-Circuit Operation of a GaN-based Half Bridge

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***Abstract*—The Short-Circuit (SC) robustness of GaN HEMTs represents a relevant issue for their use in power electronics. Hence, understanding and simulating their SC behavior is critical to develop a proper protection circuit, but, unfortunately, accurate simulations can be only achieved with numerical physics-based simulators, that includes all the physical phenomena involved in the real device, while they become less suitable for power electronics simulations. A behavioral model is proposed to accurately simulate in SPICE the SC behavior of GaN HEMTs and its impact in Half Bridges. The proposed model is derived by fitting the experimental results of gate and drain I–V characterization using equations introduced here for the first time. Experimental results conducted on the GaN-based Half Bridge are used to validate the model, that shows an improved capability in reproducing the main phenomena involved during the SC.**

***Index Terms*—GaN HEMTs, Short-Circuit, SPICE model, Half bridge**

I. Introduction

Many works investigated the Short-Circuit (SC) capability of normally-*off* Gallium Nitride High Electron Mobility Transistors (GaN HEMTs), describing the main processes involved in the SC, such as the self-regulation of the drain current and the increase of gate leakage current [1]–[4]. It was demonstrated that both phenomena are related to the increase of the junction temperature (T_j), that can reach very high values during the SC, leading to the device failure [5]–[7].

The assessments on the SC behavior of GaN HEMTs are often aided by numerical simulation tools, that use Finite Element Analysis (FEA) to obtain accurate and reliable results that can be useful for improving the devices' technology and analyze their electro-thermal behavior [6]–[8]. Even if this method provides the most reliable results, it is very little handy when simulating circuits with more than one power device, because of the complexity and the time-cost of simulations. For this purpose, system-oriented simulators like LTSpice are more convenient and all GaN HEMTs manufacturers provide simulation models for their devices. However, manufacturers' models are mainly focused on the nominal operation of the device, which hardly represent fully the phenomena related to the SC operation, such as the gate leakage current increase, leading to uncorrect simulation results. For this reason, the development of a protection circuit is often exclusively subjected to experimental characterizations on GaN HEMTs, slowing down the design process and requiring a major effort in terms of time and costs [9].

Several modeling approaches for GaN HEMTs exist in the literature, from behavioral to physics-based and numerical ones [10]. Behavioral models are preferred to simulate power converters, since they provide fast and sufficiently accurate results in comparison to physical and numerical ones. Many models derived from the Angelov model [11], that however was developed for normally-*on* GaN devices, while more recently different behavioral approaches have been proposed [12], [13], suitable also for SPICE implementation. However, a gate current model is not present and no attention is paid to abnormal operating conditions, such as the SC and adjunctive modifications to these models would be required to also describe the SC operation of the device.

In this work, a behavioral model for a p-doped gate GaN HEMT is proposed to evaluate its operation under SC. Both drain current and gate leakage current equations are derived from the experimental gate and drain I–V characterization. The validation of the model is provided by means of non-destructive SC tests on a Half Bridge (HB) employing 650-V/60-A GaN HEMTs [14].

Section II describes the methodology used for the drain and gate I–V characterization and the modeling approaches. The SC operation of the GaN-based HB is presented in section III, focusing on the operation of the two devices, while section IV provides a comparison among experimental tests under SC and simulations performed with the manufacturer's and the proposed model for different values of the DC-link voltage.

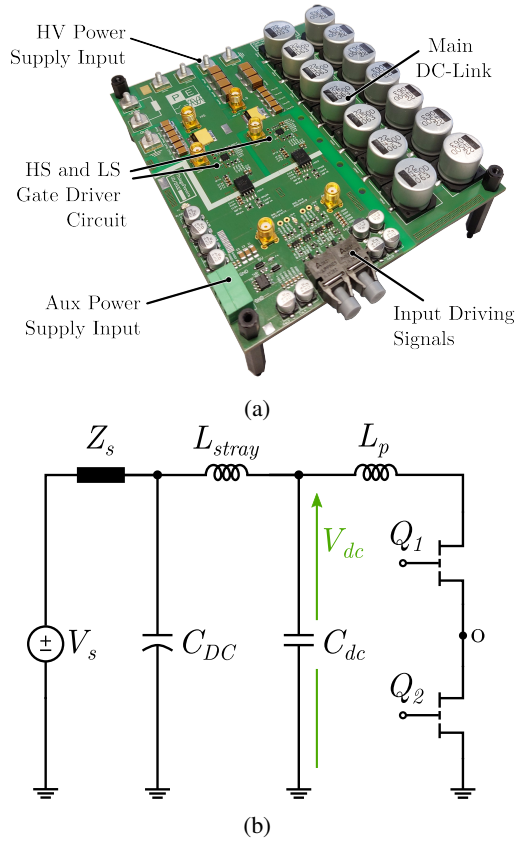


Fig. 1: Picture of the designed PCB with two 650-V/60-A GaN HEMTs in HB configuration (a) and its related simplified circuit scheme (b).

Then, section V summarizes the conclusions of this work.

II. Drain and Gate Modeling

The high T_j increase experienced by the GaN HEMT during the SC has been proven to affect both the drain current (I_D) and the gate leakage current ($I_{G,Lk}$) [5], [8]. To accurately model the SC behavior of the GaN HEMT, both I_D and $I_{G,Lk}$ experimental characterizations have been performed. For this aim, a board consisting of two 650-V/60-A GaN HEMTs in HB configuration was designed and constructed, that is also suitable for SC, double pulse and overload tests, besides as a primary stage for DC-DC converters [15]. The picture of the board is shown in Fig. 1 along with its simplified schematic of the power section, that includes a real voltage source, the DC-link capacitors and the parasitic inductance.

The drain and gate characterizations were performed on the low-side (LS) device, that can be considered as the device under test (DUT), while the high-side (HS) one is used to apply the DC-link voltage (V_{dc}) on the drain of the DUT.

A. Characterization and modeling of Drain current

The temperature dependence of I_D of the selected device is well defined in the manufacturer's datasheet [14], but a little information is provided on the operation of the HEMT in its saturation region. The output characteristics are limited to the region where $V_{DS} < 5$ V, while the transfer characteristic is provided at $V_{DS} = 10$ V. However this data are not thorough enough to determine the I_D behavior in both the linear and the saturation regions. Since during the SC the device operates in saturation, as better clarified in the following, it is of paramount importance to determine its behavior for higher V_{DS}. Therefore, a pulsed gate I–V characterization was led at different V_{GS} and constant T_j to determine the relationsip between I_D, V_{DS} and V_{GS}. The input voltage V_s was increased to reach at least the knee of the saturation region for each V_{GS}. The DUT's V_{GS} was varied from 2.0- to 6.0-V in 1.0 V steps and the input voltage V_s was changed from 0.5- to 30.0- V. The case temperature T_C was measured with a thermal camera during the tests and it was at 23 °C.

The measured peak drain current and the value of V_{DS} at which the peak I_D occurs are used to build the drain I–V curves, that are plotted in Fig. 2. The grey region represents the area of the graph that is covered by data in the manufacturer datasheet, that does not provide sufficient information about the saturation region of the device, as it can be seen from the figure. On the contrary, the experimental data obtained through this characterization are sufficient to derive a mathematical model to fit I_D also in the saturation region.

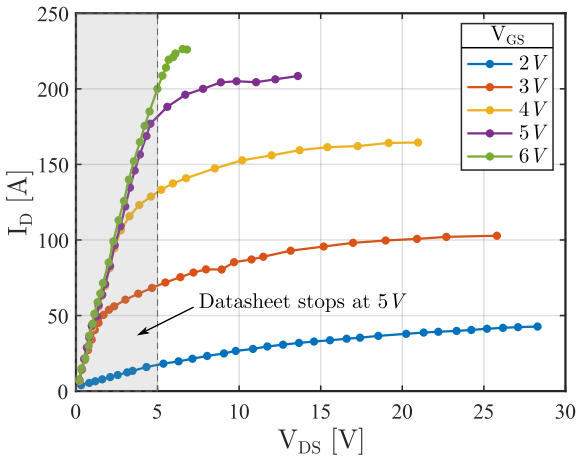


Fig. 2: Experimental results of the pulsed gate I–V characterization of the DUT at different V_{GS} and T_j = 23 °C.

The SPICE model provided by the manufacturer uses three equations, defining a controlled current source and two variable resistances that simulate the access resistance of drain and source side of the device [14]. Starting from these equations and exploiting the I–V characterization an unique and fully descriptive equation for I_D is proposed, expressed by

$$I_D = \alpha(T_j) \cdot \beta(V_{GS}) \cdot \gamma(V_{GS}, V_{DS}) \cdot (1 + \delta V_{DS}) \quad (1)$$

where the functions $\alpha(T_j)$, $\beta(V_{GS})$ and $\gamma(V_{DS})$ are respectively

$$\alpha(T_j) = I_0(a_1 - a_2(T_j - T_0)) \quad (2)$$

$$\beta(V_{GS}) = ln(1 + e^{b(V_{GS} - V_{th})}) \quad (3)$$

TABLE I: Constant parameters for the drain current model.

Drain Current Model					
Symbol	***Value***	***Unit***	***Symbol***	***Value***	***Unit***
I_0	0.105	A	b	26.0	V^{-1}
T_0	25	°C	V_{th}	1.60	V
a_1	174.1	-	δ	-0.0004	V^{-1}
a_2	0.798	$°C^{-1}$			

$$\gamma(V_{GS}, V_{DS}) = \\ = L_1(V_{GS}) tanh\big[h_1(V_{GS})V_{DS}^3 + k_1(V_{GS})V_{DS}\big] + \\ + L_2(V_{GS}) tanh\big[k_2(V_{GS})V_{DS}\big] \quad (4)$$

The function $\alpha(T_j)$ incorporates the thermal dependence of I_D, while the function $\beta(V_{GS})$ is used to shape the transfer characteristic of the GaN HEMT, defining the dependence with V_{GS} and the threshold voltage V_{th}. Both the functions $\alpha(T_j)$ and $\beta(V_{GS})$, with their parameters, are taken from the manufacturer model. On the other hand, $\gamma(V_{GS}, V_{DS})$ is the proposed function used to achieve the best fit of the experimental data of the I–V characterization and to integrate the device model. It uses L_1, L_2, h_1, k_1, k_2 as the fitting parameters of the I–V curves for each V_{GS}. Finally, the term $1 + \delta V_{DS}$ is used to model the I_D reduction in the saturation region, introducing a negative output resistance. All the constant parameters used in (1)–(3) are listed in Table I.

The fitting parameters of the function $\gamma(V_{GS}, V_{DS})$ (see (4)) are dependent on V_{GS} and they have been extracted using a MATLAB code implementing the Levenberg-Marquardt algorithm. Their values have been computed for the five tested values of V_{GS}, from 2- to 6- V in 1 V steps. After obtaining the values of the parameters for each V_{GS}, they have been interpolated using the piecewise cubic hermite interpolating polynomial (PCHIP). Fig. 3 shows the values of the fitting parameters at each tested V_{GS} and the related interpolation.

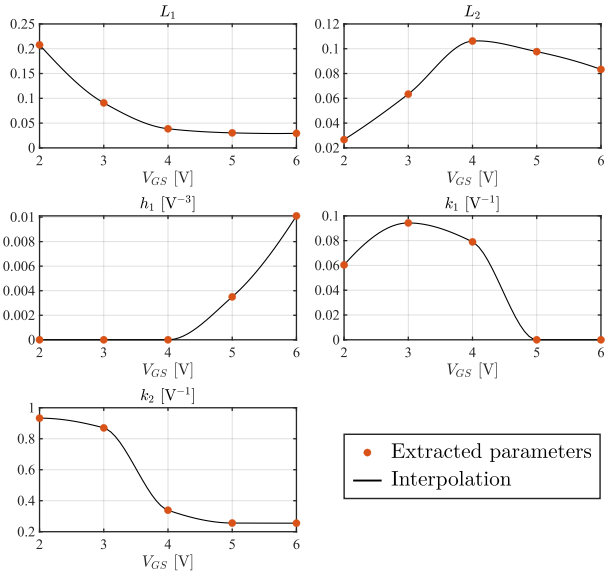


Fig. 3: Fitting parameters of function $\gamma(V_{GS}, V_{DS})$ for the I_D model. The red dots represent the values obtained from the fitting of the experimental data, while the black lines are the interpolation of the extracted data.

The drain current model expressed by (1) was compared with the experimental data and the manufacturer model, evaluated with LTSpice simulations in the same conditions of the experimental tests. The comparison is shown in Fig. 4, where the dots represent the experimental values of the I–V characterization, the dash-dotted lines refer to the manufacturer model and the solid lines refer to the proposed one. It is clear that the manufacturer model is less accurate in the saturation region, while the proposed one fits the correct behavior of the GaN HEMT both in saturation and linear region.

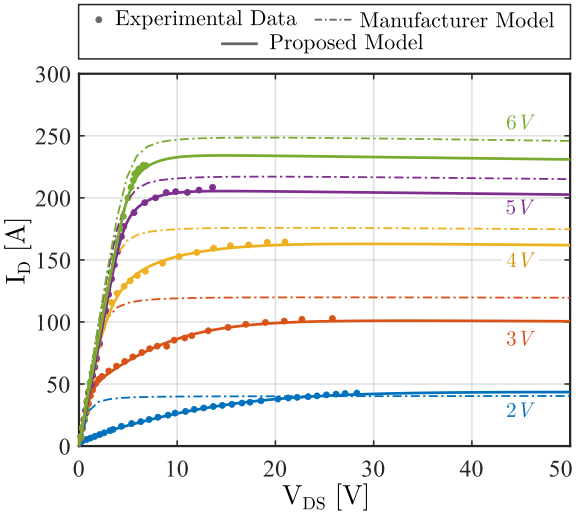


Fig. 4: Comparison of the proposed I_D model with the manufacturer one and the experimental data of the I–V characterization.

B. Characterization and modeling of Gate leakage current

While the temperature dependence of I_D is well defined and described by the manufacturer, almost no information is provided for $I_{G,Lk}$ apart from its nominal value under static conditions, that is equal to 320 μA at V_{GS} = 6 V and T_j = 25 °C [14]. For this reason, also the impact of T_j was considered during the tests.

The experimental gate I–V characterization was performed using the SCS-4200A parameter analyzer [16] and a second identical PCB with only the DUT mounted on it. The case temperature of the DUT was set through a controllable heating source placed on the thermal pad of the device and it was varied from the ambient temperature (25 °C) up to 170 °C, waiting for the thermal steady state for each imposed T_C, in the way that T_j = T_C. After reaching the thermal steady state, the gate I–V characterization was performed with the parameter analyzer, that varied V_{GS} from −4- to 6- V in 0.25 V steps and imposing V_{DS} = 0 V. A thermal camera connected to a PC was used to measure the DUT's temperature in different points of its case, to include the temperature distribution along the case itself. At the thermal steady state,

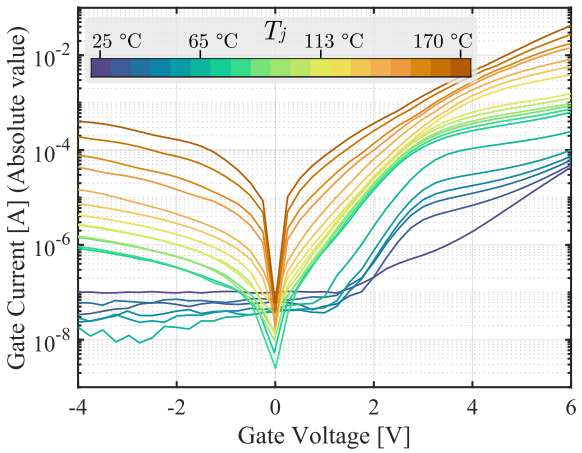


Fig. 5: Experimental results of gate I–V characterization of the DUT at V_{DS} = 0 V and different T_j from 25 °C to 170 °C in a logarithmic scale of the current.

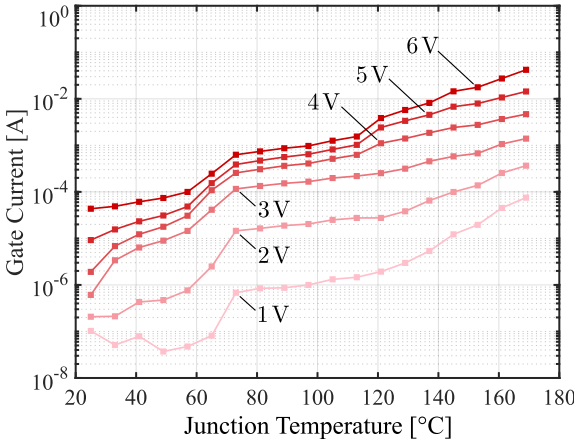


Fig. 6: Gate current dependence with T_j of the DUT for positive values of V_{GS} (V_{DS} = 0 V).

T_j was computed as the average of the measured temperatures at those specific points and the maximum temperature gradient between the hottest and the coldest points of the case was 14 °C.

The results of the gate I–V characterization are plotted in Fig. 5 versus V_{GS} at different T_j values in a logarithmic scale of the current. The temperature was varied in about 8 °C steps according to the test procedure described above.

To analyze the temperature dependence of $I_{G,Lk}$, the experimental data of Fig. 5 have been extracted at constant V_{GS} values and plotted versus T_j in Fig. 6. Since the GaN HEMT is commonly driven in the *off* state with V_{GS} = 0 V and $I_{G,Lk}$ mainly impacts the operation of the device during its *on* state, only positive values of V_{GS} have been considered.

Considering V_{GS} = 6 V, the gate current is about 30 μA at 25 °C, resulting an order of magnitude lower than the rated current defined in the datasheet. This can be attributed to the fact that the datasheet shows only the characteristics of a typical device and the variation range of its parameters. For the gate leakage current, however, no boundaries are defined and therefore a straight comparison with the value defined by the manufacturer has a little relevance. $I_{G,Lk}$ becomes ten times higher at 70 °C and about 10 mA at T_j = 150 °C, which is the maximum operating temperature for the DUT, as stated in the datasheet. As visible in Fig. 6, the T_j dependence is also of exponential type, exhibiting an increase of about three orders of magnitude in the operating range 25 – 150 °C. The gate current becomes even larger during the SC operation of the device, where significantly higher T_j is reached because of the huge instantaneous power dissipation, and so it can be a sensitive indicator of the SC event, since the fast increase of T_j is strictly linked to that of $I_{G,Lk}$.

The results of the gate current characterization were used to derive a simple behavioral model of $I_{G,Lk}$ for positive values of V_{GS}, depending on V_{GS} and T_j. A similar approach was presented in [17], where a different behavioral model is proposed and used to determine T_j during the operation of the GaN HEMT, though a little information about the fitting procedure is provided. In the proposed approach, the curves of $I_{G,Lk}$ versus T_j of Fig. 6 have been used to perform an exponential regression of the experimental data. Since the curves are obtained for six values of V_{GS}, from 1- to 6- V in 1 V steps, if each curve is identified by the index $k = 1, \ldots, 6$ referring to the specific V_{GS} at which the regression is applied, the exponential regression is expressed by

$$f_k(T_j) = I_{G0} \cdot e^{r_k(T_j)} \tag{5}$$

where I_{G0} is a constant parameter, equal for all k values, and

$$r_k(T_j) = m_k T_j + q_k \tag{6}$$

is the fitting equation for the data in Fig. 6, since in logarithmic scale (5) becomes $ln(f_k(T_j)/I_{G0}) = r_k(T_j)$ and the experimental data show a quite linear trend in this scale. In this equation, m_k and q_k are the fitting parameters.

The trust-region algorithm implemented in MATLAB was used to derive m_k and q_k for each k and the obtained values of the fitting parameters are reported in Fig. 7. After noticing that the m_k values were very close to each other, a simplified exponential regression was computed considering a unique coefficient m for all the curves, computed as their average value, also shown in Fig. 7(a). The values of q_k incorporate the V_{GS} dependence and have been also interpolated using a rational function $q(V_{GS})$, expressed by

$$q(V_{GS}) = \frac{n_1 V_{GS} + n_2}{d_1 V_{GS} + d_2} \tag{7}$$

where the parameter d_1 is set to 1.0 and used just to guarantee the adimensionality of the denominator. The values of the coefficients q_k with their interpolation are shown in Fig. 7(b).

Therefore, the final expression for $I_{G,Lk}$, incorporating both T_j and V_{GS} dependence, is

$$I_{G,Lk}(V_{GS}, T_j) = I_{G0} \cdot e^{mT_j + q(V_{GS})} \tag{8}$$

All the constant parameters used in (8) are listed in Table II.

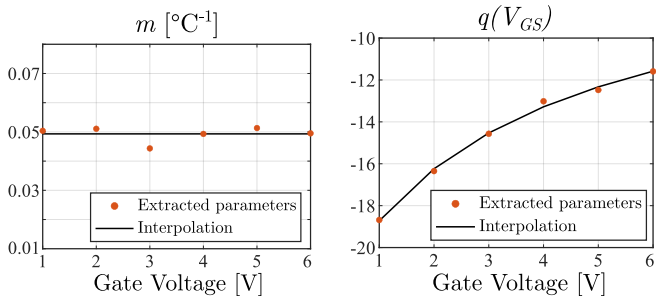


Fig. 7: Values of parameters m_k (a) and q_k (b) and their related interpolation used for the exponential regression of $I_{G,Lk}$.

TABLE II: Constant parameters for the gate current model.

Gate Current Model					
Symbol	***Value***	***Unit***	***Symbol***	***Value***	***Unit***
I_{G0}	10.0	nA	n_2	–14.46	-
m	0.049	°C^{-1}	d_1	1.0	V^{-1}
n_1	13.14	V^{-1}	d_2	3.41	-

The proposed $I_{G,Lk}$ model was compared to the experimental results of the gate I–V characterization to evaluate its accuracy. Fig. 8 shows the experimental data of $I_{G,Lk}$ versus T_j, previously plotted in Fig. 6, with the related exponential regressions for each selected V_{GS}. The exponential regression without simplification (see (5)), i.e. using the extracted values of m_k and q_k for each k, are represented with dash-dotted lines, while the simplified exponential regression, expressed according to (8), is represented with solid lines.

As visible in Fig. 8, the simplification coming from using the same coefficient m for all the curves does not strongly affect the regression of the data, except for the case of V_{GS} = 3 V, where the error is larger.

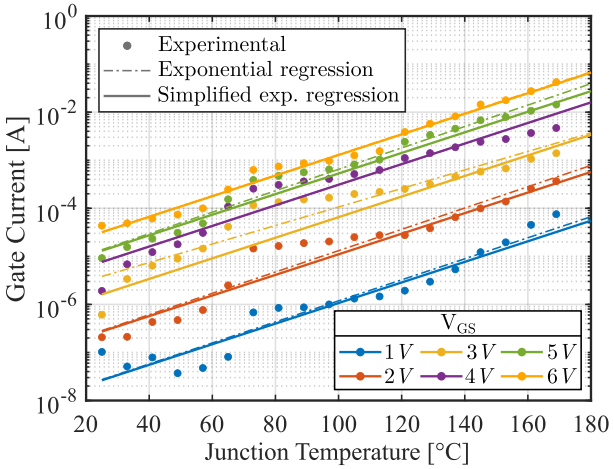


Fig. 8: Comparison among the experimental data of $I_{G,Lk}$ versus T_j (dots), exponential regression (dash-dotted lines) and simplified exponential regression used to derive the gate current model (solid lines).

III. Short-Circuit Operation of a GaN-based Half Bridge

As the main purpose of this work is to provide a reliable simulation model for the SC operation of a GaN-based HB, it is necessary to analyze the behavior of the two devices under SC before proceeding to validate the model. Considering the simplified scheme of Fig. 1, a SC can be created on the HB by turning on one device when the other one is already conducting. Let us suppose that Q_1 is *on* and all V_{dc} is blocked by Q_2. At the time instant t_0 Q_2 is also turned on and a SC is triggered for the time duration T_{SC}, after which Q_2 turns off again. During this time, Q_2 experiences a type I SC, while Q_1 undergoes a type II SC.

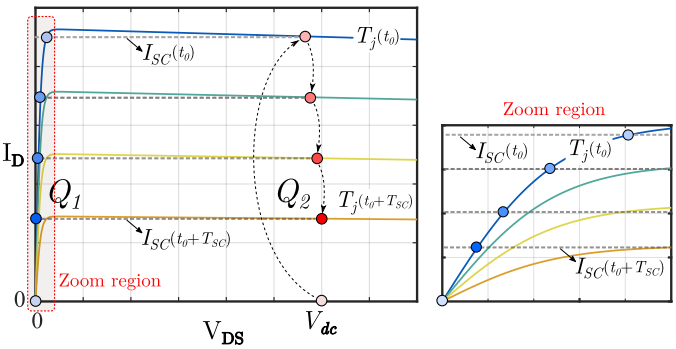


Fig. 9: Theoretical operating points on the I–V output characteristic during the SC of a GaN-HB.

As shown in Fig. 9, the operating point of Q_2 (red circles) stays in the saturation region and the device behaves like a controlled current source while blocking almost all V_{dc}, establishing the SC current I_{SC} in the HB. Assuming the same gate voltages V_{GS} and junction temperature T_j and neglecting other effects, at $t = t_0$ Q_1 and Q_2 work on the same output characteristic and the operating point of Q_1 (blue circles), is determined by the intersection of its characteristic with that of Q_2. The high power dissipation on device Q_2, approximately given by $V_{dc}I_{SC}$, causes a sudden increase of its T_j and the downshifting of the I–V characteristic towards lower values of current until the end of the SC ($t = t_0 + T_{SC}$). As I_{SC} decreases, the operating point of Q_1, neglecting its lower T_j increase, still remains on the initial characteristic (blue line) and goes more and more in its linear region. So, in this specific case, the SC current I_{SC} is determined by the operating point on the output characteristic of Q_2, while Q_1 behaves like a current-controlled resistance defined by its $R_{DS,on}$.

IV. Validation of the Model under Short-Circuit

The validation of the model for the 650-V/60-A GaN HEMT was carried out comparing the LTSpice simulations with the experimental results in SC conditions. Both the manufacturer's and the proposed models are used in the simulation environment to evaluate the accuracy with the real behavior of the device. Non-destructive SC tests are conducted on the designed Half-Bridge (HB) prototype at V_{GS} = 5 V and ambient temperature, for different values of V_{dc}, from 50-

to 400-V. The SC pulse-width was set to T_{SC} = 5 μs. In this case, a 5 V driving voltage was preferred in order to avoid the possible failure of the device at high V_{dc} with the recommended 6 V driving voltage, which has been proven to happen in less than 1 μs [1]. Anyway, this condition is also suitable for practical applications thanks to the low threshold voltage (1.7 V typical) of the 650-V/60-A GaN HEMT and the slight increase of the *on*-resistance compared with V_{GS} = 6 V, that remains lower than 1.5% at I_D = 20 A. A 100-Ω gate resistance was selected for the GaN HEMTs, as large gate resistors are used in the majority of the SC tests presented in the literature to slow down the switching transients and avoid turn-off oscillations and instabilities [1]–[3], [18].

For the experimental tests, a 4 channel/1-GHz high definition oscilloscope was used with 500-V/500-MHz voltage passive probes to measure V_{GS} and V_{DS} of the low-side (LS) device and V_{dc}, while a 1500-V/120-MHz differential probe was used to measure V_{GS} of the high-side (HS) device. The current I_D was measured through a Rogowski current transducer with 20.0 mV/A sensitivity and 16-MHz bandwidth. V_{DS} of device Q_1 was not directly measured during the tests, but it was numerically obtained in the post-processing from the voltage balance in the output loop as $V_{dc} - V_{DS,Q2} - L_p dI_D/dt$, where L_p is the total parasitic inductance in the power path.

The simulated circuit is shown in Fig. 10(a) and it includes the parasitic elements measured with a vector network analyzer on the real prototype, which are reported in Table III with all the other parameters set for the simulation. Both the experimental tests and the simulations were executed according to the driving signals of Fig. 10(b).

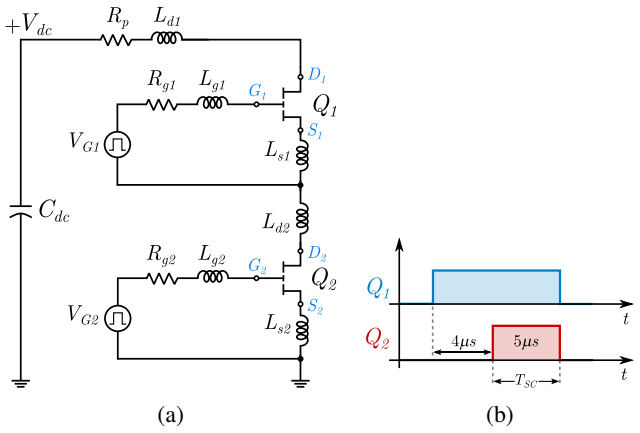


Fig. 10: Circuit used in simulation based on the real prototype board (a) and driving signals for the SC tests (b).

The results of the experimental SC test at V_{dc} = 300 V are shown in Fig. 11. At the beginning of the SC event, Q_2 blocks all V_{dc} and I_D rises in 400 ns up to 170 A, causing a high *di/dt*, that is responsible for the transient variation of V_{DS} of the two devices. At this point, both the HEMTs are in saturation, but Q_2 suffers from a higher power dissipation that rapidly increases its T_j, causing the downshifting of its output

TABLE III: Parameters used in the simulation.

Parameter	Value	Parameter	Value
V_{dc}	50 – 400 V	L_{g1}, L_{g2}	1.0 nH
V_{G1}, V_{G2}	0 – 5 V	L_{d1}, L_{d2}	3.0 nH
Q_1, Q_2	GS66516T	L_{s1}	0.8 nH
C_{dc}	308 μF	L_{s2}	1.2 nH
R_{g1}, R_{g2}	100 Ω	R_p	10 mΩ

characteristic. Therefore, as explained in the previous section, V_{DS} of Q_2 increases towards V_{dc}, while V_{DS} of Q_1 decreases and the device goes to the linear region. The effect of T_j is clearly visible on I_D, that at the end of the SC decreased to 42 A, and on V_{GS} of Q_2, that starts from 4.80 V and then drops to 2.90 V, with a 40% reduction.

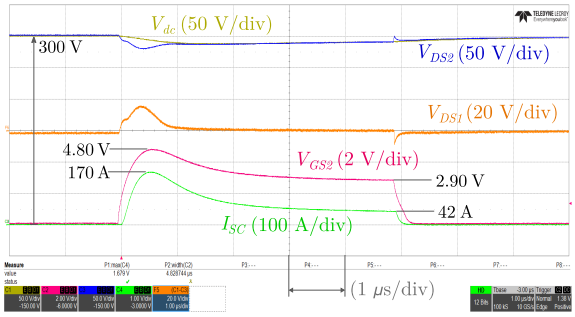


Fig. 11: Experimental waveforms of the SC test on the GaN-based HB in the conditions V_{dc} = 300 V, T_{SC} = 5 μs, R_G = 100 Ω. The current is measured with a 20 mV/A Rogowski probe.

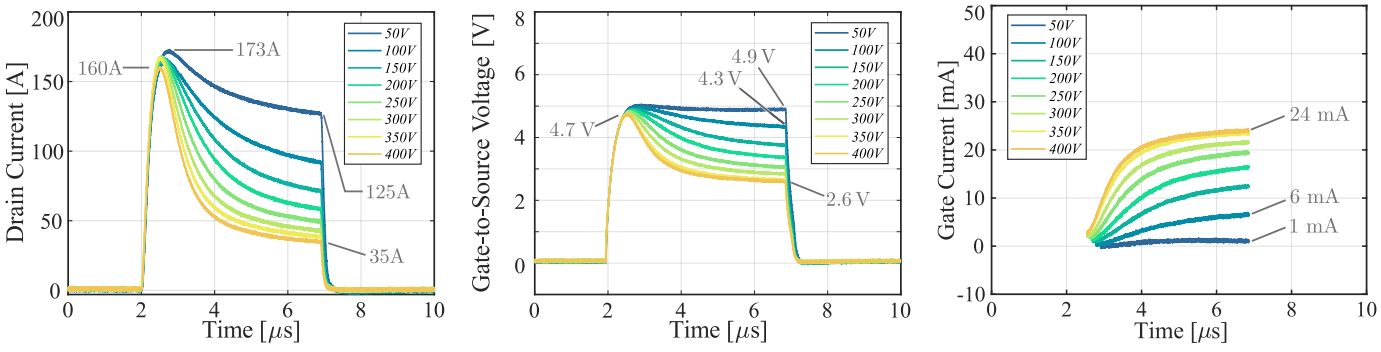
The experimental waveforms of I_D, V_{GS} and $I_{G,Lk}$ of device Q_2, plotted in Fig. 12 for all the tested V_{dc}, are used to validate the proposed model. $I_{G,Lk}$ was not directly measured on the prototype, but it was estimated from the V_{GS} waveforms between the turn-on and turn-off transients according to

$$I_{G,Lk} = \frac{V_G - V_{GS}}{R_G + R_{d,out}} - \frac{V_{GS}}{R_{GS}} \tag{9}$$

where $R_{d,out}$ is the output resistance of the driver, equal to 3 Ω, and R_{GS} is a 10 kΩ pull-down resistor placed in the circuit between gate and source of the device.

The results of the simulations using both the manufacturer model and the proposed one were compared with the experimental waveforms for each condition. However, to simplify the discussion and the visualization of the results, two V_{dc} values are considered in the following, namely 100- and 400-V. In fact, in these conditions the experimental results show considerable variations and therefore are suitable to validate the model in two different extreme conditions. Moreover, for a better comparison of the waveforms, the driving signals used in simulation were delayed of 200 ns at the turn-off compared with the experiemental ones, leading to the delay of the turn-off time instants for V_{GS} and I_D.

The I_D waveforms simulated using the manufacturer model are compared with the experimental ones in Fig. 13. The



(a) (b) (c)

Fig. 12: Experimental waveforms during the SC tests for a V_{dc} variation from 50- to 400- V in the conditions V_G = 5 V, R_G = 100 Ω: (a) drain current, (b) gate voltage and (c) estimated gate leakage current of device Q_2.

manufacturer model overestimates I_D at both 100- and 400- V. The peak values of the simulated current are 200 A and 175 A at 100- and 400- V respectively, with respect the real 165 A and 160 A. At the same time, the reduction of I_D due to the T_j increase does not represent the real behavior of the current. In fact, an overestimation of about 30 A is made at 100 V and 15 A at 400 V.

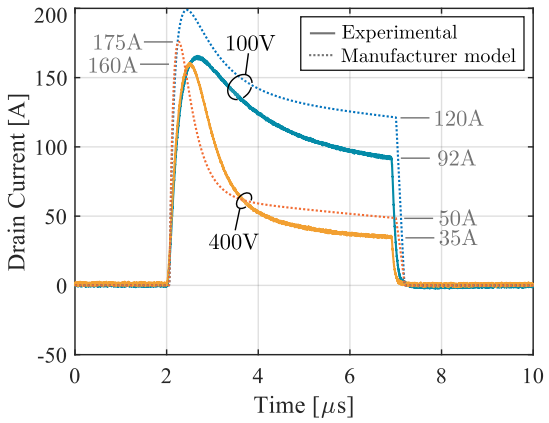


Fig. 13: Comparison between experimental and simulated waveforms of I_D using the manufacturer model for V_{dc} equal to 100- and 400- V.

The drain current is much more realistic with the proposed model, that accurately simulates both the peak and the final values, as shown in Fig. 14. The error in estimating the peak value is less than 2 A and the difference between the experimental data and the simulated ones with the proposed model is mainly linked to the thermal model of the device, that probably underestimates the thermal time-constant of the real device.

It must be noted that the thermal model is the manufacturer's one and it is used for the simulations of both Fig. 13 and Fig. 14. Therefore, the difference in the final values of I_D using the manufacturer's and the proposed model is exclusively linked to the V_{GS} reduction because of the increase of $I_{G,Lk}$. This means that $I_{G,Lk}$ effectively plays a role in the self-

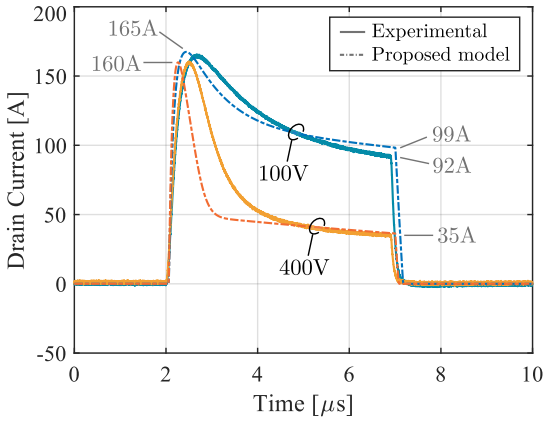


Fig. 14: Comparison between experimental and simulated waveforms of I_D using the proposed model for V_{dc} equal to 100- and 400- V.

regulation mechanism of the drain current during the SC event and its impact is only valuable with the proposed model, that takes into account the increment of $I_{G,Lk}$ with T_j, providing a reliable instrument to characterize the SC behavior of the GaN HEMT under study.

In fact, the proposed model can follow the real variation of V_{GS}, as shown in Fig. 15(a), while V_{GS} remains fixed to 4.9 V with the manufacturer model because of the negligible $I_{G,Lk}$. Using the proposed model, V_{GS} decreases to 4.6 V at V_{dc} = 100 V, while the real value is about 4.3 V, and decreases to 2.7 V at V_{dc} = 400 V, that is very close to the real measured value of 2.6 V (cf. Fig. 15(a)). In addition, the estimated $I_{G,Lk}$ at 100 V and 400 V increases up to 6 mA and 24 mA, respectively. The manufacturer model does not incorporate this variation, and $I_{G,Lk}$ remains negligible. Instead, using the proposed model leads to a value of $I_{G,Lk}$ equal to about 3 mA and 24 mA at 100- and 400- V, respectively, which is very close to the estimated value. Therefore, the proposed model can predict the increase of $I_{G,Lk}$ and the correspondence with the experimental results confirms that the model is correct, although it could be further improved.

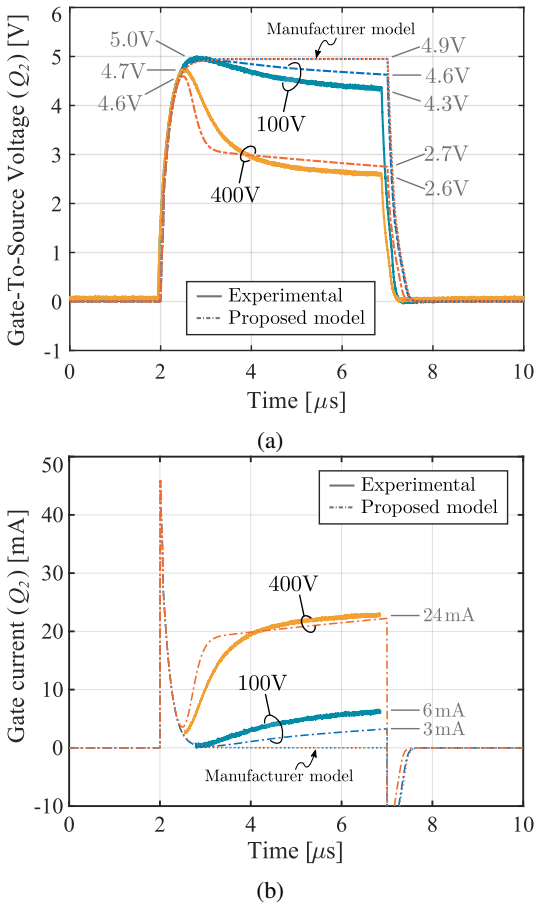


Fig. 15: Comparison between experimental and simulated waveforms of V_{GS} with manufacturer's and proposed model (a) and simulated $I_{G,Lk}$ (b) for V_{dc} equal to 100- and 400- V.

V. Conclusion

The analysis of the SC operation of a GaN-based half-bridge requires a reliable model to accurately simulate the behavior of the GaN HEMT. In this paper a behavioral model for the 650-V/60-A GaN HEMT was developed considering the real drain and gate current behavior, derived from the I–V characterization. Two fitting equations were used to express the drain and gate current dependence with V_{GS}, V_{DS} and T_j. They have been implemented in LTSpice, integrating the manufacturer model, and used to accurately simulate the operation of a half-bridge during SC. The drain current model provides an accurate determination of the GaN HEMT's operation in saturation, without losing accuracy in the linear region. The gate leakage model, absent in in other behavioral models in the literature and also in the manufacturer's one, is able to determine the impact of $I_{G,Lk}$ on the self-regulation mechanism of I_D during the SC, that was not possible before. The experimental validation with non-destructive SC tests confirmed the goodness of the model, that therefore can become an useful instrument to simplify the design process of a protection circuit against short-circuit.

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