Heavy-Ion Induced Single Event Gate Damage in Medium Voltage Power MOSFETs

Giovanni Busatto, Giuseppe Currò, Francesco Iannuzzo, Antonino Porzio, Annunziata Sanseverino, and Francesco Velardi

***Abstract*—Starting from a physical model of the electric field that develops in the gate oxide during heavy-ion irradiation, we have experimentally and numerically investigated the single event gate damage observed in medium voltage power MOSFETs. Simulation results reveal that the total electric field reached during the heavy-ion impact is close to the one that is known to trigger the formation of latent damages during electro-static discharge (ESD) experiments.**

***Index Terms*—Latent gate damage, power MOSFETs, SEGR.**

I. Introduction

POWER MOSFETs are very important devices for aerospace applications; unfortunately their ability to safely operate in this radiation environment is drastically reduced by two failure mechanisms induced by the impacts of single energetic particles: the single event burnout (SEB) and the single event gate rupture (SEGR).

Many papers dedicated to SEGR of power MOSFETs report experimental evidence of such a phenomenon [1], [2] and correlate it to characteristics of the penetrating ions (LET, range, energy, angle, etc.) [3]–[8] to the technological characteristics of the samples (cellular or stripe structures, oxide thickness, cell pitch, etc.) [9]–[17] and to its biasing conditions (gate and drain voltage, temperature, etc.) [18], [19].

In [20], a conceptual model of the phenomenon was also presented that attributes the gate rupture to the large increase in the electric field $\mathrm{E_{OX\_SI}}$ across the gate oxide layer due to the motion of the generated carriers in the silicon structure and underneath the gate after the ion impact.

A supplemental increase in the electric field across the oxide was indicated in [9], and in [21] it was invoked to explain SEGR of large area MOS capacitors used in linear operational amplifiers. This component of the electric field, indicated as $\mathrm{E_{INT}}$ in [21], is due to the holes that survive in the oxide after the ion strike. In fact, when an energetic particle passes through the gate oxide, electron-hole pairs are generated in a narrow column around the ion track. A fraction of electrons and holes recombines. The remaining electrons are rapidly swept out of the oxide in less than 0.3 ps thanks to their higher diffusivity and mobility. Instead, the survived holes in the oxide are reasonably immobile during the event time. As a consequence of immobile holes and fast removal of electrons the abovementioned incremental electric field, $\mathrm{E_{INT}}$ reaches its maximum in less than 0.3 picoseconds [21]. While this component was only qualitatively indicated in [9] it was numerically computed in [21], where it was added to the electric field due to the external bias in order to get the net total electric field across the oxide, $\mathrm{E_{OX}}$. It was shown [21] that, in critical conditions, $\mathrm{E_{OX}}$ overcomes the threshold of 13 MV/cm that is able to induce a current through the oxide and cause its rupture. It is worth outlining that $\mathrm{E_{INT}}$ was not explicitly indicated in [9], [11], or [15] because its effects are included in the critical voltage that is experimentally measured by the authors.

Besides SEGR, other radiation induced damages at the gate oxide are reported in the literature. In particular a radiation induced leakage current (RILC) is observed after heavy-ion irradiation both in thick [22] and in thin/ultra thin oxides [23]–[26]. Moreover, radiation induced soft breakdowns (RSB) are also observed in these latter oxides [27]–[32]. It was also demonstrated that both RILC and RSB are enhanced by ESD stress performed after the irradiation. In [33] the authors demonstrated that the combination of ESD and radiation damage may have a non-marginal impact on the reliability of advanced CMOS devices in space electronics. They demonstrated that heavy-ion strikes on floating MOSFETs produce only modest changes in the devices' electrical characteristics, but may decrease the ESD breakdown voltage. They attributed this reduction to the presence of "latent damages" left by the heavy-ion strikes in the gate oxide. The authors in [33] used the term "latent damages" to indicate a modification of the physical characteristics of the oxide which are weakly detectable during or right after the irradiation but may cause the oxide destruction when a post irradiation gate stress is applied to the device.

The formation of latent damages has also been observed in power MOSFETs [34]–[36], which have much thicker gate oxide. The creation of latent defects [34] or latent damages [35] is correlated to the observation of a step by step increase in the gate leakage current, $\mathrm{I_{GSS}}$, measured during the irradiation. It was also demonstrated [34] that these steps must be attributed to the multiple impacts in a small area of the gate oxide. On the other hand, the formation of latent damages was observed even in very low fuence experiments where no step by step increase was observed in $\mathrm{I_{GSS}}$ during the irradiation [36]. In this latter case the latent damages were revealed by a post irradiation gate bias.

The formation of latent damage in relatively thick oxides ($\sim 30\ \mathrm{nm}$) similar to the ones used in power MOSFETs was also observed in charge device model ESD (CDM-ESD) [37]. It was demonstrated that these damages are related to the formation of

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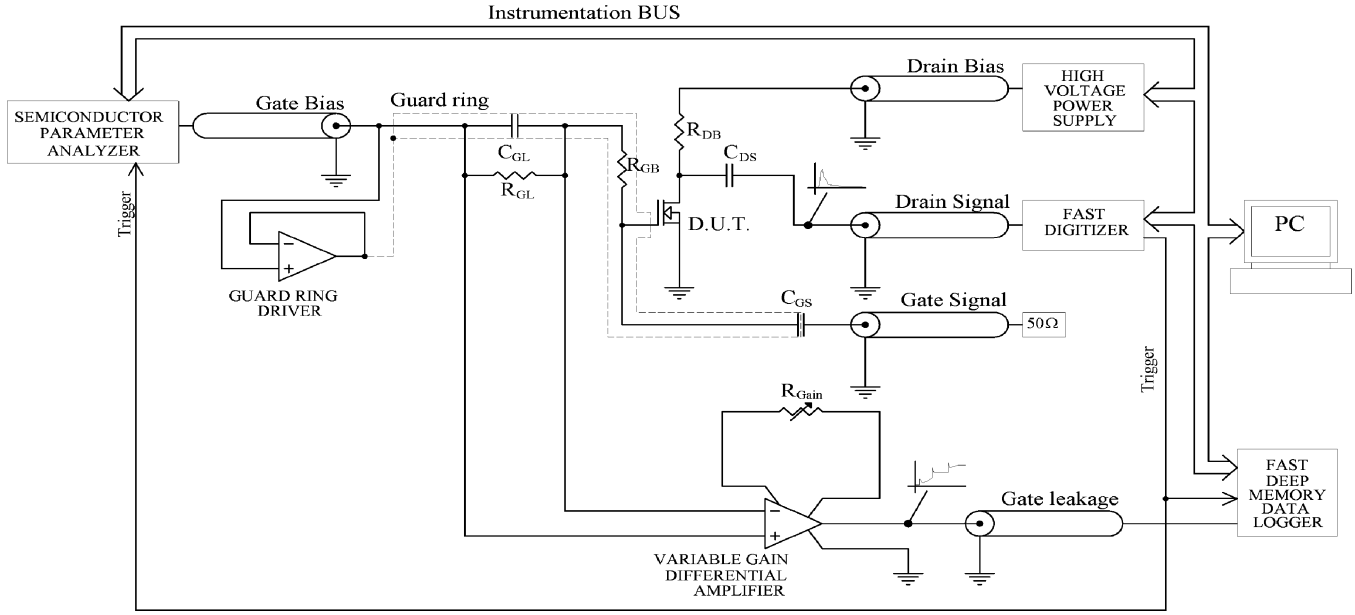

Fig. 1. The experimental set-up used for the experiments.

amorphous silicon "melt balls". They are created because of a too rapid cooling of the silicon that was previously melt by a large power dissipation caused by the conduction of a current through the oxide for a short time (~ 2 ns). The electric field able to induce this conduction was estimated to be 15 MV/cm, which is not far from the threshold indicated in [21] for SEGR to take place.

The objective of this paper is to study the formation of latent damages in medium voltage power MOSFETs. It will be proposed that, for the tested devices, the formation of a latent damage has a mechanism similar to an SEGR with the difference that the energy involved in a latent damage formation is not enough to totally break the gate oxide.

A low fluence irradiation two-phase procedure has been developed that is able to induce a limited number of latent damages during heavy-ion irradiation and to reveal them by a post irradiation biasing that does not overstress the device. 3D finite element numerical simulation was used to evaluate the oxide electric field component $\mathrm{E_{OX\_SI}}$ related to the charge deposition in the silicon. In addition the model reported in [21] was used to evaluate the $\mathrm{E_{OX\_HO}}$ contribution related to the holes surviving in the oxide right after the ion strike. The overlay of these two components gives an origin to a total electric field that overcomes, for a very short time after the ion impact, the threshold voltage that is known to start the conduction through the gate oxide and cause the formation of latent damages in ESD experiments [37].

The presentation of the proposed experimental procedure reported in Section IV is preceded by the description of the experimental set up in Section II where we also compare the proposed circuit with the one typically used in the heavy ion irradiation tests. Moreover, the results of the high fluence irradiation experiments, which are normally used to study the heavy ion single effects, are reported in Section III in order to connect them to the results of the newly proposed low fluence irradiation experiments depicted in Section V.

The experiments were conducted on MOSFET devices having equivalent gate oxide layers but different widths of the neck region. Both simulation and experiment confirm that the pitch reduction causes a reduction in the sensitivity of power MOSFETs to the latent damages [15].

II. Experimental Set-Up

The schematic of the experimental circuit is shown in Fig. 1. It is similar to the basic SEB/SEGR test circuit indicated by MIL-STD-750D method 1080. The capacitors $\mathrm{C_{DS}}$ and $\mathrm{C_{GL}}$ play the same role in both circuits, and the resistors $\mathrm{R_{GL}}$ and $\mathrm{R_{DB}}$ are used as picoammeters. The two resistors used in method 1080 to limit $\mathrm{I_D}$ and $\mathrm{I_G}$ during the strike are set to zero in our circuit.

The experimental set-up is constructed in order to achieve:

- the best behaviour in terms of signal to noise ratio due to the very low levels exhibited by the measured signals;
- minimal effects of the stray parasitic inductance of the circuit;
- the external terminations of the measurement circuit adapted to the impedance of the cables (50 Ω) due to the very fast variations in the measured signal, which exhibits a rise time of less than 1 ns.

During the exposure, drain and gate leakage currents are monitored in order to identify the values of $\mathrm{V_{DS}}$ and $\mathrm{V_{GS}}$ at which the gate and/or the drain structures become damaged; moreover, the current waveforms related to each ion impact are acquired and the related charges are numerically computed as the time integrals of the current. The section of the experimental circuit devoted to detecting the drain and the gate pulses is the same as the circuit used for the SEB/SEGR characterisation we described in [19]. It is worth outlining that the mean value of pulse peaks measured by the oscilloscope during the irradiation is much larger than the trigger level used for the acquisition. Moreover, we used the oscilloscope in the fast frame mode where no blanking time is experienced by the instrument during the whole

single irradiation test. As a consequence we can assume that the current pulses resulting from practically all the impacting ions are acquired. In such a way we can count the exact number of ions that impact on the device active area during each test.

The experimental set-up includes a high resolution parameter analyser (Agilent B1500 A) that allows us to study the increase in leakage current with high resolution. The parameter analyser forces a V_{GS} bias to the device and allows us to monitor the time evolution of I_{GSS} in real time during the irradiation test. The time resolution of the parameter analyser, as it is used in our experiments, is 1 ms hence the effects of the stray parameters of the cables extinguish themselves well before the settling of current to be measured and does not affect the accuracy of I_{GSS} acquired by the instrument.

Furthermore, to minimize the offset in the measurement of the leakage current, we have also introduced a shielding ring that surrounds all the wires and the connections to the gate lead. This shielding ring is kept to the same potential of the gate by an ultra-low bias operational amplifier. In such a way we can reduce the leakage current of the circuit to about 1.3 nA at $V_{GS} = -10$ V.

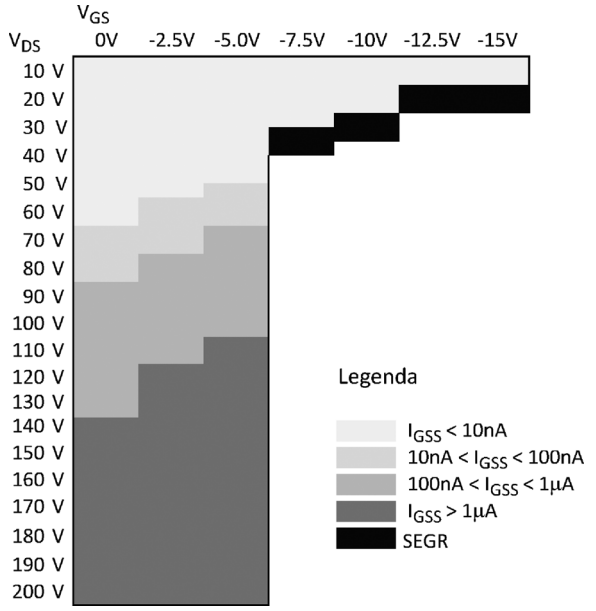

Fig. 2. The map of the I_{GSS} gate leakage.

III. Gate Oxide Degradation due to Heavy-Ion Impacts

Previous works dealing with SEGR of power MOSFETs [1]–[15] typically report the values of V_{DS} and V_{GS} at which SEGR takes place without pointing out the test conditions at which latent damages can be created. As a first step of our experimental work we used the experimental set-up of Fig. 1 and we performed our irradiations in such a way to point out also those situations where SEGR does not take place but gate damages are detected. This helps us in identifying the operating conditions where we have to focus our attention.

In this part of the experiment we used a relatively high fluence ($\sim 10^4$ ions/cm^2) in order to connect our results with previous works. In facts, for low V_{GS}, the gate damage is typically evidenced by a progressive increase in the gate leakage current during the irradiation as it happens with a cumulative effect and, in some cases, also a step by step increase of I_{GSS} is observed [34]–[36]. For higher gate voltages an SEGR takes place that is revealed by a huge increase in the gate current and the subsequent oxide rupture.

To obtain the experimental data, each device was irradiated with heavy ions at fixed V_{DS} and V_{GS} until the desired ion fluence was reached. Gate leakage current was measured during the irradiation but it is not reported here for brevity. After each irradiation the device was biased at $V_{GS} = \pm 10$ V and $V_{DS} = 0$ V for one minute at the end of which the gate leakage current (I_{GSS}) was measured. For the fixed values of V_{GS} and V_{DS}, if no gate damage was observed, V_{DS} was increased and the test sequence repeated. The experiment was stopped when either an SEGR took place or $I_{GSS} > 1$ μA was measured. It is worth outlining that $I_{GSS} > 1$ μA does not always correspond to an SEGR and very often the I_{GSS} of the device recovers after a thermal or room temperature annealing. Instead, SEGR can be recognized because it is accompanied by a large increase of gate leakage current during the irradiation and the oxide loses its isolation characteristics.

Our experimental results are summarized in Fig. 2 where a greyscale map of the gate leakage current I_{GSS} as a function of V_{GS} and V_{DS} is reported for a commercial 200 V power MOSFET. The white area represents the bias conditions where the I_{GSS}, measured after the irradiation, was less than 10 nA. The black colour indicates the bias conditions at which an SEGR is observed. The light grey, grey and dark grey regions indicate the bias conditions for which 10 nA $< I_{GSS} <$ 100 nA, 100 nA $< I_{GSS} <$ 1 μA and $I_{GSS} > 1$ μA, respectively. This decade range sequence was chosen in order to have a reasonable resolution at low values of I_{GSS} without losing information at the higher values.

Fig. 2 indicates that for $|V_{GS}| > 7.5$ V the device experiences an SEGR which corresponds to a complete failure of the gate oxide ($I_{GSS} > 10$ mA at $V_{GS} = 10$ V). The value of V_{DS} at which SEGR takes place decreases linearly with V_{GS}. A similar behaviour was observed in the literature [2], [11], [12], [14] for power MOSFETs having J-FET regions wider than 3 μm as happens for the device under test whose J-FET is 7.4 μm wide. For $|V_{GS}| < 7.5$ V gate damages are evidenced. The critical V_{DS} at which these gate damages start to be created, that is the upper boundary of the light grey region in Fig. 2, also decreases linearly with the increase in V_{GS}.

The objective of the next sections is to investigate about the behaviour of the power MOSFET in this latter biasing region which can be considered as a gradual pre-SEGR region and where the formation of latent damages is typically observed.

IV. Experimental Procedure

To study the formation of latent damages in the gate oxide below the SEGR bias region ($|V_{GS}| < 4$ V) we developed a two-phase experimental procedure:

(a) During the first phase (the "irradiation phase") we irradiated the device being tested in order to create latent damages. We used a very small bromine flux (~ 10 ions/(cm^{2}s)) for less than 50 s. In each exposure

TABLE I
THE DEVICES TESTED AND SIMULATED

MOSFET	Gate Oxide Thickness	Neck Width	Epitaxial Layer Thickness
A-type	35nm	7.4μm	22μm + 18μm (buffer layer)
B-type	35nm	5.4μm	22μm + 18μm (buffer layer)
C-type	35nm	3.4μm	22μm + 18μm (buffer layer)

we counted in total between 30 and 50 ions impacting on the device active area ($\sim 0.11\ \mathrm{cm}^2$), corresponding to the fluence of about 270 to 450 $\mathrm{ions/cm}^2$. Such a small fluence was used to avoid any total dose effect that may mislead the interpretation of the results. The absence of these effects was confirmed by the measurement of the static subthreshold MOSFET characteristics, which evidenced no changes after the irradiation. The use of this very small fluence forced us to bias the device during the irradiation with high $\mathrm{V_{DS}}$, in order to increase the sensitive area and, consequently, significantly increase the probability of creating latent damage, as will be demonstrated by the simulation results reported in the next sections.

(b) During the second phase ("post irradiation gate bias", PIGB), the ion beam was stopped and the device was biased for at least 3000 s in order to activate the possible latent damages produced during the exposure. We used gate and drain bias conditions that guaranteed an electric field across the oxide significantly lower than the Fowler-Nordheim conduction limit, thus avoiding a further stress on the oxide that could have altered the evolution of the phenomenon.

V. EXPERIMENTAL RESULTS

We have tested three specifically constructed prototypes which are rated to 200 V and have the same gate layer except for different neck widths. The main geometrical parameters of the devices tested are summarised in Table I.

The irradiation experiments were conducted at the Laboratori Nazionali del Sud, INFN, Italy. The devices were irradiated with $^{79}\mathrm{Br}$ ions at 223 MeV, and the corresponding energy loss and range were evaluated by using the SRIM (Stopping and Range of Ions in Matter) tool [38]. The SRIM simulations have been performed on a multilayer sequence which reproduces the vertical structure of a typical power MOSFET with a blocking voltage capability of 200 V. The linear energy loss in the gate oxide layer and at the body-drain junction was estimated to be 1000 eV/Å and 950 eV/Å respectively; furthermore the longitudinal range was estimated to be 30 $\mu\mathrm{m}$.

The first experimental result refers to an A-type power MOSFET that was irradiated at $\mathrm{V_{GS}} = 0\ \mathrm{V}$ and $\mathrm{V_{DS}} = 160\ \mathrm{V}$ with 223 MeV $^{79}\mathrm{Br}$ ions. The gate leakage current had not increased during the irradiation, as shown in Fig. 3, where the $\mathrm{I_{GSS}}$ time evolution during the whole exposure time is reported. After the irradiation the device was biased with $\mathrm{V_{GS}} = -10\ \mathrm{V}$ and $\mathrm{V_{DS}} = 160\ \mathrm{V}$ in order to activate the latent damages. In Fig. 4, the $\mathrm{I_{GSS}}$ time evolution during PIGB is reported.

The figure indicates that micro-damages inside the gate oxide were formed during the exposure and subsequently activated by the applied electric field during the second PIGB phase. We repeated the experiment on other two samples of the same type at the same bias conditions and obtained similar results. In Table II a summary of the samples tested and the related irradiation test conditions are reported.

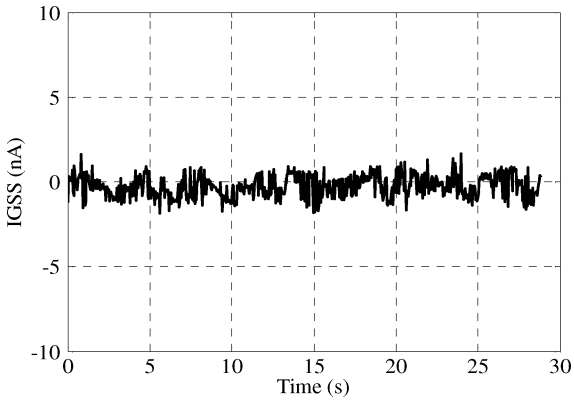

Fig. 3. The gate leakage current during the irradiation at low ion flux for the A-type MOSFET at $\mathrm{V_{DS}} = 160\ \mathrm{V}$ and $\mathrm{V_{GS}} = 0\ \mathrm{V}$.

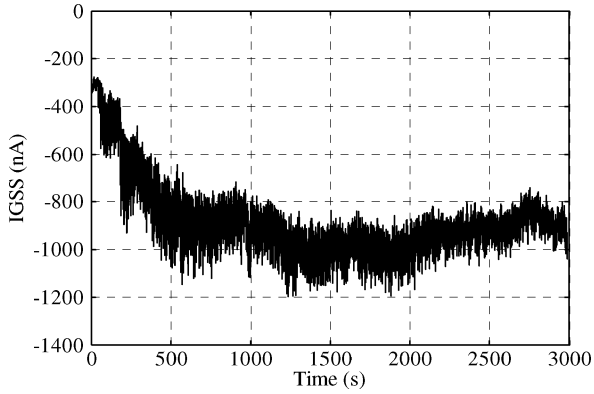

Fig. 4. $\mathrm{I_{GSS}}$ time evolution during PIGB at $\mathrm{V_{GS}} = -10\ \mathrm{V}$ and $\mathrm{V_{DS}} = 160\ \mathrm{V}$ of the A-type MOSFET, after exposure at $\mathrm{V_{DS}} = 160\ \mathrm{V}$ and $\mathrm{V_{GS}} = 0\ \mathrm{V}$.

TABLE II
THE SAMPLES TESTED

MOSFET	# Samples	$\mathrm{V_{DS}}$ [V]	$\mathrm{V_{GS}}$ [V]	Gate damage evidenced by PIGB
A-type	3	140	0	NO
	3	160	0	YES
B-type	2	160	0	NO
	3	180	0	YES
C-type	3	160	0	NO
	2	180	0	NO
	3	190	0	YES

Subsequently, the same experiment, with the same bias conditions, was performed on two samples of the B-type device with a reduced neck width. However, in this case PIGB had revealed no micro-damages, as shown in Fig. 5, where the corresponding $\mathrm{I_{GSS}}$ time evolution is reported for one of the two experiments.

The reason for this reduced sensitivity to latent damage formation can be found in the lower neck width of the B-type devices. In fact, a lower electric field $\mathrm{E_{OX\_SI}}$ develops in their gate

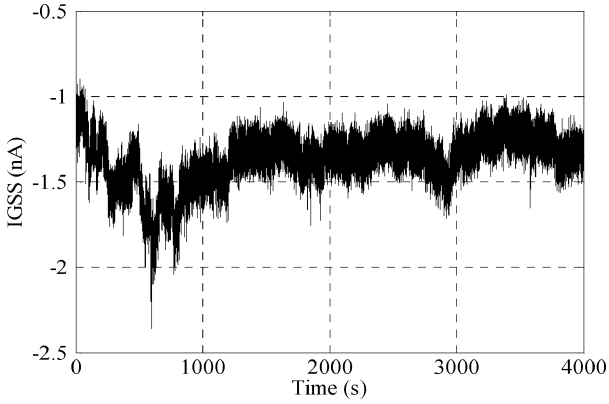

Fig. 5. I_{GSS} time evolution during PIGB at $V_{GS} = -10\,V$ and $V_{DS} = 160\,V$ of the B-type MOSFET, after exposure at $V_{DS} = 160\,V$ and $V_{GS} = 0\,V$.

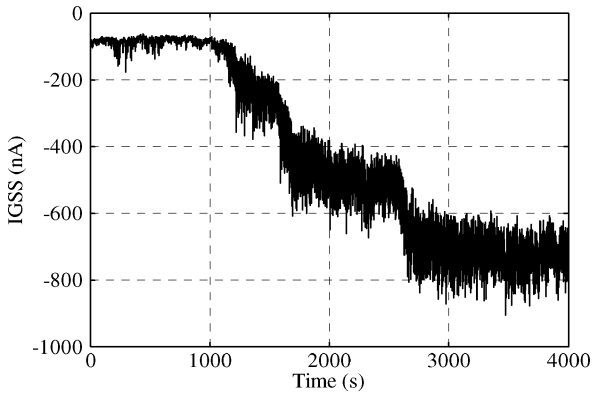

Fig. 6. I_{GSS} time evolution during PIGB at $V_{GS} = -10\,V$ and $V_{DS} = 180\,V$ of the B-type MOSFET after exposure at $V_{DS} = 180\,V$ and $V_{GS} = 0\,V$.

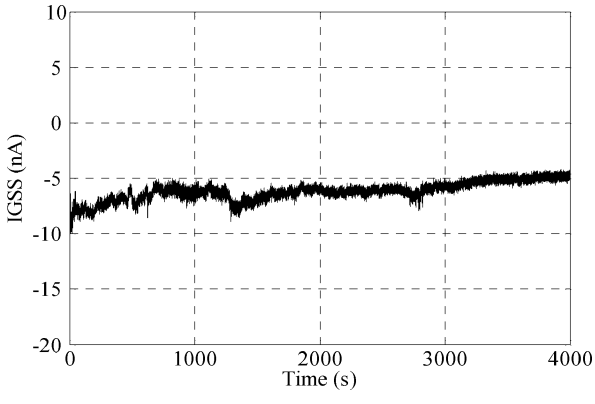

Fig. 7. I_{GSS} time evolution during PIGB at $V_{GS} = -10\,V$ and $V_{DS} = 180\,V$ of the C-type MOSFET after exposure at $V_{DS} = 180\,V$ and $V_{GS} = 0\,V$.

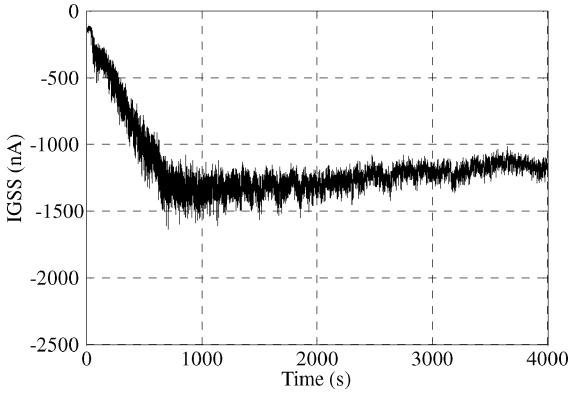

Fig. 8. I_{GSS} time evolution during PIGB at $V_{GS} = -10\,V$ and $V_{DS} = 190\,V$ of the C-type MOSFET after exposure at $V_{DS} = 190\,V$ and $V_{GS} = 0\,V$.

oxide as a consequence of the charge generation in the silicon structure, as was demonstrated in [15] and will be confirmed for our devices by the simulation results reported in the next sections. The other component of the electric field E_{OX_HO}, due to the holes surviving in the oxide layer, is the same for the A- and B-type MOSFETs. In fact, they have the same gate structure, so that during its passage the ion generates the same amount of electron-hole pairs in the gate oxide of both devices. The electrons move out of the oxide in less than 0.3 ps when E_{OX_SI} is still too low to affect both the electrons removal and the amount of the surviving holes and, therefore, it does not affect E_{OX_HO}. Consequently, the total electric field E_{OX} resulting from the overlay of the two contributions, E_{OX_SI} and E_{OX_HO}, is lower for the B-type device and causes a reduced probability of creating latent damages in these test conditions.

To obtain latent damages in B-type devices with low fluence we had to increase the V_{DS} during the irradiation phase up to 180 V, as shown in Fig. 6, where the PIGB time evolution related to a B-type device is reported. It shows that I_{GSS} increases step by step with a fairly regular increase of about 200 nA at each step. We repeated the experiment on other two samples with similar results.

This trend is confirmed by the experimental behaviour of the C-type devices. The further neck width reduction makes the C-type gate structure more robust against the latent damage formation; in fact, the PIGB of the C-type device after the exposure at $V_{DS} = 180\,V$ and $V_{GS} = 0$ revealed no latent gate damage, as indicated in Fig. 7.

In order to create gate damages in the C-type structure, it was necessary to increase the drain voltage during the irradiation to $V_{DS} = 190\,V$. In Fig. 8, the PIGB of the C-type device after exposure at $V_{DS} = 190\,V$ and $V_{GS} = 0\,V$ is reported.

Figs. 4, 6 and 8 show that the time evolution of I_{GSS} during PIGB is not the same for the different experiments. In fact the waveforms differ from each other both in the time at which the I_{GSS} starts to increase and in the shape of its evolution. We propose here that the activation of latent damage sites is a statistic process and is influenced both by the biasing conditions and the position where the site is created. The mechanism of the conduction through the oxide is of statistic nature and is influenced by the electric field that develops in the oxide which is strongly affected by the charge that is accumulated in the damaged area. In particular the small current flow induces a progressive increase of the accumulated charge that causes the increase of the local electric field whose time evolution follows the charge accumulation.

It is worth outlining that the application of the same bias conditions used for PIGB tests on fresh devices did not reveal any increase in the gate leakage current. As an example, in Fig. 9 we report an I_{GSS} time evolution of a fresh B-type device for $V_{DS} = 180\,V$ and $V_{GS} = -10\,V$ (the conditions used for the experiment described in Fig. 6).

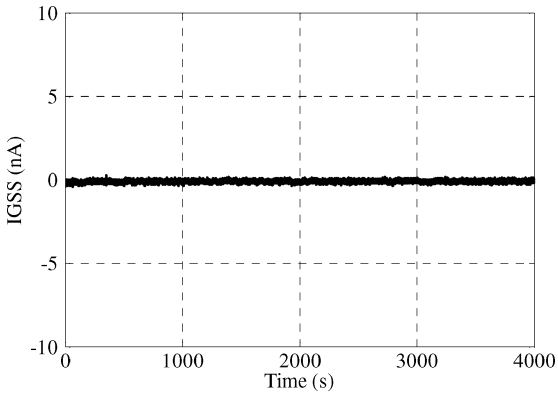

Fig. 9. I_{GSS} time evolution with $V_{GS} = -10$ V and $V_{DS} = 180$ V for a fresh B-type device.

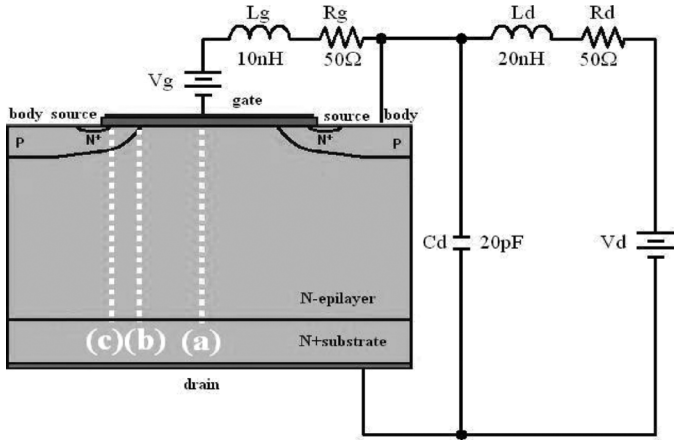

Fig. 10. The simulated elementary cell with lumped elements.

VI. The Numerical Simulation

In order to confirm the role played by the electric field E_{OX_SI} in the gate micro-damages, the above experimental results were analysed by means of 3D finite element simulations performed using the ATLAS TCAD simulation tool by Silvaco International [39].

The simulations are 3D to allow us to describe the intrinsic 3D nature of the device structure. The information regarding the simulated structures was supplied by the 2D process simulator ATHENA from Silvaco International [40], which is able to simulate the entire technological process described by the process flow chart used during the fabrication of the devices. The 2D process simulation from ATHENA was used to extrapolate a 3D structure using DEVEDIT3D from Silvaco International [39].

In order to simulate the 3D effects of the ion impact better, a complete MOSFET cell was simulated, incorporating the full thickness of the epitaxial layer including the buffer layer that is used to reduce the electric field in the silicon. For simulation purposes, the source and body contacts were connected to each other to ensure the actual short present in the MOSFET structure between those electrodes.

The models used in the simulation have been chosen to include the main physical mechanisms taking place when a heavy ion impacts on the device [15]. The correctness of the choices was verified by comparing simulated on and off state characteristics of the power MOSFET with the corresponding experimental ones.

Special attention has been dedicated to the model that describes the charge deposition on the device structure during the heavy-ion strike. The impact of the particle is simulated by the deposition of a large number of electron and hole pairs along its trajectory. We have used a modified version of the standard charge deposition model included in ATLAS simulator [39] that accurately describes both the shape of the volume where the charge is deposited and its time evolution according to the following law:

$$Q(r,z,t) = \frac{N(z)\cdot \exp\left(-\frac{r}{R}\right)\cdot \exp\left(-\left(\frac{t-to}{tc}\right)^2\right)}{tc\cdot\sqrt{\pi}\cdot erfc\left(-\frac{to}{tc}\right)}. \quad (1)$$

This imposes an exponential reduction in the generated charge along the radius perpendicular to the trajectory, and a Gaussian law for the time variation. We have used the spatial decay constant R and constants to and tc of the Gaussian time evolution reported in the papers [9], [20] which performed simulation of impact of Br ion with energy similar to the one we have used in our experiments.

Contrarily to the standard ATLAS model, we have used a variable concentration of the deposited charge $N(z)$ along the ion track. It was evaluated by using the computed values of the energy deposited by the heavy ion along the z direction as they come out from SRIM program. The ion range resulting from SRIM was subdivided into 18 parts. Within each part, a constant value of generated charge was used. It was computed by using the mean value of the energy loss in the corresponding part obtained by SRIM. This choice is very important in order to accurately simulate the generated charge for which the approximation of a constant ions' LET is not realistic. An accurate estimation of the generated charge is very important for predicting the electric field that develops in the silicon region.

In order to simplify the simulation, we avoided the usage of mixed mode tools. With this purpose the experimental test circuit was described by lumped components that in ATLAS are accounted by proper boundary conditions at the external contacts. The schematic of the circuit obtained is shown in Fig. 10. It reports the elementary cell of the MOSFET where the impact takes place and the external circuit is summarised by the lumped elements. In particular, the coupling drain capacitors are substituted by two batteries, Vg and Vd; two Rd and Rg resistors have been introduced in order to take into account the 50 Ω resistance of the transmission lines in series with the input resistance of the oscilloscope. Two small inductances, Lg and Ld, are placed in series with the gate and drain networks, respectively, to account for the stray inductances of the circuit. A particularly important role is played by the capacitor Cd placed parallel to the simulated portion of the device. This capacitor accounts for the capacitance of the overall body-drain junction.

The correctness of the choices related to the simulation models, charge deposition model, and external circuit parameters was dynamically verified by the good agreement between the experimental and simulated amount of the charge generated

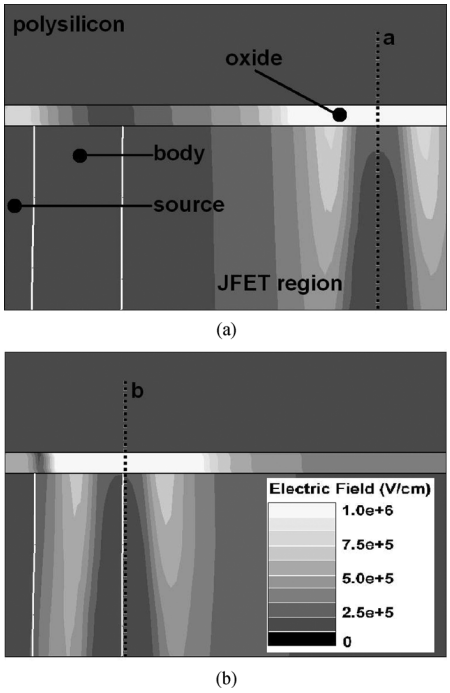

Fig. 11. The electric field distribution in the oxide layer for an ion impacting at the centre of the neck (a), and at the body boundary (b).

during the heavy-ion impact in several test conditions and for different device structures and parameters [18], [41].

In Fig. 10 three ion tracks perpendicular to the surface are also indicated. They correspond to the centre of the neck (a), the boundary of the body region (b), and the boundary of the source region (c). We used them as the ion tracks for the simulations.

VII. Simulation Results

The numerical model described in the previous section was employed to simulate the ion impact on the A-, B- and C-types power MOSFET at the bias conditions used in the experiments. We used the geometrical parameters of the experimentally tested devices reported in Table I for constructing the 3D mesh employed in the simulation.

The 2D distributions of the first component of the electric field, $\mathrm{E_{OX\_SI}}$, are reported in Fig. 11 for the A-type device in the cases when the ion impacts at the centre of the neck (a) and at the body boundary (b). The two pictures result from the cut of the 3D structure made on the charge deposition plane. The bias conditions are $\mathrm{V_{DS}} = 160\,\mathrm{V}$ and $\mathrm{V_{GS}} = 0\,\mathrm{V}$, at which the A-type device experimentally exhibited micro-damages during low fluence irradiation. The pictures are taken at about 3 ps when the electric field assumes its maximum value. In both simulated cases the spatial distribution of $\mathrm{E_{OX\_SI}}$ assumes its maximum value in the oxide in the position of the ion track. It keeps an almost constant value in the vertical direction and decreases significantly in the horizontal direction going away from the ion track.

The time evolution of the maximum value assumed by $\mathrm{E_{OX\_SI}}$ in the oxide is reported in Fig. 12 for the same bias conditions ($\mathrm{V_{DS}} = 160$ V and $\mathrm{V_{GS}} = 0$ V). Solid, dashed, and dash-dotted curves result from three different simulations

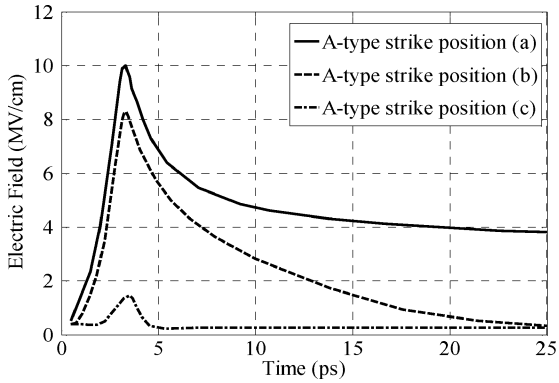

Fig. 12. The time evolution of the maximum value of $\mathrm{E_{OX\_SI}}$ for the A-type device at different ion strike positions ($\mathrm{V_{DS}} = 160\,\mathrm{V}$, $\mathrm{V_{GS}} = 0\,\mathrm{V}$).

referring to ion impacts taking place in the (a), (b), and (c) positions of Fig. 10, respectively. The curves were constructed by numerically identifying the maximum values assumed by the spatial distribution of $\mathrm{E_{OX\_SI}}$ at each time instant. The three curves show the presence of a single peak after about 3 ps which is associated with the strong surface charge density at the oxide-silicon interface, which induces an image charge at the polysilicon-oxide interface and causes the electric field to rise [9]. The value of this peak depends significantly on the position of the ion strike being at its maximum when the impact takes place at the centre of the neck, as demonstrated in [9] and confirmed by the results shown in Fig. 12. The figure shows that, for the A-type MOSFET at $\mathrm{V_{DS}} = 160\,\mathrm{V}$ and $\mathrm{V_{GS}} = 0\,\mathrm{V}$, where the device experimentally exhibits latent damage, the maximum value of the electric field caused by impacts at any position in the neck is comprised between 8 and 10 MV/cm, that are the values resulting from strikes at the boundary and at the centre of the neck, respectively.

The value of 8 MV/cm for $\mathrm{E_{OX\_SI}}$ was also observed in SEGR simulations for a negative gate bias when the device showed a gate rupture [9], [11]. In these papers the $\mathrm{E_{OX\_HO}}$ component was not explicitly indicated because its effects are included in the critical voltage that is experimentally measured. $\mathrm{E_{OX\_HO}}$ is associated with the holes that survive in the oxide after the ion strike due to the rapid outflow of the electrons having a much larger mobility than the holes [21], [42], [43]. It is worth outlining that this latter component was referred in [21] as $\mathrm{E_{INT}}$.

In this paper we want also evaluate $\mathrm{E_{OX\_HO}}$ in order to calculate the total electric field across the oxide that can be obtained as the overlay of $\mathrm{E_{OX\_SI}}$ and $\mathrm{E_{OX\_HO}}$.

We have developed a model based on [21] but not reported here, for brevity, that allowed us to compute a contribution for $\mathrm{E_{OX\_HO}}$ of about 6 MV/cm in the test conditions of the experiments presented in this paper. If we add this contribution to the $\mathrm{E_{OX\_SI}}$ reported in Fig. 12 we can observe that, for both the solid and dashed curves, the peak of the total electric field becomes larger than the threshold of 13 MV/cm that was recognised as causing SEGR of large area capacitors [21].

The time evolution of the maximum simulated $\mathrm{E_{OX\_SI}}$ for impacts at the centre of the neck is shown in Fig. 13 for the A- (solid line), B- (dotted), and C-type devices (dash-dotted) at

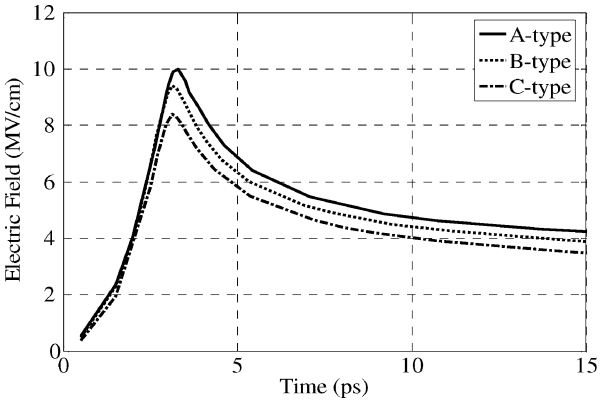

Fig. 13. The time evolution of the maximum value of E_{OX_SI} for A-, B-, and C-type MOSFETs for an ion impact at the centre of the neck, ($V_{DS} = 160$ V, $V_{GS} = 0$ V).

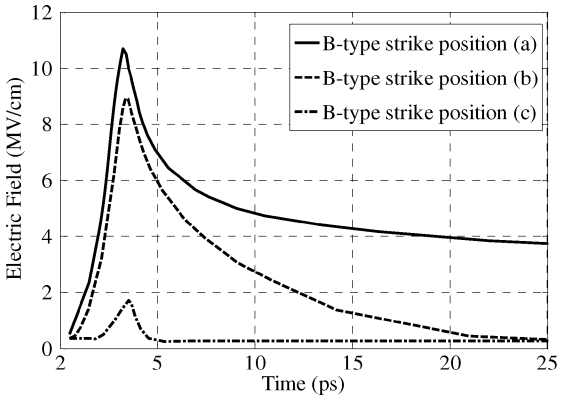

Fig. 14. The time evolution of the maximum value of E_{OX_SI} for the B-type device at different ion strike positions ($V_{DS} = 180$ V, $V_{GS} = 0$ V).

$V_{DS} = 160$ V and $V_{GS} = 0$ V. We can see that the maximum value of the electric field decreases by about 20% on passing from the A- to the C-type MOSFET for impacts at the centre of the neck.

It is worth outlining that the maximum value of E_{OX_SI} in the B-type MOSFET for an impact at the (b) position, not reported in Fig. 13, is about 7 MV/cm in the latter test conditions. To obtain a value similar to that of the A-type we had to increase V_{DS} up to 180 V, as shown in Fig. 14, where the time evolution of the maximum value of E_{OX_SI} is reported for the B-type MOSFET with $V_{DS} = 180$ V and $V_{GS} = 0$ V. Solid, dashed, and dash-dotted curves refer to impacts on the (a), (b), and (c) positions of Fig. 10, respectively. In this case we can also consider that the maximum value of the electric field caused by impacts at any position in the neck is practically comprised between 8 and 10 MV/cm.

VIII. Discussion

Simulation results presented in the previous section indicate that the maximum value of E_{OX_SI} is larger than 8 MV/cm for all the impacts taking place in any position in the neck region, at the biasing conditions where the samples experimentally exhibited the formation of latent damage ($V_{GS} = 0$ V and $V_{DS} =$ 160 V, 180 V and 190 V for the A-, B- and C-type MOSFET, respectively). For these ion strikes the maximum value of the total electric field, when adding 6 MV/cm for E_{OX_HO} to the field in Figs. 12 and 14, is larger than 13 MV/cm that was recognised as causing SEGR of large area capacitors [21]. This peak value is also very close to the threshold of 15 MV/cm at which latent damages are formed in the gate oxide during ESD tests [37].

It is worth outlining that during both heavy-ion irradiation and ESD experiments, the oxide is subject to a very high electric field for a very short time, so the two phenomena can be considered to have a similar nature [33]. In ESD events a very high electric field force a current to flow through the oxide and causes the increase of the local temperature beyond the fusion limit of the silicon. The consequent rapid temperature reduction causes the formation of amorphous silicon "melt balls" which act as latent damage sites.

During an SEGR the large electric field triggers the conduction through the oxide that is sustained by the negative gate biasing that supplies enough energy to destroy the oxide.

We are proposing here that the difference in the amount of the damages observed in SEGR and in the pre-SEGR region, for low V_{GS}, can be explained by the fact that at low gate bias the increase in the electric field during the impact disappears very rapidly and is insufficient to break the oxide. A PIGB may activate the latent damage and can cause gate failure.

Further work is required to find out the real threshold at which a latent damage is formed during heavy-ion irradiation and, because of the variation in electric field according to the position of the ion strike, a statistical analysis is required to get a realistic picture of the phenomena involved.

In our work, we used high biasing voltages in order to get a very high probability of generating latent damages. As demonstrated by the simulation the whole neck region can be considered to be the sensitive area for the formation of latent damages for the incident particle considered in the simulations. For the A-type MOSFET, the neck area is about 1/8 of the device active area and therefore the probability of creating a latent damage is very high even for experiments in which a very low number of ions (30–50) impacts on the device.

IX. Conclusion

An experimental and numerical investigation of latent damages in the gate oxide of medium voltage power MOSFETs during heavy-ion irradiation is presented. It shows that these latent damages are observed for high drain and low gate bias. Their nature is quite similar to SEGR phenomena even if they are not destructive during the irradiation.

Simulations performed under the biasing conditions where latent damages are experimentally observed indicate that the electric field across the oxide reaches, for a small time after the ion strike, values that are known to create latent damages during the ESD test and SEGR during heavy-ion irradiation experiments with large negative V_{GS}.

Simulation results indicate that for large values of V_{DS} all the ions impacting on any position of the neck region induce large values of the electric field so that the whole neck region can be considered to be the sensitive area for the formation of latent

damages. The probability of generating latent damages in these conditions is very high.

Finally, simulation results are coherent with experimental data and indicate that the sensitivity of medium voltage power MOSFETs to the formation of latent damages in low fluence irradiation experiments improves when the width of the neck's J-FET region is reduced.

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