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A Simple Thermal Model for Junction and Hot Spot Temperature Estimation of 650 V GaN HEMT during Short Circuit

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Abstract: Temperature is a critical parameter for the GaN HEMT as it sharply impacts the electrical characteristics of the device more than for SiC or Si MOSFETs. Either when designing a power converter or testing a device for reliability and robustness characterizations, it is essential to estimate the junction temperature of the device. For this aim, manufacturers provide compact models to simulate the device in SPICE-based simulators. These models provide the junction temperature, which is considered uniform along the channel. We demonstrate through two-dimensional numerical simulations that this approach is not suitable when the device undergoes high electrothermal stress, such as during short circuit (SC), when the temperature distribution along the channel is strongly not uniform. Based on numerical simulations and experimental measurements on a 650 V/4 A GaN HEMT, we derived a thermal network suitable for SPICE simulations to correctly compute the junction temperature and the SC current, even if not providing information about the possible failure of the device due to the formation of a local hot spot. For this reason, we used a second thermal network to estimate the maximum temperature reached inside the device, whose results are in good agreement with the experimental observed failures.

Keywords: GaN HEMT; junction temperature; short circuit; thermal model

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1. Introduction

Latest generation wide band-gap (WBG) power devices are increasingly used in power electronics applications, replacing the well-established silicon (Si) power MOSFETs and IGBTs, as they can achieve higher efficiency and power density [1,2]. Silicon carbide (SiC) technology has already reached a high level of maturity, operating across a wide range of power and voltage levels with high thermal stability, robustness, and reliability. On the other hand, gallium nitride high electron mobility transistors (GaN HEMTs) are still prone to robustness issues, e.g., when operating under short circuit (SC) conditions [3–6].

Many studies have been conducted on the SC behavior of GaN devices: from capability and degradation [3,7–9] to instability [10,11] and failure mechanisms analysis [12,13]. All these works state that the junction temperature (T_j) has a major impact on the GaN HEMT's SC behavior, causing the drain current collapse and the increase in the gate leakage current, contributing to realizing the self-regulation mechanism of the SC current. In addition, in [12–14] the temperature is found to be the main cause of the device failure, which can be related to the presence of a hot spot in the GaN layer where the temperature overcomes the melting point of the material.

Because of the crucial role covered by the temperature, its accurate simulation becomes of paramount importance. However, the thermal models provided by GaN HEMTs' manufacturers are derived under nominal operating conditions, as, for example, in [15], where the thermal impedance is estimated through 3D finite element simulations considering a

constant power dissipation on the device. Under these hypotheses, the heat transfer mainly involves the surface of the GaN layer, with a nearly homogeneous temperature distribution along the channel. This assumption is not valid during SC, as several works have shown that the power density is mainly concentrated in a small area of the channel, below the gate [9,12,14]. Moreover, the thermal impedance is also dependent on the heat distribution in the volume of the device and, hence, on the dissipated power [16].

In [17], it is shown through experimental measurements on a 650 V/60 A device operating in SC that there is a marked difference between the measured drain current and the one predicted by LTSpice simulations, both in the peak value and in its temperature dependence, and this difference is attributed to the manufacturer's thermal model. In [8,17], the authors try to estimate the hot spot temperature using the real power dissipation profile derived from experimental tests as the input of the SPICE thermal model of commercial devices, but this procedure relies on the fact that the thermal model should be suitable also for SC conditions, that is not assured. This could lead to an incorrect estimation of the temperature reached inside the device and consequent inaccurate assessments on its SC behavior.

In this article, we focus on the thermal dynamics of a 650 V GaN HEMT through two-dimensional finite element simulations, highlighting the differences that appear between constant current switching (CCS) and SC conditions. The results of the simulations are used to obtain an equivalent thermal circuit of a GaN HEMT during SC capable of predicting both the junction temperature T_j, defined as the average temperature in the conduction channel, and the maximum temperature in the device structure. The equivalent thermal circuit is implemented in LTSpice together with the electrical equivalent circuit to obtain a temperature sensitive circuit model of a GaN HEMT in SC. LTSpice circuit simulation results are compared to experimental measurements performed during the SC of 650 V/4 A commercial GaN HEMTs. The proposed model provides results in good agreement with the experimental ones and resolves the inconsistency between the measured drain current in SC and the waveform predicted by circuit simulations based on the manufacturer's model. Furthermore, it is demonstrated that the temperature predicted by the proposed model at the hot spot exceeds the failure limit temperature of GaN devices.

2. Numerical Simulations

The starting point of our analysis involves the study of the thermal behavior of a GaN device under two different operating conditions: constant current switching (CCS) and short circuit (SC). For this purpose, the structure in Figure 1, which schematizes a normally-*off* AlGaN/GaN HEMT cell with a p-type gate and AlGaN Buffer, was simulated with the Synopsys TCAD tool [18].

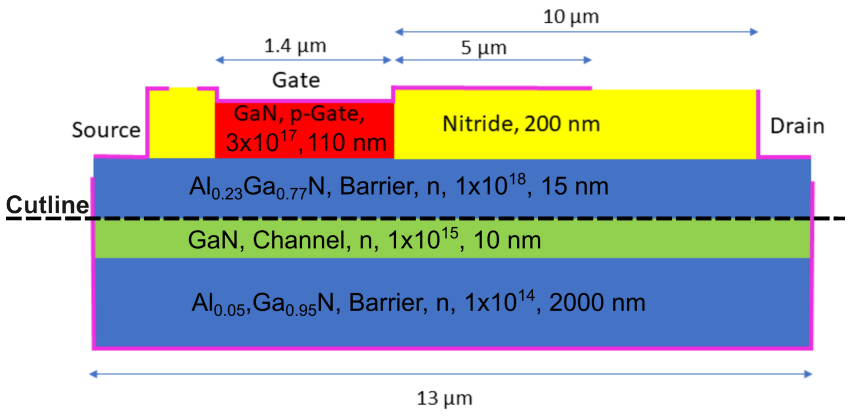


Figure 1. Two-dimensional structure of the GaN HEMT simulated in TCAD.

The structure is based on the one described in [19] and is formed by an $Al_{0.05}Ga_{0.95}N$ buffer layer, a 10 nm GaN channel layer, and a 15 nm $Al_{0.23}Ga_{0.77}N$ barrier layer. The gate

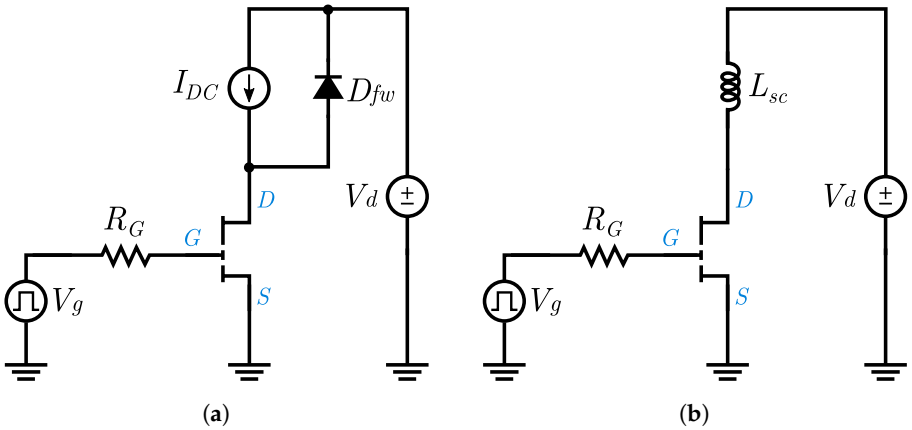
is a 110 nm p-type GaN layer doped with Manganese; its length is 1.4 µm, and field plate of 5 µm is present. A single field plate was used to simplify the simulation even if in practice more field plates are used. This simplification has a very low impact on the results of our analysis, which is more concentrated on the current density that mainly influences the thermal behavior of the device.

The source and drain contacts are defined as Schottky with a metal work function of 4.3 eV, and the gate contact has been realized using the Schottky contact resistance model with the TCAD default values. The entire structure is 13 µm long, and an area factor of about $20 \cdot 10^4$ has been set to obtain an area of about 2.6 mm^2. The buffer contact was defined as both an electrical and a thermal node with a starting temperature of 300 K and by setting a thermal boundary condition with 0.0004 cm^{2}K/W thermal resistance. These parameters were chosen according to [20] in order to simulate a device as similar as possible to a commercial 650-V/4-A GaN HEMT.

The presence of the traps in AlGaN and GaN was considered by introducing traps of donor type at the AlGaN/Nitride interface ($5 \cdot 10^{13}$ cm^{-3} at 0.6 eV from MidGap) and of acceptor type at AlGaN/GaN ($6 \cdot 10^{12}$ cm^{-3} at 0.23 eV from the conduction band), and in the buffer layer ($1 \cdot 10^{15}$ cm^{-3} at 0.45 eV from the conduction band) [19]. The levels and concentrations were chosen to match the subtreshold slope of the I_D–V_g curve and the off-state leakage current.

The following physical models were used: Shockley–Read–Hall recombination, the Masetti mobility model, the Caughey–Thomas model to describe the high-field saturation effects, Fermi–Dirac statistics, and nonlocal band-to-band tunneling.

After carrying out static simulations to verify the structure's breakdown voltage and DC characteristics, the TCAD mixed-mode tool was used to study the behavior of the device inserted into the circuits of Figure 2. The circuits were driven in both cases by connecting a voltage source V_g to the gate through a 10 Ω resistor R_G. Figure 2a shows the circuit used for CCS, where a constant current source I_{DC} and an ideal freewheeling diode D_{fw} are placed at the drain of the device and the voltage source V_d is used to set the drain voltage to 50 V. The hypothesis of using a constant current switching instead of inductive load switching does not affect the considerations on the thermal behavior carried out in the next sections, that is the object of this research. The SC was simulated by realizing the scheme of Figure 2b, where L_{sc} is a 10 nH inductor placed at the drain contact to simulate the parasitic inductance on the DC-link. The low value of V_d guarantees that the device operates with low electrothermal budget, avoiding any critical condition.



(**a**) (**b**)

Figure 2. Scheme of simulated circuits for CCS (**a**) and SC (**b**).

2.1. Constant Current Switching

The constant current switching was simulated applying a pulsed V_g with a period of 2 µs, 50% duty-cycle and 5 V amplitude. The current source I_{DC} supplies 4 A. Figure 3 shows the waveforms at the device terminals during a single period. The gate voltage (in

green) and the drain voltage (divided by 5, in blue) refer to the left axis, while the current waveform (in red) refers to the right.

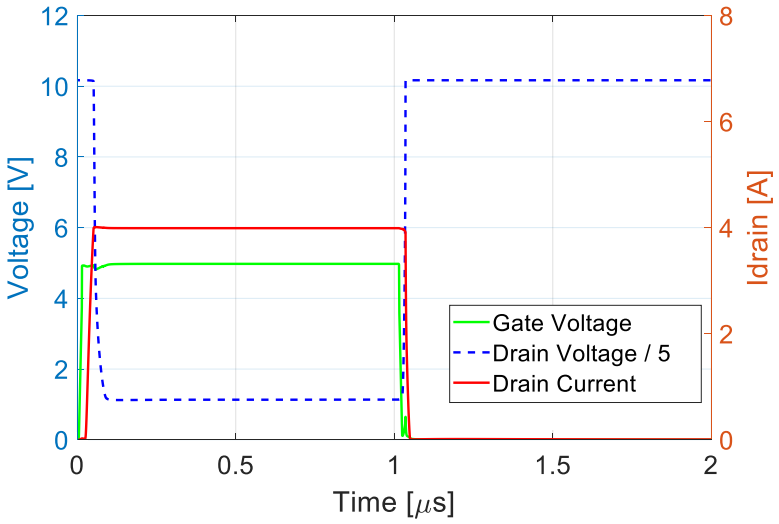


Figure 3. TCAD simulations of the electrical waveforms in CCS during a single switching period.

The instantaneous power dissipation, not reported in the figure, is maximum at the turn-on and turn-off switching transients (200 W at 0.046 µs and 195 W at 1.03 µs, respectively), while it is lower during the conduction (about 30 W). This power translates into heat produced inside the device, whose temperature will increase. The simulator, in addition to the electrical characteristics, provides the time dependence of minimum, average and maximum temperatures inside the device, identified as T_{min}, T_{ave} and T_{max}, respectively, and their graphs are shown in Figure 4. T_{max} (magenta curve) has two peaks corresponding to the maximum power dissipation during the switching, showing an increase of about 30 K at these time instants with respect the initial temperature. However, this increase is located in a small volume of the device, as the average temperature calculated in the entire structure (green curve) remains between 300 and 311 K. The latter value is reached after about 1 µs, when T_{min} also reaches its highest value of 308 K (blue curve). The device returns to the initial thermal conditions after 2 µs.

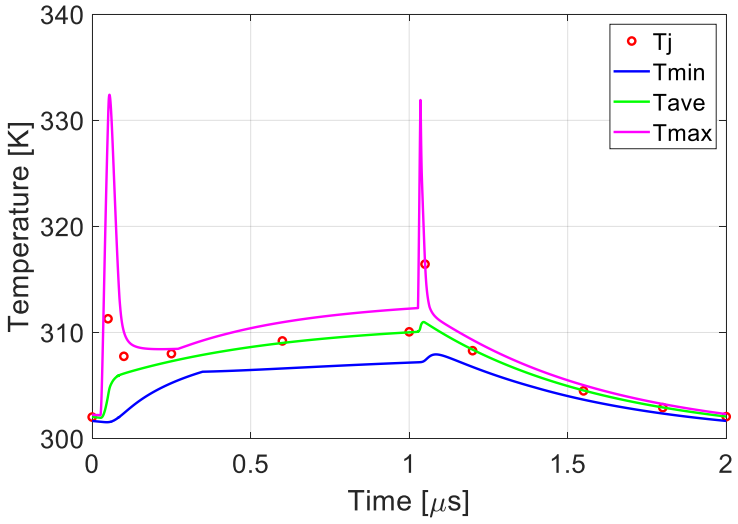


Figure 4. Graph of temperatures (T_{min}, T_{ave}, T_{max}) inside the device provided by TCAD during CCS. The red circles indicate the computed values of T_j.

The curves in Figure 5 obtained automatically by TCAD do not provide important information like the location of possible critical points. A more detailed analysis of TCAD

results is therefore necessary. For this purpose, the 2D spatial temperature distribution provided by TCAD was analyzed starting from the time-domain electrical waveforms of Figure 3. In particular, the one-dimensional temperature distribution was extracted from the 2D distributions along a cut line at the GaN/AlGaN interface where the 2DEG is formed. The obtained one-dimensional temperature profiles are plotted in Figure 5 for the time instants: 0 µs, 0.05 µs, 0.06 µs, 1.05 µs, 1.6 µs, 2 µs. At t = 0 µs, the temperature is fixed at 302 K and is uniform in the channel (blue curve). An increase is observed immediately after the device turn-on (t = 0.05 µs, green curve), with two peaks at the gate's right edge and the field plate's termination. Subsequently, the dissipated power decreases due to the reduction of the drain voltage with consequent temperature reduction (t = 0.06 µs, purple curve). This condition persists up to t = 1.05 µs in correspondence with the device turn-off transient, where the temperature increases (red curve), showing a peak under the gate region. After that, the device starts cooling down (yellow curve) and returns to the initial temperature after 2 µs (light blue curve). For completeness, the inset of Figure 5 reports the 2D lattice temperature distribution in the device at t = 0.05 µs, showing the two hottest regions at the gate's right edge and the field plate's termination. The TCAD simulation results were also used to extract T_j, whose definition requires some attention. In fact, considering the strong variability of the temperature in the structure of the device (see Figure 5), it is necessary to preliminarily say what is meant by junction temperature. It is generally accepted [21] that T_j should be considered as the average temperature of the conduction channel. In fact, important parameters such as the on-resistance of the device, the transconductance and partly the threshold voltage depend on this temperature. We then used the TCAD results to extract the T_j values according to the following procedure: The one-dimensional channel temperature distribution was again extracted from the 2D distributions along a cut line at the GaN/AlGaN interface. T_j was calculated as the average value of this temperature distribution. The results of this post-simulation analysis are reported as red circles in Figure 4. It is seen that the extracted values of T_j overlap reasonably well with the T_{ave} curve except during device commutation, where T_j is approximately 6 K higher than T_{ave}. Therefore, we can say that T_j during CCS is comparable to the average temperature predicted by 2D simulations inside the device.

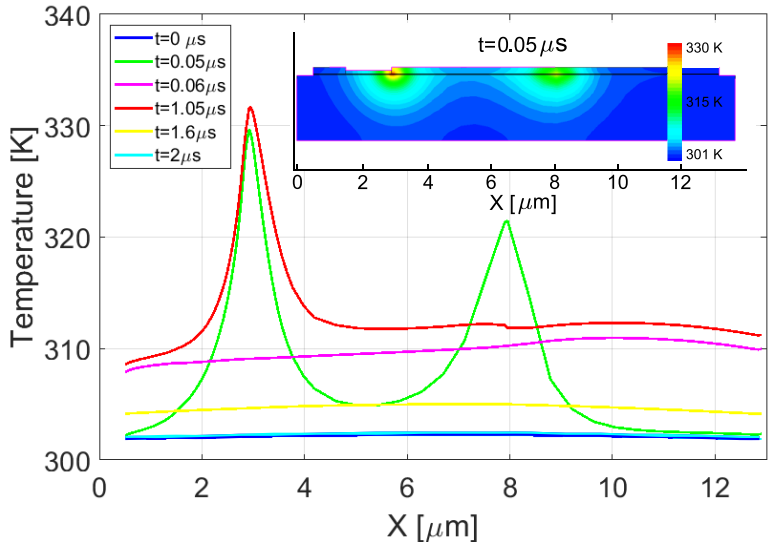


Figure 5. Temperature profile at the GaN/AlGaN interface at different time instants during one switching period extracted from TCAD simulations. In the inset, the temperature distribution at t = 0.05 µs.

2.2. Short Circuit Operation

To simulate a type-I SC condition, described by the circuit of Figure 2b, a pulsed V_g was used with 5 V amplitude and 1 µs duration, with the voltage V_d fixed to 50 V. The

simulated waveforms of the gate voltage (in green), the drain voltage (divided by 10, in blue) and the drain current (in red) are reported in Figure 6. The SC current reaches a peak value of about 8 A and then decreases to 6.4 A, returning to zero when the device is turned off. The instantaneous power dissipation, not reported, has a peak value of 400 W, while its mean value during the gate pulse duration is about 350 W, leading to the increase in temperature, which causes the SC current reduction and the progressive heating of the device.

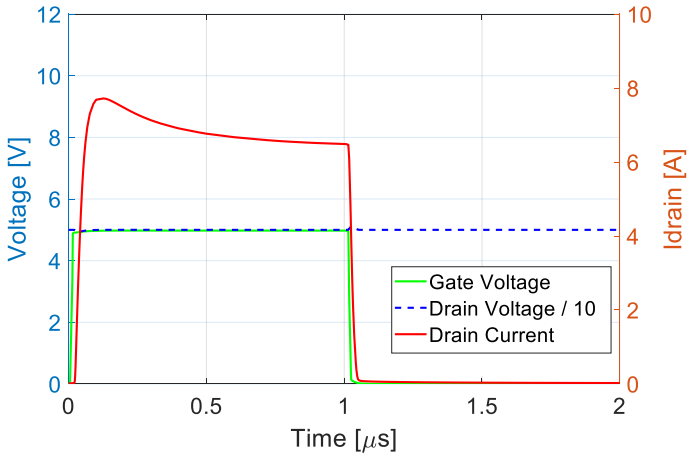


Figure 6. TCAD simulation of the electrical waveforms during the SC.

Figure 7 reports the time evolution of T_{max}, T_{ave}, and T_{min} during the SC, while the red circles represent the temperature T_j extracted with the same procedure described before. These curves appear very different from those in Figure 4. As the involved power is more significant, the temperature is higher in the whole device. The maximum temperature (480 K) is reached inside the device at t = 1 µs and is about 80 K higher than the extracted T_j, which in turn is 50 K higher than the maximum value of T_{ave}. It follows that during the SC, the definition of T_j itself is not consistent as the temperature is strongly not homogeneous along the channel. In fact, the temperature distribution along the GaN/AlGaN interface during the SC, reported in Figure 8, shows that a hot spot is located at the right edge of the gate (x = 2.88 µm), where the temperature reaches the maximum value of 480 K at t = 1 µs (red curve) before decreasing (yellow curve) and returning to the starting value after 2 µs (light blue curve). The inset of Figure 8 shows the 2D temperature distribution at t = 1 µs (the end of the SC), highlighting the presence of the hot spot.

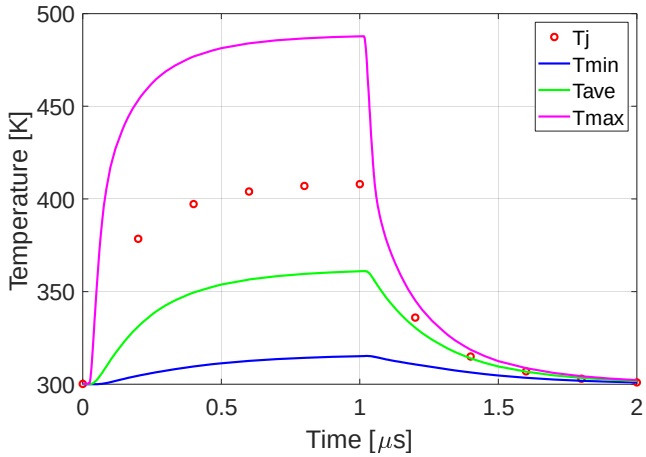


Figure 7. Graph of temperatures (T_{min}, T_{ave}, T_{max}) inside the device provided by TCAD during the SC. The red circles indicate the computed values of T_j.

Figure 8 confirms that the definition of T_j as the mean channel temperature is not appropriate during the SC operation of the GaN HEMT, because of the huge temperature gradient along the channel and the hot spot presence.

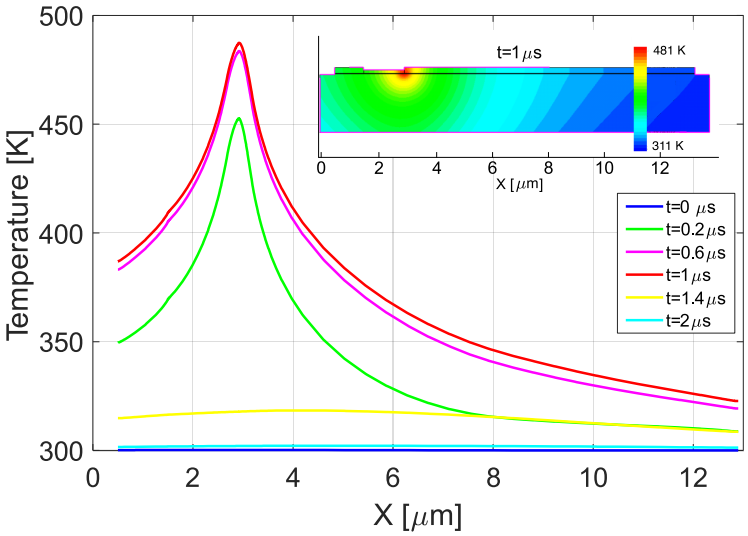


Figure 8. Temperature profile at the GaN/AlGaN interface at different time instants during the SC. In the inset, the temperature distribution for t = 1 µs.

3. Limitations of LTSpice Model for Thermal Analysis during SC

The results of Figures 4 and 7 highlight that the two analyzed operating conditions show completely different thermal responses. The consequence is that when using simulation tools such as LTSpice, they are not able to correctly simulate the channel temperature during the SC. In fact, GaN HEMTs' thermal models used in SPICE-based tools are derived assuming uniform heat distribution along the channel [15,16]. This fact leads to the determination of an equivalent thermal impedance of the device that is valid only during the normal operation of the device, while it deviates from the real behavior when an abnormal operating condition is simulated, as in the case of the SC. As a consequence, although the simulation of a GaN HEMT during SC can be used to obtain an estimation of drain and gate currents [17,22], their temperature dependence is affected by the inaccuracy and the unreliability of the thermal model.

To demonstrate the previous consideration, we compared the TCAD and the LTSpice simulations of a commercial 650-V/4-A GaN HEMT. We used the manufacturer's LTSpice Level 3 model, which includes the Cauer thermal model, to reproduce the device behavior in the same operating conditions as in the previous section: V_g = 5 V, V_d = 50 V.

The LTSpice simulation results of CCS are reported in Figure 9, which shows the drain current (in red) and T_j (in blue). T_j simulated in LTSpice differs from that of TCAD (green circles), also reported in Figure 9, for less than 10 K if we exclude the points related to the maximum dissipated power during the turn-on and turn-off transitions.

Figure 10 shows the simulated waveforms in SC conditions. In this case, a substantial difference in T_j between LTSpice and TCAD simulations can be observed. At the end of the SC, T_j from LTSpice simulation is about 330 K, while it is 410 K from TCAD, with a difference of about 80 K. This happens because LTSpice uses the same thermal model for both CCS and SC conditions, with the only difference in the dissipated power being the input of the thermal network. This fact leads to an error in evaluating the temperature during the SC event. It must be noted that T_j in SC was computed according to the procedure described in Section 2 and does not represent the maximum temperature reached in the hot spot. In this case, the error of the LTSpice simulation would be even higher, equal to about 150 K (compare Figures 7 and 10).

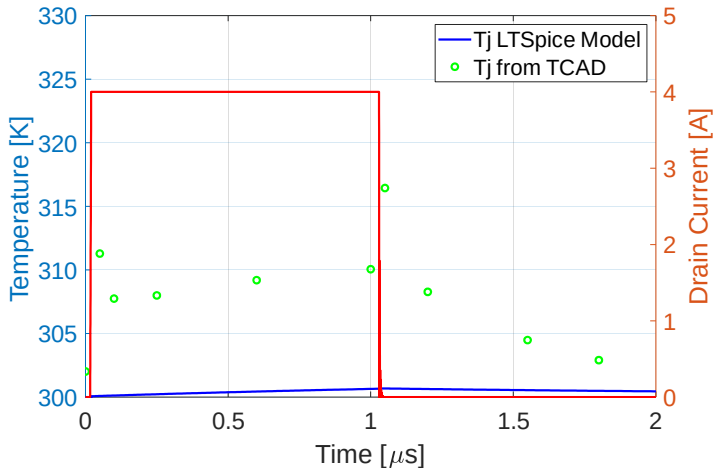


Figure 9. Drain current (in red) and T_j simulated with LTSpice during CCS at V_g = 5 V and V_d = 50 V. The green circles represent T_j extracted from TCAD (see Section 2).

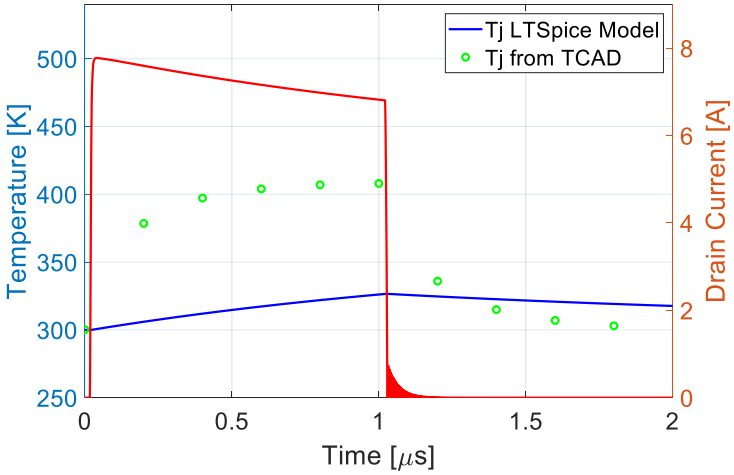


Figure 10. Drain current (in red) and T_j simulated with LTSpice during SC at V_g = 5 V and V_d = 50 V. The green circles represent T_j extracted from TCAD (see Section 2).

In fact, the SPICE model neglects the presence of a hot spot where the temperature (T_{max}) is much higher than the average temperature along the channel. The impact of the hot spot temperature could be potentially dangerous as the drain voltage increases. In fact, as shown in Figure 11, as V_d increases from 50 V to 400 V, the hot spot temperature increases, exceeding 1000 K at V_d = 400 V. The temperature range between 900 K and 1000 K is correlated with the device failure [23–25]. The inset of Figure 11 reports the temperature distribution at t = 1 µs for V_d = 400 V and shows that the hot spot is located at the end of the field plate. As shown in Figure 12, where 2D distribution of the electric field modulus is reported for V_d = 100 V, 200 V, 300 V and 400 V, as the drain voltage increases the effectiveness of the field plate reduces and the maximum of the electric field moves from the right edge of the gate to the field plate's edge, which becomes the most critical point in the structure, as found in [6,13].

The limitations of the LTSpice model to describe the SC behavior of the GaN HEMT could be expected if we consider the hypothesis used to derive the thermal model. The Cauer model describes each layer of the device through an electrical equivalent *RC* network, derived under the assumption of a homogeneous temperature in the channel [15], while TCAD simulations showed a strong spatial distribution of the temperature.

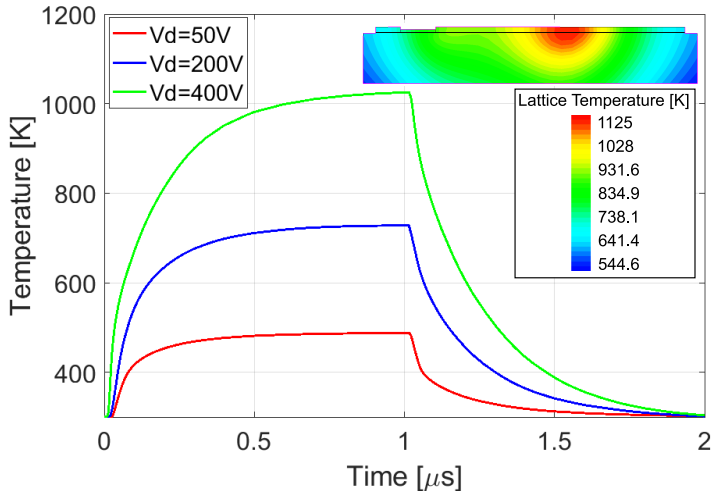


Figure 11. Time evolution of T_{max} during the SC at different drain voltages and V_g = 5 V. The temperature distribution at t = 1 µs and V_d = 400 V is also reported in the inset.

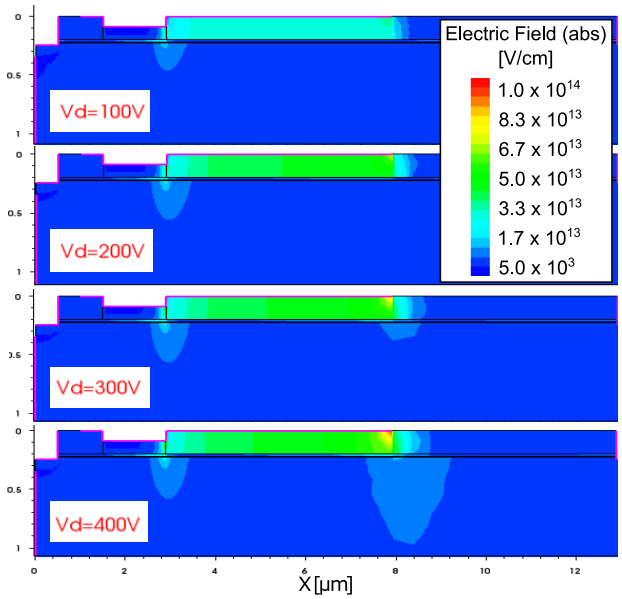


Figure 12. Electric field inside the structure at fixed V_g = 5 V for different values of V_d.

4. Experimental Measurements

From the considerations of Section 3, we should expect that an inaccurate estimate of T_j also affects the LTSpice simulated drain current. To explore this aspect, measurements under type-I SC conditions were carried out on two samples of a commercial 650 V/4 A GaN device [20]. A picture of the experimental setup is shown in Figure 13.

For the experimental tests, we used the same setup described in [13], whose picture is shown in Figure 13. The drain contact of the low-side device was directly short-circuited to the DC-link to replicate the test circuit of Figure 2b. The device was turned on for 1 µs by applying a voltage pulse on the gate with amplitude $V_{GS,on}$ = 5 V through a 10 Ω gate resistor. The drain voltage was varied using as DC-link voltage 50 V, 200 V, and 400 V. The drain current waveforms measured during the tests (solid lines) are reported in Figure 14, compared with those simulated with the Level 3 LTSpice model (dashed lines) with the case temperature set to 300 K.

The experimental waveforms show that at different V_d the peak value of I_D is quite constant, while the temperature increase is responsible of the I_D reduction, which is

more pronounced increasing the drain voltage. The failure of the device after 200 ns at V_d = 400 V indicates that the temperature has reached a critical value. If we compare experimental waveforms with LTSpice simulations, we note that the current peak value is quite well estimated by the model, while significant differences are observed in the time evolution of the current. For low drain voltage (V_d = 50 V), the simulated current is slightly overestimated. Increasing V_d, the reduction in the simulated current is more pronounced than the related experimental curve. In particular, if we consider the case V_d = 400 V, the strong reduction in I_D seems to indicate a huge increase in the device's T_j. This statement is not confirmed by the junction temperature evaluated by the LTSpice model. From the values reported in the inset of Figure 14 we can note that T_j remains below 450 K even at 400 V, while the observed experimental failure of the device suggests an internal temperature much higher.

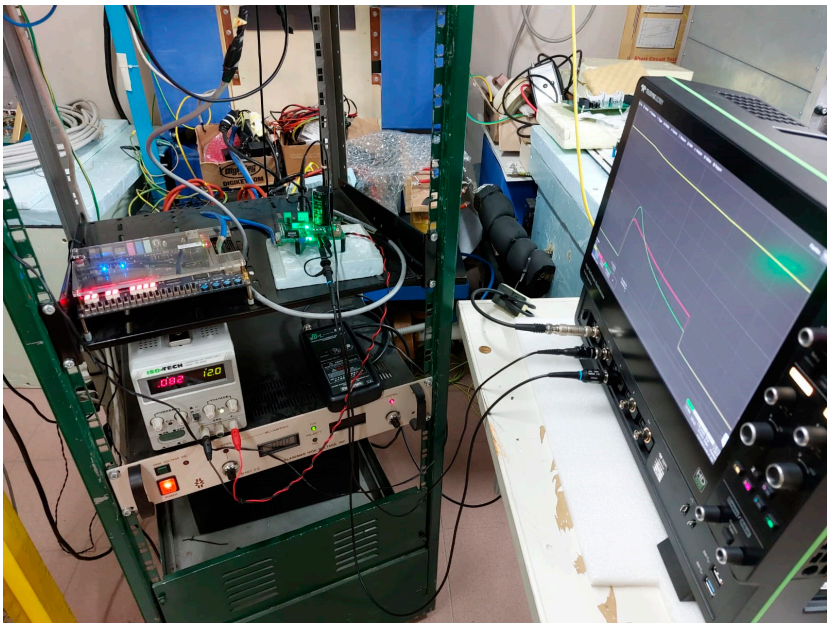


Figure 13. Picture of the experimental setup.

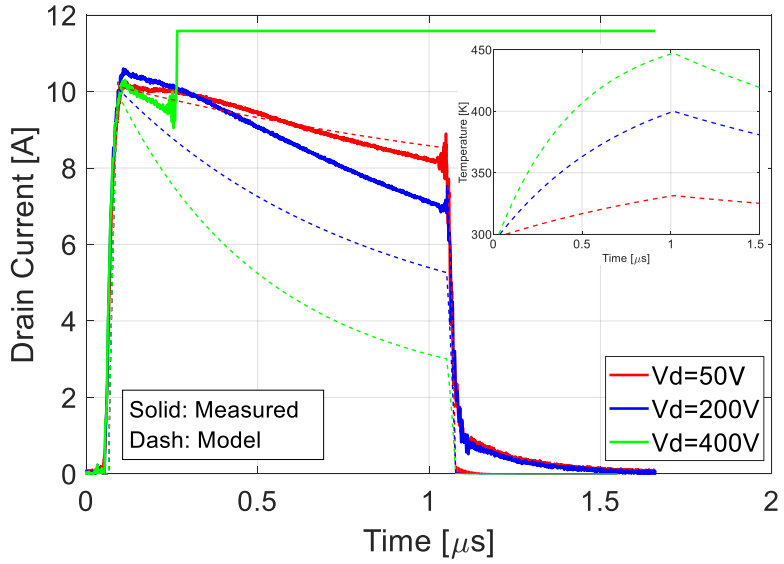


Figure 14. Comparison between the current waveforms measured during the SC (solid lines) and those from LTSpice simulations (dashed lines) at different drain voltages. In the inset, the simulated T_j are also reported.

5. Proposed Model

A comprehensive model for the simulation of the GaN HEMT during SC should provide a correct T_j estimation, necessary to obtain a realistic I_D dependence from the temperature, and an estimation of the hot spot temperature reached inside the device, that affects its robustness.

Based on the results of TCAD simulations in this section we propose a simple thermal model that reproduces the real temperature dependence of I_D and provides the hot spot temperature (T_{max}) inside the device. Due to the fast dynamic of the SC event, the device can be considered an adiabatic system where the heat transfer is strongly constrained in the first layers of the structure, not involving the case and the environment [26]. This consideration allows us to derive a simple thermal model with a single time constant. In fact, under this assumption, T_{max} and T_j curves can be fitted with adequate accuracy for all drain voltages, as reported, for example, in Figure 15 for V_d = 200 V.

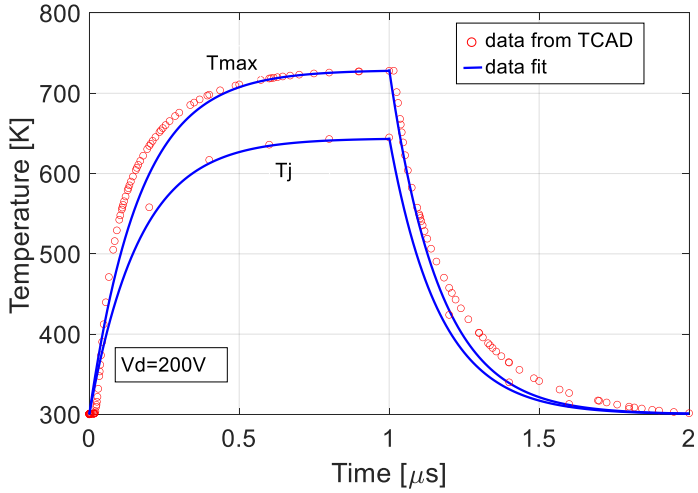


Figure 15. Fitting of T_{max} and T_j using a single-time constant model.

The fitting functions are expressed by (1) and (2) during the SC pulse and during the cooling phase, respectively.

$$T_r(t) = R_\vartheta P_m (1 - e^{-t/R_\vartheta C_\vartheta}) + T_C \quad (1)$$

$$T_f(t) = (T^* - T_C) e^{-(t - t_{SC})/R_\vartheta C_\vartheta} + T_C \quad (2)$$

R_ϑ and C_ϑ are fitting parameters that represent the equivalent thermal resistance and capacitance and they are a function of the applied drain voltage V_d. P_m is the mean power dissipated during the SC pulse and is computed from TCAD simulations. T_C represents the case temperature and T^* is the temperature at the onset of the turn-off after the SC phase, that is t_{SC} = 1 µs in this case.

The fitting procedure was initially applied to T_{max} curves varying V_d from 50 V to 400 V. The extracted values of R_ϑ and C_ϑ are shown in Figure 16 at different V_d. It is worth noting that the thermal time constant $\tau = R_\vartheta C_\vartheta$ remains equal to 167 ns for all voltages.

In the manufacturer's thermal model for CCS, it is possible to relate R_ϑ and C_ϑ to the geometrical and physical parameters of the device, because both the power density distribution and junction temperature are supposed to be uniform along the whole channel. Figure 17 shows that during the SC, the power density has a different space distribution depending on the applied V_d, leading to the dependence of R_ϑ and C_ϑ on this parameter. In particular, C_ϑ becomes larger for higher V_d values, as it is proportional to the volume involved in the heat transfer, which increases with V_d, as depicted in Figure 17. On the other hand, for increasing V_d, the power density distribution involves a larger surface,

reducing the effective length between the heat generation and the substrate, leading to lower values of R_ϑ.

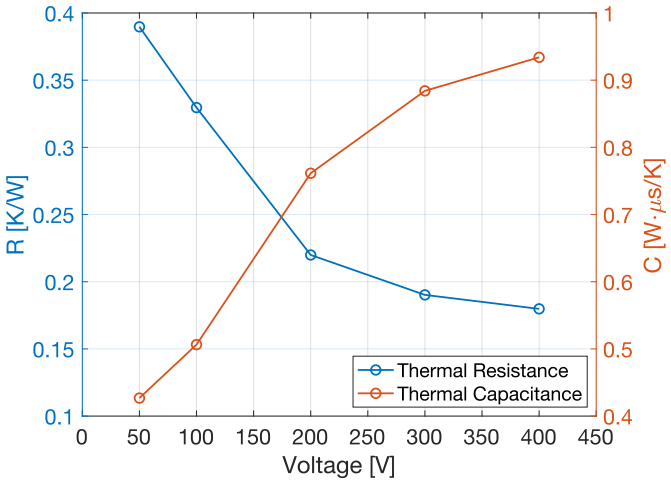


Figure 16. Thermal parameters extracted from fitting of T_{max} as a function of V_d.

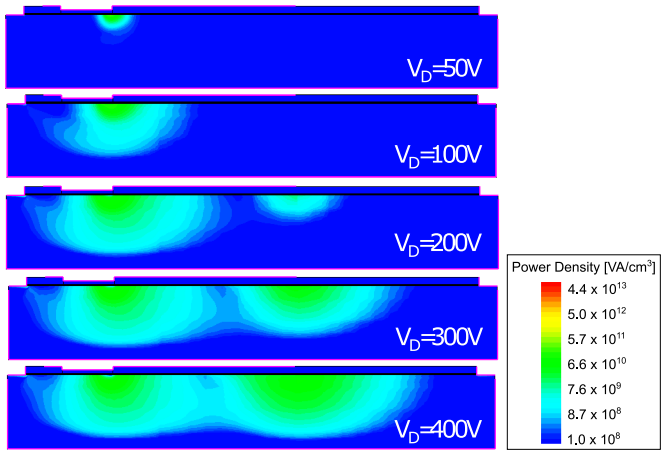


Figure 17. Simulated power density distribution inside the structure for different V_d.

The same procedure was used to estimate R_ϑ and C_ϑ that fit T_j, whose values are reported in Figure 18. In this case, the value of τ is found to be 189 ns for all voltages.

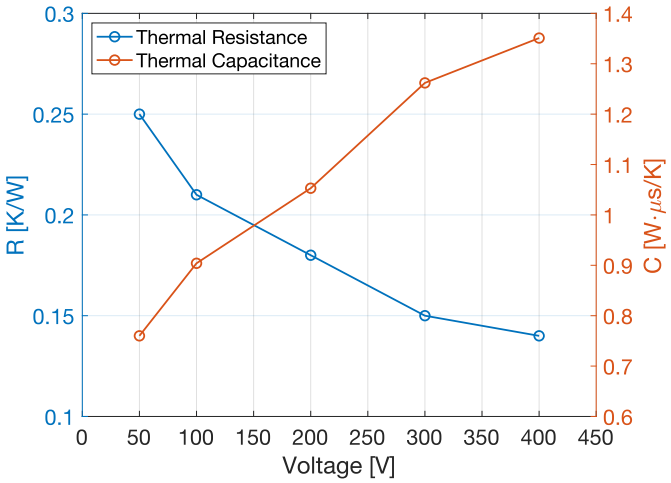


Figure 18. Thermal parameters extracted from fitting of T_j as a function of V_d.

The two networks shown in Figure 19 represent the electrical equivalent circuit described by (1) and (2), which can be used to estimate both T_{max} and T_j during the SC. They have been inserted in the LTSpice model of the GaN device, substituting the manufacturer thermal model. It is worth noting that the electrical parasitic capacitances and resistances were already included in the manufacturer model and they have not been modified. A further thermal pin was added to the subcircuit of the GaN HEMT for the sense of T_{max}, as shown in Figure 19.

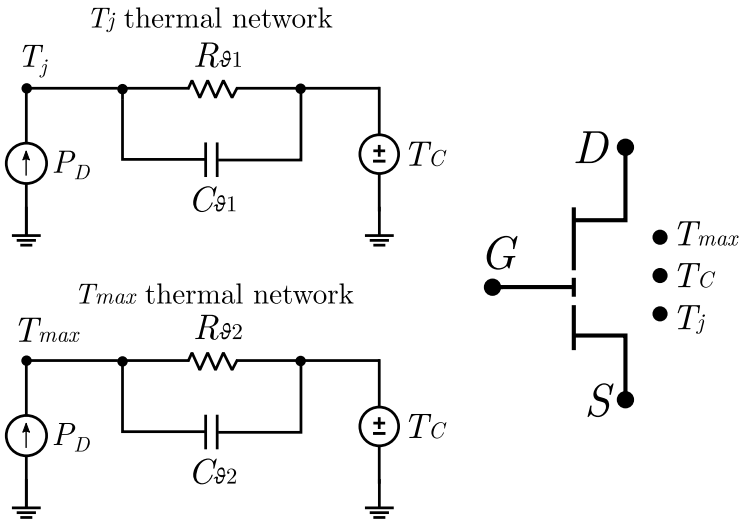


Figure 19. Schematic of the thermal networks and the modified symbol for the GaN HEMT used for the LTSpice simulations.

The thermal networks receive as input the instantaneous power dissipation given by $P_D = V_{DS} I_D$, where I_D is a function of V_{DS}, V_{GS}, and T_j defined by (3), as described in [20,27].

$$I_D = K_1(T_j) \cdot ln(1 + e^{\frac{V_{GS} - b_1}{c_1}}) \cdot f(V_{GS}, V_{DS}) \quad (3)$$

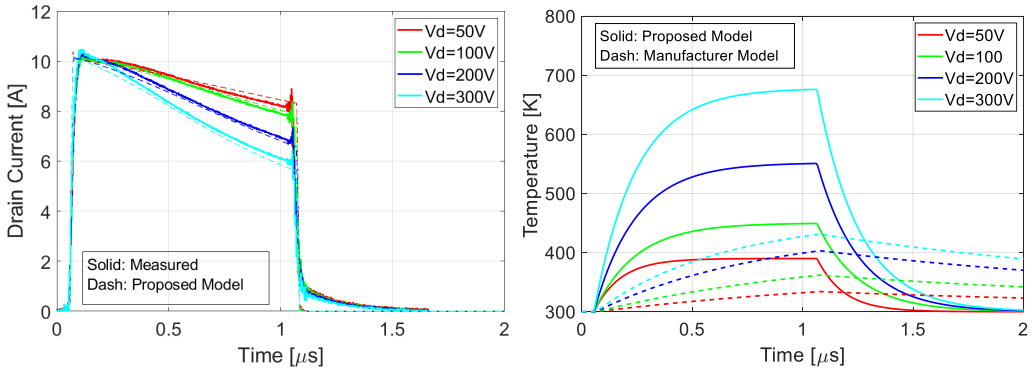
The I_D dependence with T_j, expressed in degrees Celsius, is taken into account through (4), where k_1 is a parameter related to the output and transfer characteristics and l_1 is a fitting parameter taking into account the temperature characteristic.

$$K_1(T_j) = k_1 \cdot [1 - l_1(T_j - 25)] \quad (4)$$

As a first result of the application of the proposed model, we simulated I_D and T_j during the SC for different V_d. In Figure 20a, the simulated I_D waveforms are compared with the experimental ones, showing a valuable improvement of accuracy with respect to the manufacturer model (compared with Figure 14). In Figure 20b, we reported the simulated T_j obtained with the proposed model in comparison with the manufacturer model.

Although T_j simulated with the manufacturer model is much lower compared to the proposed model, its influence on I_D is overestimated, as already highlighted in Figure 14. This observation implies the need to modify the thermal dependence of I_D in (4) by changing the coefficient l_1 from 0.0044 to 0.0013 $°C^{-1}$, while k_1 remains equal to 0.99 A.

Finally, the proposed model provides an estimation of the maximum temperature reached inside the device and gives information about its possible failure. Experimental measurements performed on two samples of the tested device show that the GaN HEMT fails after few hundreds of nanoseconds at V_d = 400 V, as reported in Figure 21. For this voltage value, as highlighted in the inset the estimated T_{max} becomes higher than the failure limit of 900 K measured for the GaN/AlGaN structures [23,25].



(**a**) (**b**)

Figure 20. (**a**) Comparison of measured I_D with proposed model; (**b**) comparison between simulated T_j using manufacturer's and proposed model.

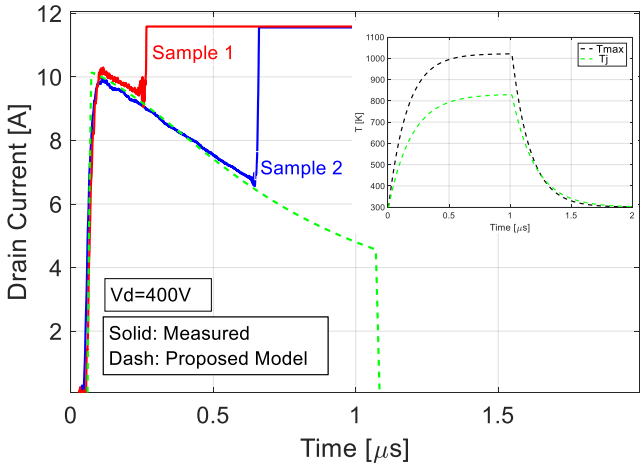


Figure 21. Measured and simulated I_D at V_d = 400 V for two samples. The simulated T_{max} and T_j are plotted in the inset.

6. Conclusions

The GaN HEMT model commonly used in circuit simulators cannot accurately predict the behavior of the device during abnormal operations such as SC. A correct estimation of the junction temperature is necessary to accurately simulate the drain current during the SC, but it is not sufficient to give information about the possible failure of the device, which instead is related to the maximum temperature reached inside the device. Based on TCAD simulations and experimental measurements, we derived two thermal networks to estimate both junction and maximum temperature, which can be included in the device LTSpice model. The proposed model reproduces with good accuracy the experimentally measured drain current of 650 V/4 A GaN HEMTs and the estimated T_{max} justifies the experimentally observed failures.

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