MOS-Gated GTO: a new functionally integrated device suitable for high voltage power applications

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Summary

The aim of this paper is to present the performances of the fully integrated MOS-Gated GTO: a new power device well suited to be applied in the field of high blocking voltages. We start from the characteristics of a fabricated 1.2kV device used to tune the simulator, and we extend the analysis up to 4.5kV blocking voltage. Simulation results are used to understand in detail the physical operations of the device at high values of the blocking voltage and how they compare to the homologous IGBTs. The effects of the lifetime variation are also presented and the trade-off between static and dynamic performances are discussed in detail.

1 Introduction

The thyristor technology is widely used in high power application were the performance of IGBT devices are limited from on-state voltage that became relatively high because of the conductivity modulation of the n- base region is only sustained by the collector junction. In the last years many structures thyristors based, like EST [1], MOSGTO with MOS controlled emitter shorts [2] and MCT [3], have been proposed. Their operation is based on the activation of a main thyristor into their vertical structure for which both anode and cathode junctions contribute to the conductivity modulation. These devices, though, are affected by the presence of parasitic thyristors that can latch up in static and dynamic operations limiting the safe operating area of the device.

Recently the principle of operation of a functionally integrated monolithic MOS-Gated thyristor [4] has been presented as an evolution of the Emitter Switched Bipolar Transistor [5]. This device combines the advantage of a gate turn-off thyristor with an easy MOS gate control without the presence of latching parasitic devices. Similar Emitter Switched Thyristor structures (ETO) were also presented in a discrete form and showed very interesting performances [6, 7].

The objective of this paper is to present the perspective performances of the fully integrated MOS-Gated GTO in the range of high blocking voltages and use the simulator to better understand the behavior of the device. We start from the characteristics of an experimentally fabricated 1.2kV device, that we used also to tune the simulation models, and we extend the analysis up to 4.5kV blocking voltage. The simulated characteristics of high voltage MOS-Gated GTOs with different blocking voltage are compared with those of a first generation IGBTs having the same blocking voltages.

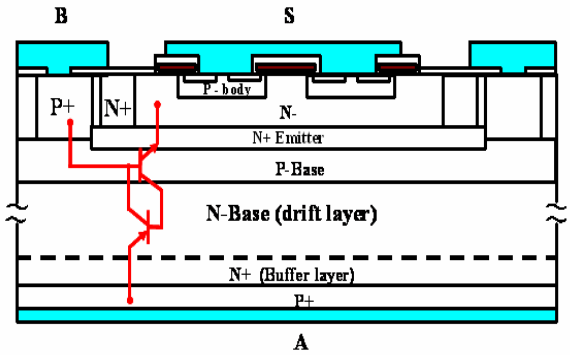

Figure 1 Schematic of the proposed device elementary cell.

2 MOS-Gated GTO Structure

The structure of the MOS-Gated GTO elementary cell is presented in Fig.1. The structure is achieved by integrating low voltage MOS cells inside the cathode region of a high voltage gate turn-off thyristor. This technology is the evolution of the industrialized process used to fabricate ESBT which is already commercially available. The proposed device differs from the previously presented MOS controlled Thyristors structures because at normal operation conditions the activation of the internal parasitic structures involving the external source path is strictly inhibited by the presence of the MOSFET so that they have no impact on the safe operating area of the device.

The equivalent circuit of the device is depicted in Fig.2 that shows the thyristor cathode in series with a N-channel MOSFET. When the MOSFET is on, the device is a thyristor and the current flows from the anode to the cathode as a consequence of regenerative effects

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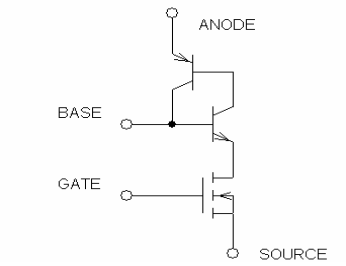

Figure 2 Equivalent circuit of the proposed device

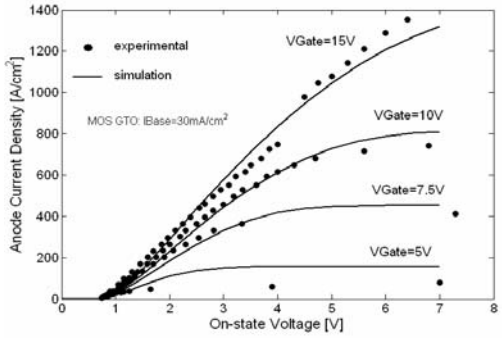

Figure 3 Experimental and simulated forward characteristics of 1.2kV device varying the gate voltage. For the simulated device the N^-drift region lifetimes are fixed to τ_{no}=10us and τ_{po}=3us.

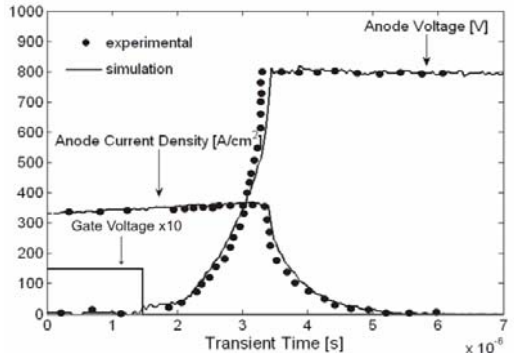

Figure 4 Turn-off waveforms of 1.2kV MOS-GTO.

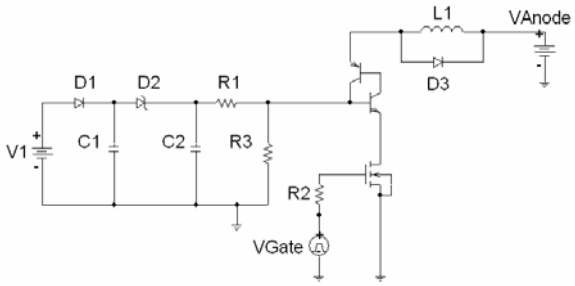

Figure 5 Circuit used for the commutation.

involving NPN and PNP transistors. When the MOSFET is switched off, the cathode current is immediately cut off and the anode current is diverted to the base terminal so that the GTO is turned off at unity reverse current gain [6] thus resulting in a reasonable turn-off time and in a good RBSOA.

With the help of Silvaco finite element TCAD simulator [8] a 1.2kV prototype having an area of about 23mm^2 has been fabricated. The comparison between experimental and simulated characteristics of a 1.2kV device irradiated with 15MRad electron dose, was used to tune the parameters of the simulator in order to have a good accuracy of the simulation as it is shown in Figs.3 and 4 where the forward and inductive switching characteristics are reported of both simulated and experimental results. The circuit used to drive and load the device during the turn-off is shown in Fig.5.

With reference to Fig. 3 we have to outline that the on state device characteristics are very interesting. In fact the device supplies a voltage drop of less than 3V at an anode current density of more than 600A/cm^2 with a very small base current density which is just required to trigger the regenerative effect.

If we focus the attention on the waveforms of Fig. 4 we can see some peculiarities of the MOS-Gated GTO inductive turn-off. In facts after the turn-off of the internal MOSFET, which takes place when its gate voltage is turned to zero, the device experiences a storage phase during which the anode voltage increases and reaches a plateau value which is imposed by the external circuit thus avoiding the possibility for the internal MOSFET to reach its avalanche voltage limit. This plateau value is related to the conduction of the thyristor during the storage phase and to the voltage at the base terminal which is due to the base current flowing through R1, R3 and C2. After the end of the storage phase the anode voltage continues up to the power supply voltage and afterward the turn off is completed by the anode current fall down and the subsequent tailing phase.

A more detailed description of the device internal behavior during the turn off is presented in the following.

3 Predictable characteristics of high voltage MOS-Gated GTO

The perspective performances of the MOS-Gated GTO at increasing blocking voltage are revised in this section. To predict its capabilities, starting from the design of the constructed 1.2kV device, we have adjusted doping and width of the n-base region to achieve simulated structure with desired performances.

For each simulated device (2.5, 3.5 and 4.5kV) we have compared forward and switching characteristics with those of IGBTs having the same $n^-n^+p^+$ vertical structures. The IGBTs used for the comparison correspond to first generation devices having a planar gate structure. Moreover, the parameters used for the simulations are compatible with both the n^-Epi/p+-substrate used for the lower voltage devices and the n--substrate wafers normally employed for the high voltage ones. In particular for all simulated devices we have considered a reference n-drift lifetime of 30μs for electron and 10μs for holes.

The first comparison regards the forward characteristics: Fig. 6 shows that the on-state voltage drop of the IGBT increases with the blocking voltage, whereas

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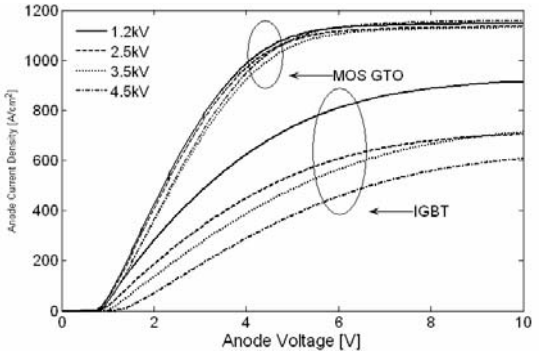

Figure 6 On state characteristics of MOS-Gated GTO and IGBT devices having different blocking voltage at V_G=10V for both devices and I_B=30mA/cm^2 for the MOS-Gated GTO.

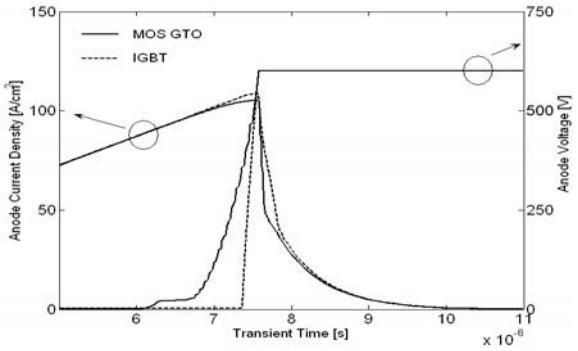

Figure 7 Turn-off waveforms of 1.2kV MOS-GTO and IGBT for a commutated anode current density of about 100A/cm^2.

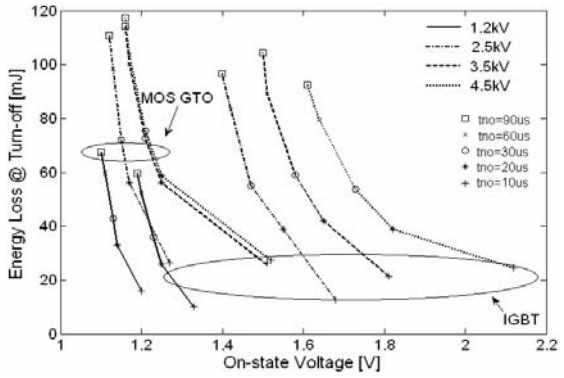

Figure 8 Comparison between trade-off curves of MOS-Gated GTO and IGBT devices with different blocking voltage at J_A=100A/cm^2.

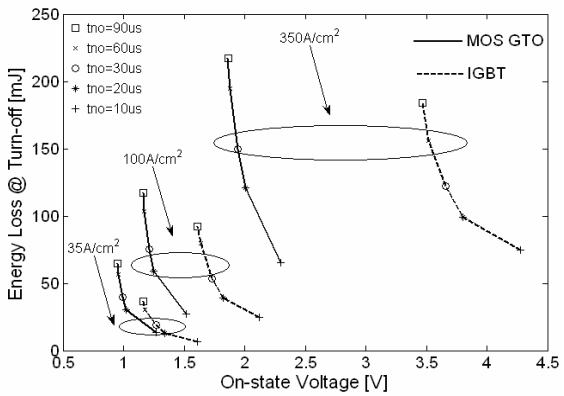

Figure 9 Comparison of trade-off curves for 4.5kV

the MOS-Gated GTO exhibits characteristics almost independent of the variation of the base physical parameters thanks to the activation of the thyristor that permits a much more effective conductivity modulation of the n^- base region. Fig. 6 shows that the on state performances of the MOS-Gated GTO becomes more attractive with respect to those of the corresponding IGBT at increasing value of the blocking voltage. At 100 A/cm^2 there is a factor of about two between the voltage drops of the two 4.5kV devices.

Fig. 7 reports a comparison between the turn off waveforms for 1.2kV MOS-Gated GTO and IGBT. The MOS-Gated GTO exhibits a plateau in the anode voltage not present in the IGBT waveform. Moreover, due to the higher charge stored in its base the MOS-Gated GTO turn-off is slower than the IGBT both during the voltage rise and the current fall thus partly reducing the advantages related to its lower on state voltage drop.

A better comparison between the performances of the two devices can be achieved putting together the static and switching characteristics of the two devices in trade-off curves. To do that we have simulated the turn-off commutations of the 1.2kV up to 4.5kV MOS-Gated GTOs and IGBTs. Fig. 8 reports the simulated energy loss at the turn-off for devices having 1cm^2 area, as function of on-state voltage. The curves were obtained at J_A=100A/cm^2, where J_A is the output current density taken immediately before the current fall. Each point is obtained varying the minority carriers lifetime of the n-region tno and taking tpo=tno/3.

The comparison is always favorable to the MOS-Gated GTO and becomes better at increasing blocking voltage. The advantages arising from the use of the MOS-Gated GTO for high voltage applications are more evident at increasing anode current densities as it is shown in Fig. 9 where the trade-off curves are reported for 4.5kV devices at different J_A, namely 35,100 and 350A/cm^2.

It worth noting that the IGBTs used for the comparison are not optimized and correspond to the first generation devices. The comparison refers to the performances of the newly proposed device with those of an IGBT at the same stage of development in consideration that practically all technological improvements achieved on the IGBT can be also exported to the MOS-Gated GTO. For this, results of the following analysis can give useful highlights about the capability of the proposed device.

4 Physical operation

Let us focus our attention on the 4.5kV turn-off to better understand the different performances of the two devices and highlight the physical behavior of the presented device.

The current densities and the gate voltages waveforms during the inductive turn-off are reported in Fig.10 a) and b) for 4.5kV MOS-Gated GTO and IGBT, respectively.

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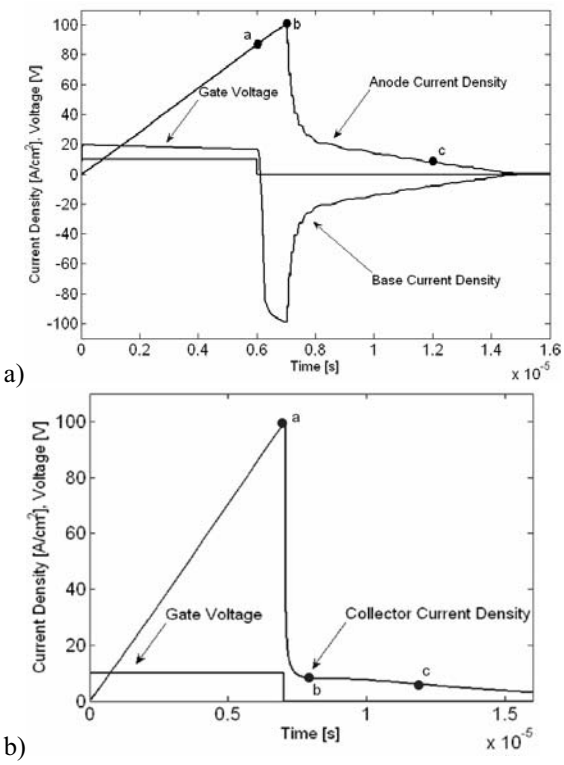

Figure 10 Current density and gate voltage waveforms during the 4.5kV of MOS-Gated GTO (a) and IGBT (b) turn-off.

Table 1

	Von(V)	Eoff (mJ/cm^2)
MOS-Gated GTO	1.25	75.47
IGBT	2.25	53.97

For both analyzed devices the electrons and holes lifetimes were set to tno=30μs and tpo=10μs, respectively. The waveforms of the output voltage, not reported in the figure, have the same shape of the ones of Fig. 7. The current waveforms of the MOS-Gated GTO show that during the storage phase the base current becomes negative and equal to the anode current. Base and anode currents remain equal during the whole duration of the current fall thus evidencing that the turn-off of the internal GTO takes place at a unity forced reverse gain [6]. The comparison between the two devices show for both of them a rapid initial fall followed by a slower tailing. The current tail of the MOS-Gated GTO starts from a higher value but it has a faster reduction to zero with respect to the IGBT tail. As it will become more clear from the analysis of the simulation results, this behavior is due to the fact that the reduction of the higher charge stored in the low doped region of the MOS-Gated GTO, is not left only to the carriers lifetime but it is assisted by the base current flow. The value of the on-state voltages and the energy losses extracted from the waveforms of Fig. 10 are summarized in Table 1.

To get some physical insights in the comparison between the switching operations of the 4.5kV high voltage MOS-Gated GTO and IGBT, we report in Figs. 11 and 12 the doping profiles and the carriers concentrations along the $n^-n^+p^+$ region. For both figures the surface and the bottom of the vertical structure are on the left and right sides, respectively. The cut line corresponds to the center of the base contact with the zero abscissa coincident with the edge between the P-base and the P+ contact for the MOS-Gated GTO (see Fig. 1). Instead the cut line refers to the center of surface MOSFET neck for the IGBT. The instant which figures a), b) and c) refers to correspond to the time instants marked with a, b and c in Fig. 10, respectively. They correspond to the end of the conduction phase, the end of the storage phase for the MOS-Gated GTO and a significant point of the current tail respectively.

Fig.11 a) and 12 a) refer to the end of the conduction phase for both devices and clearly show the benefit of the regenerative effect which regulates the MOS-Gated GTO operation. In facts the carriers concentration in n-base is sustained by the injection from both the cathode and the anode regions. For the IGBT the carriers injection comes only from the collector and the conductivity modulation of the n-base results less effective thus justifying the larger on-state voltage drop exhibited by the IGBT.

Fig.11 b) refers to the end of storage phase in the MOS-Gated GTO device. For the sake of comparison Fig. 12 b) reports the carriers distribution in similar conditions in the IGBT. For both devices a dynamic space charge region develops across the n-base top junction. In the MOS-Gated GTO the residual charge is larger than the IGBT one but a significant holes flow is extracted from the base contact as a consequence of the external base current. It induces in the space charge region a holes population larger than that in the IGBT thus explaining the faster reduction of the tail in the anode current exhibited by the MOS-Gated GTO.

Figs.11 c) and 12 c) refer both to the instant t=12us. The residual charge in the MOS-Gated GTO is much lower than the IGBT one taken at the same instant. It is worth noting that the minority carriers lifetime used in the simulation is tp0=10μs for both devices. The slower carriers removal of the IGBT can be explained by considering that its turn-off is the open base turn-off of the PNP BJT where the stored charge is removed only thanks to the carriers recombination associated to the n-base and to the highly doped terminal regions, namely the body of the surface MOSFET and the collector regions [9].

The consequence of the above considerations is that the turn-off energy losses of the IGBT are only 28% lower than those ones of the MOS-Gated GTO whereas the IGBT on state voltage drop is 80% larger as reported in Table 1. Moreover, the simulation results explain why the trade-off curves presented in the previous section are favorable to the MOS-Gated GTO particularly at high blocking voltages.

5 Conclusion

We have presented experimental and simulated static and dynamic characteristics of a 1.2kV MOS-GTO. Starting from this design, we have simulated the performances of higher blocking voltage devices and we

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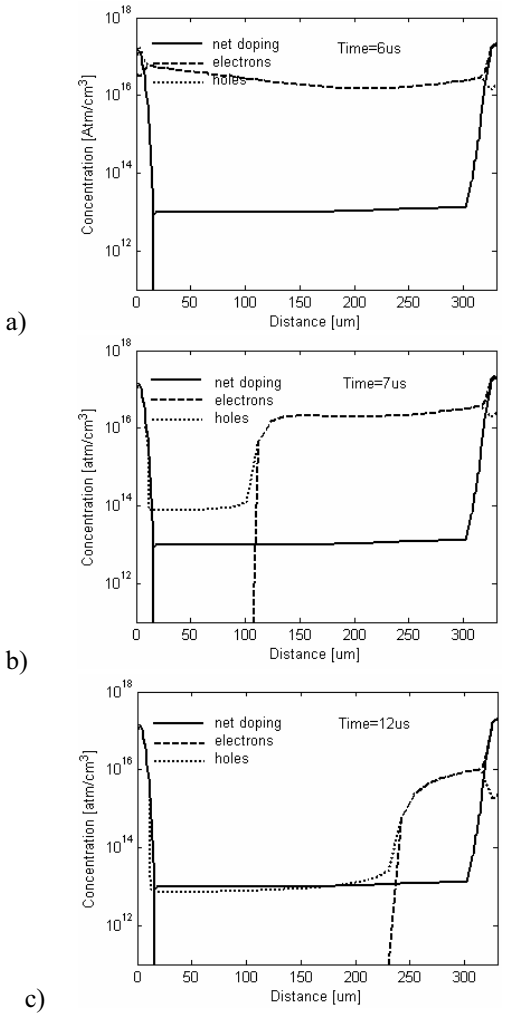

Figure 11 Doping and carriers profiles in MOS-Gated GTO during the turn off at different instants.

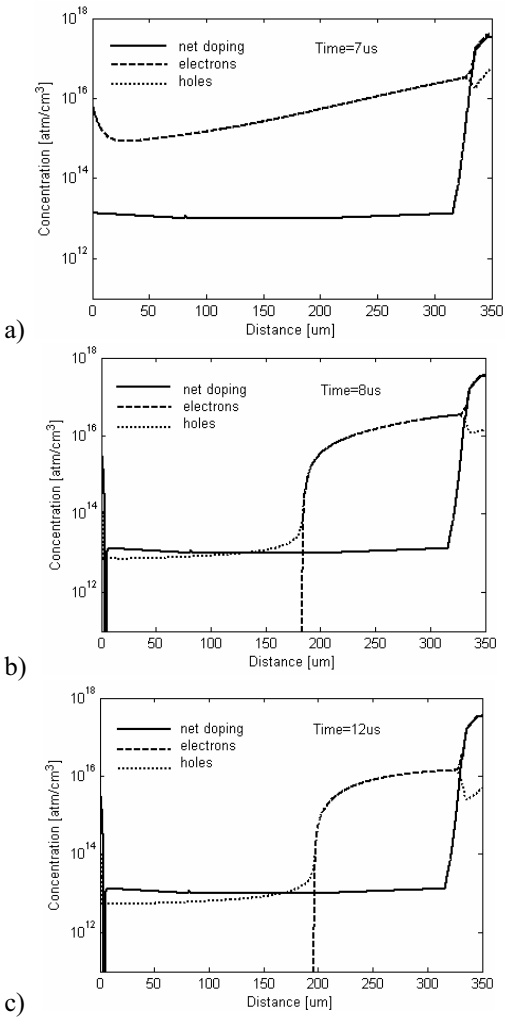

Figure 12 Doping and carriers profiles in IGBT during the turn off at different instants.

have compared them with those ones of corresponding first generation IGBT. Simulation results indicate that even if the switching performances of the MOS-Gated GTO are lightly worse than the related IGBT its much better on state characteristics make the trade-off curves favorable to the proposed devices that can be considered to be a good competitor of IGBT devices particularly for high voltage applications.

6 Literature

[1] M.S. Shekar, B.J. Baliga, M. Nandakumat, S.Tandon, A.Reisman, “A new MOS-Gated power thyristor structure with turn-off achieved by controlling the base resistance”, IEEE Electron Devices Letters, vol.2, no.5, May 1991.

[2] M. Stoisiek, H. Strack, "MOS-GTO - A Turn-Off Thyristor with MOS-Controlled Emitter Shorts", Proc. of IEDM 1985, pp. 158-161, (1985)

[3] V.A.K. Temple, ”MOS-Controlled thyristor – A new class of power devices”, IEEE Transaction on Electron Devices, vol.33, no.10, 1986, pp. 1609-1618.

[4] C. Ronsisvalle, V. Enea, G, Belverde, ”A novel MOS-Gated thyristor 4-terminal device particularly suited for high-current and high-frequency applications”, 9th International Seminar on Power Semiconductor, Prague 2008.

[5] C.Ronsisvalle, V.Enea: “The ESBT: a new monolithic power actuator technology devoted to high voltage and high frequency applications”, Proc. of CIPS’08, pp. 379-383, Nuremberg, 2008.

[6] B.Chen, A. Q. Huang, M. Baran, C. Han, W. Song: “Operation characteristics of emitter turn-off thyristor (ETO) for solid-state circuit breaker and fault current limiter”, 21st IEEE Applied Power Electronics Conference and Exposition, 2006, APEC '06, pp. 174-178.

[7] B. Zhang; A.Q. Huang, L.Yunfeng, S. Atcitty, ”Performance of the new generation emitter turn-off (ETO) thyristor”, 37th Industry Applications Conferen IAS Annual Meeting. Volume 1, 13-18 Oct. 2002 pp. 559-563.

[8] Silvaco “ATLAS User's Manual.”, Silvaco, Santa Clara, California, USA.

[9] B. J. Baliga, “Fundamentals of Power Semiconductor Devices”, Technology & Engineering, 2008.

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