A Simple and Accurate Software Technique for the Dynamic Measurement of the Current in Fast Switching Devices using a Resistive Shunt

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***Abstract*—A series resistive shunt, also called Current Viewing Resistor, CVR, is one of the simplest and most commonly used methods for measuring the current flowing through an electronic device. However, the non-ideality of the shunt resistors creates several measurement problems, particularly when the devices undergo high-speed switching, as in wide-bandgap devices. In this case, the parasitic inductance associated with the CVR causes an overvoltage, which affects the current estimation during the initial stages of the transients, when the current gradient can become very large. To solve this problem, two types of solutions have been proposed in the literature. The first, which is hardware-based, is oriented both to reducing the shunt's parasitic inductance and to compensating it by adding external circuits that cancel its effect on the voltage signal measured across the CVR. For these hardware solutions, techniques are used to cancel the magnetic field produced by the shunt, and, therefore, axial resistors with parallel windings, printed resistance sheets, or coaxial shunts are used, which lead to an increase in both the complexity of the layout and the cost of the circuit, making them unsuitable for PCB integration and large-scale production. In the second type of solution, the signal measured on the CVR in the presence of stray inductance is fed into software procedures that enable an accurate, wide-bandwidth current measurement. The current extraction software techniques presented in the literature so far require very sophisticated calculations and mathematical procedures, and are suitable only for offline analysis of experimental characterization, such as double-pulse measurements. The procedure proposed in this paper falls within the scope of software procedures and is based on a simple technique that uses the implicit solution of the circuit equations to extract the current from the dynamic measurement of the voltage drop across the CVR. Only the leakage inductance is used as a parameter that can be measured directly on the circuit. It is shown that the proposed procedure exploits the advantages of a cheap, easy-to-manufacture sensor, enabling accurate, wide-bandwidth current measurement even on high-speed devices. The method is experimentally validated, and the results are compared with those obtained by a commercial Rogowski coil and a coaxial shunt.**

***Index Terms*—Power devices, Current measurement, Wide-band-gap semiconductors, GaN HEMT.**

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I. Introduction

ACCURATE current measurement in power electronic circuits has always been a particularly sensitive problem, since current measurement is necessary to implement various functions such as control, determining the performance of electronic converters in terms of conversion efficiency, and, above all, measuring the power dissipated in power semiconductor devices during the conduction and switching phases. The advent of power devices made of wideband semiconductors (WBG), such as silicon carbide (SiC) and gallium nitride (GaN) [1], [2], has further aggravated the problem due to their very high switching speed, which requires a strong broadening of the current measurement bandwidth [3]

Traditional measurement methods based on the use of Hall effect sensors (Current Clamp), Rogowski coils or Pearson sensors [4], are poorly suited to current measurement in very fast switching devices, due to several reasons including the fact that their use involves modifications to the circuit and the consequent introduction of intolerable parasitic inductance that affect the performance of the switching converter in terms of dissipated power and electromagnetic compatibility [5]. Furthermore, the cost and size of these sensors make them unsuitable for in-circuit integration and use in industrial applications.

The sensors that seem most suitable for measuring current in WBG devices are Current Viewing Resistors (CVR) [6]. In fact, they allow :

a) Very high bandwidth and high linearity in double pulse dynamic characterization of power devices;

b) Small insertion impedance, small size, and overcurrent ruggedness in the integrated current measurement and overcurrent detection;

c) High bandwidth, low cost, and high reliability in EMI detection and in converter current measurement.

The main difficulty in using CVRs is their parasitic inductance, which causes high overvoltage on the signal being measured, especially when switching is very fast and generates high current gradients [6].

A first solution to this problem is the CVR coaxial shunt [7], [8], whose coaxial structure almost completely eliminates the inductance of the measurement circuit, enabling the commercial availability of CVR coaxial shunts with a declared bandwidth of 400 MHz - 2 GHz. It is worth noting, however,

that the authors of [8] measured a maximum bandwidth of 150 MHz on commercial 2 GHz CVR coaxial shunts. Moreover, parasitic inductance and capacitance in the coaxial shunt were shown to affect current measurement, and a software procedure is requested to compensate for their effects [9]. In addition, commercially available CVR coaxial shunts are expensive, quite large, and introduce a relatively high parasitic insertion inductance [6]. This last drawback discourages their use and in-circuit integration in applications that employ high-speed WBG power devices. To reduce the parasitic insertion inductance, coaxial shunt resistors made of low-cost SMD resistors [10], [11] were developed, and insertion inductances as low as 0.60 nH were achieved in [11]. However, integrating the CVR coaxial shunt on a PCB requires a rather sophisticated arrangement of connections and vertical mounting of the shunt resistors on the PCB, which can have a significant impact on its thickness and cost [11].

For the above reasons, CVRs made with SMD low-inductance resistors remain the cheapest and easiest-to-use solution. However, the parasitic inductance of these sensors can significantly influence not only the dynamic detection of very fast switching currents but also the device-under-test's behavior, introducing unwanted oscillations in the measured waveforms [12].

To solve this problem, three approaches are reported in the literature:

a) Minimize the parasitic inductance to minimize its effect on the current measurement. For this purpose, several low-inductance SMD resistors are connected in parallel [11], [13], [14], thereby keeping parasitic inductance very low. A value of less than 0.1 nH was achieved in [14]. In these works, typically, the effects of parasitic inductance are not corrected, and the obtained current waveforms are affected by its contribution. In [15], the obtained switching losses were still considered useful as they represent an overestimate of the actual losses. Furthermore, the proposed solutions require large areas on the PCB and are impractical for industrial applications.

b) Introduce reactive networks into the measuring circuit to compensate for the effects of the CVR inductance. In particular, a network comprising inductive [15], [16] or capacitive [17] components is inserted into the circuit in such a way as to obtain the voltage measured at its output terminals proportional to the current but purified from the contribution of the parasitic inductance. The use of these hardware compensation techniques is impractical in a real circuit because it requires modification of the circuit and the insertion of bulky and expensive components, whose non-idealities could limit the measurement bandwidth [16]. In the case of a capacitive network, the compensation capacitor could resonate with the parasitic inductance of the circuit, inducing unwanted high-frequency oscillations in the output power circuit [17].

c) Perform mathematical processing on the signal measured on the CVR, including the contribution of the parasitic inductance, to accurately estimate the current. In a first paper [18], the equation involving the measured voltage, stray inductance, and current was numerically integrated, but the authors had to extract the initial conditions from a low-frequency current measurement. The parasitic parameters of the track between the source and the ground were also used in [19] to extract the current. In addition to the track's self-inductance, the authors also considered its parasitic resistance and mutual inductance, which they extracted using the finite element analysis software Ansys Q3D Extractor. Then, they used a detailed Fourier series expansion applied to the voltage measured on the track to derive the current waveform. Prior to this analysis, the authors used a denoising procedure to remove low-voltage noise from the track's parasitic resistance directly associated with the current to be measured. The procedure used in [19] is very similar to that in [20] for extracting the current from the voltage measured on a pick-up coil placed on the track between the DUT's source and ground.

The results obtained in [18], [19], and [20] are very good, but the procedure to obtain them is rather cumbersome, difficult to implement, and practically impossible to use for real-time measurement of the current in a circuit.

This paper falls under the last c) typology and presents a software technique to extract the drain current by processing the voltage measured across a CVR made of low-inductance SMD resistors placed between the DUT source and ground, including the stray inductance contribution. The main contributions related to the proposed technique consist of the computational simplicity, real-time feasibility, absence of circuit modification, and minimal parameter extraction. Our measurement technique starts from the idea that the effect of parasitic inductance can be compensated via software by referring to a virtual circuit in which a compensation inductance is inserted as is done in the hardware compensation technique [15], [16]. It is demonstrated that the implicit solution of this virtual circuit represents a very practical way to solve the differential equation involving the voltage measured on the CVR [19]. For the real-time implementation, the virtual circuit simplifies to a single difference equation that can be easily embedded into standard digital microcontrollers or FPGAs. Furthermore, the proposed technique does not require introducing additional hardware into the circuit, overcoming the limitations of hardware-based technique, such as additional insertion inductance, components non-idealities, and unwanted resonances. The only parameters required by the proposed technique, namely the shunt resistance and its parasitic inductance, can be measured directly on the physical sensor arrangement without complex tracking software overhead.

The method is validated both experimentally and by circuit simulations, used to supply a systematic evaluation of how hardware-constrained digitization parameters (sampling rate and ADC quantization bit-depth) impact measurement accuracy, and establish a definitive mathematical guideline that allows design engineers to properly size and select cost-effective commercial components (e.g., ADCs, FPGAs) to achieve the target real-time bandwidth. Ultimately, the core contribution lies in demonstrating that combining an ultra-low-cost, standard, easy-to-manufacture SMD layout with a virtual software compensation can match or outperform premium hardware sensors without any of their physical or cost penalties.

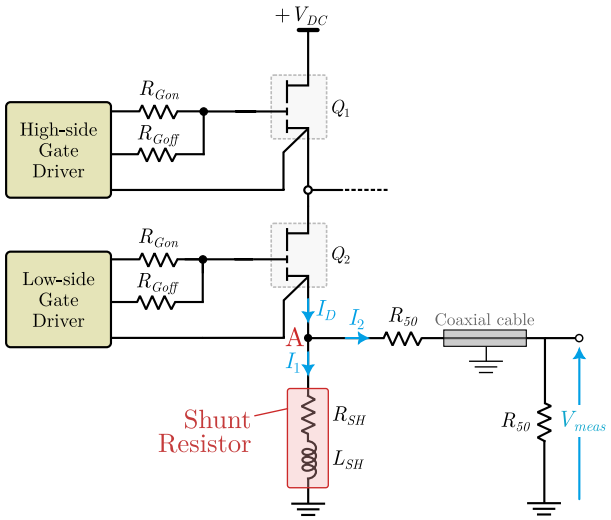

Fig. 1: Generic scheme of a half-bridge circuit where a shunt resistor is used to measure the current I_D flowing in the low-side power device Q_2.

II. The Measurement Procedure and its Software Implementation

A. Numerical extraction of the current from the voltage measured on the shunt

Fig. 1 shows a half-bridge circuit, which is commonly used as the core element of many DC/DC and DC/AC power converters, as well as for the characterization of a power device through double pulse test (DPT) or short-circuit (SC) test. The drain current I_D can be measured by applying a wide-bandwidth, high-resolution acquisition system to the shunt voltage drop. To avoid the problems associated with the parasitic elements of the probe [15], it is convenient to connect an additional 50 Ω resistor in series to the 50 Ω coaxial cable to match the impedance of the measurement network with the 50 Ω input resistance of the oscilloscope.

In the ideal condition of a purely resistive shunt, the proportionality relationship between the measured voltage V_{meas} and the drain current I_D can be written as:

$$V_{meas} = \frac{R_{sh}R_{50}}{R_{sh}+2R_{50}} \cdot I_D = R^* \cdot I_D \tag{1}$$

where $R^* = R_{sh}R_{50}/(R_{sh}+2R_{50})$.

In an actual circuit, (1) is valid only in steady-state conditions because of the stray inductance L_{sh} of the shunt, and the relationship between V_{meas} and I_1 becomes:

$$2V_{meas} = R_{sh}I_1 + L_{sh}\frac{dI_1}{dt} \tag{2}$$

The extraction of I_D from (2) poses several problems which require the sophisticated solutions implemented in [18]–[20].

Here we propose to extract the current $I_D(t)$ from the measurement of V_{meas} by solving (3), which represents the time-domain system equations related to the measurement loop of Fig. 1 and is the integral form of (2). The system (3) can be solved by implementing the Simulink model depicted in Fig. 2 once the values of R_{sh} and L_{sh} are known and using a

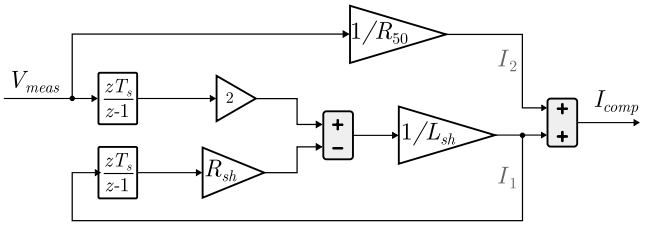

Fig. 2: Simulink implementation of the time-domain equations for the extraction of I_D from the acquisition of V_{meas}.

numerical integration method, e.g. the Backward Euler, using the sampling time T_s of the acquired signal V_{meas}. In the latter case, the difference equation (4) can be derived from (3) and directly implemented on a digital microcontroller for real-time measurement. In (4), y_v^{k-1} and y_i^{k-1} represent the integral of V_{meas} and I_1, respectively, at the previous iteration, used to compute the value of I_D at the current iteration k.

$$\begin{cases} I_1(t) = \dfrac{1}{L_{sh}}\left(2\displaystyle\int V_{meas}(t)dt - R_{sh}\int I_1(t)dt\right) \\ I_2(t) = \dfrac{V_{meas}(t)}{R_{50}} \\ I_D(t) = I_1(t) + I_2(t) \end{cases} \tag{3}$$

$$I_D^k = \frac{2(V_{meas}^k T_s + y_v^{k-1}) - R_{sh}y_i^{k-1}}{L_{sh}+R_{sh}T_s} + \frac{V_{meas}^k}{R_{50}} \tag{4}$$

Current extraction can be greatly simplified if we consider the results of [16], where we have shown that inserting an appropriately sized inductor L_c in the measuring branch compensates for the dynamic effects of L_{sh} and (1) can be directly used to extract I_D under any operating condition. Referring to Fig. 3(a), the network consisting of the 50 Ω resistors and the inductor L_c introduces a single pole in the transfer function between V_{meas} and I_D that allows the cancellation of the zero introduced by L_{sh}. The value of L_c was calculated based on a frequency analysis performed on the circuit of Fig. 3(a), where a dynamic current source represents the current I_D flowing through the DUT, and it was demonstrated to be [16]:

$$L_c = \frac{2R_{50}}{R_{sh}}L_{sh} \quad . \tag{5}$$

Based on the last summarized results, a very simplified procedure can be obtained considering that it is possible to associate the current measurement circuit of Fig. 1 to the virtual circuit of Fig. 3(a), which is equivalent to the former between the nodes *A* and ground. In the virtual circuit, the effect of L_{sh} is compensated by the presence of L_c assuming condition (5). It must be noted that the network in Fig. 3(a) is purely theoretical and no physical components (such as the inductor L_c) are added to the real hardware board, thereby avoiding any insertion impedance that could perturb the power switch operation. Therefore, the voltage V_{meas} measured in the physical circuit of Fig. 1 is provided as a digital input to the virtual software-implemented circuit of Fig. 3(b). Since this network operates entirely in the software domain, it does not exert any physical effect on the device-under-test, and its

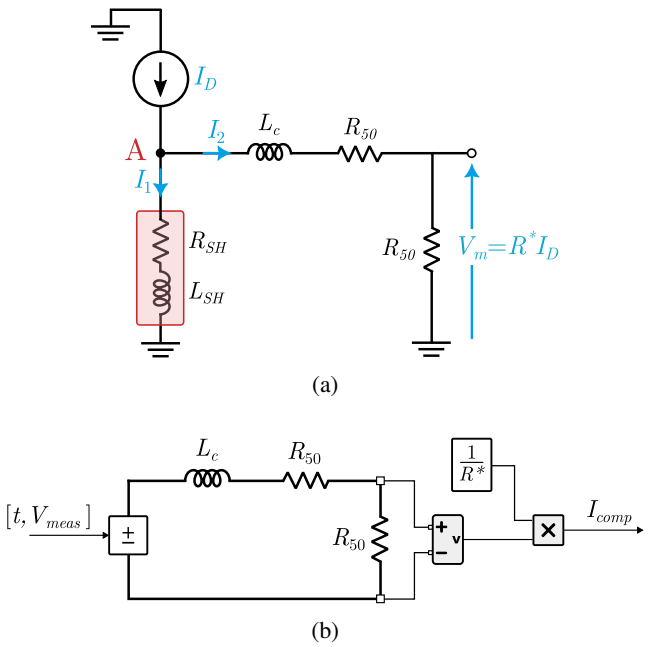

Fig. 3: Equivalent circuit of the hardware network used in [16] to measure I_D, where the inductance L_c is used to compensate for L_{sh} (a) and Simulink/Simscape software implementation for the extraction of I_D from the acquisition of V_{meas} (b).

output (I_{comp}) mathematically reconstructs the original drain current I_D.

The circuit model in Fig. 3(b) has been implemented using the Simscape Power Systems Toolbox of MATLAB/Simulink. The output file of the oscilloscope, that reports the couples [t, V_{meas}], is used as the input of the RL network that reproduces the right part of the circuit of Fig. 3(a). The voltage across R_{50} is then multiplied by $1/R^*$ to obtain the compensated current I_{comp}, corresponding to I_D, that can be displayed and saved. The proposed procedure provides a perfect analogy between software and hardware compensation networks, while avoiding the practical problems associated with hardware compensation, as demonstrated below.

B. Circuit simulations to validate the procedure

A PSpice simulator was used to verify the proposed procedure. PSpice was used to obtain V_{meas} as a two-dimensional vector, as in the experimental tests. This vector was subsequently provided as input to the Simulink network of Fig. 3(b) to extract I_D of the device under test (DUT) and compare it with the waveform directly obtained using the circuit simulator. PSpice simulations were performed on the circuit of Fig. 1 using the model provided by the manufacturer for the 600 V – 23 A GaN HEMTs [21]. The gate resistors R_{Gon} and R_{Goff} of both drivers were set to 10 Ω. The other values were chosen equal to those measured in the experimental setup described in the following section, i.e. $L_{sh} = 1$ nH, $R_{sh} = 11$ mΩ. The resulting value of $L_c = 9.09$ μH to be inserted in the Simulink network of Fig. 3(b) was derived applying (5).

The measurement procedure was used to extract I_D during a Double Pulse Test (DPT) and a type-I short-circuit (SC) test. The DPT simulation was conducted considering Q_2 as the DUT, connecting a 30 μH load inductance in parallel to Q_1, which is kept in *off* state. The SC was obtained by keeping the GaN HEMT Q_1 on before turning on the DUT Q_2 and maintaining it in the *on* state during its entire conduction phase. The test conditions for both the simulated scenarios are: $V_{DC} = 300$ V, V_{GG} (high level voltage of the gate pulse) $= 5$ V.

The obtained simulation results for the DPT and SC are reported in Fig. 4(a) and (b), respectively. The waveforms refer to the DUT drain current furnished by PSpice (dashed blue), the current I_{comp} extracted after Simulink post-processing (green), and the voltage V_{meas} (red) measured across R_{50}. The Simulink model of Fig. 2 derived from the time domain analysis was also used to determine I_{comp}, that is also reported in Fig. 4, but the resulting current waveform is indistinguishable from that of the virtual model of Fig. 3(b), as expected. In fact, the time-domain analysis of the virtual circuit of Fig. 3(b) gives the same expression as (3) for I_D assuming condition (5).

The two insets report the zooms at the device turn-on and turn-off, respectively. Fig. 4 shows that I_{comp} is practically identical to the PSpice drain current, even if V_{meas} is affected by a large overvoltage followed by high-frequency oscillations. The compensated current can also accurately reproduce the high-frequency oscillations due to the resonance between the stray inductance and device output capacitance, which appear on I_D in the first phase of the turn-on and after the device is turned off (see the insets of Fig. 4(a) and (b)).

C. Accuracy of the measurement technique

In this section, we aim to evaluate the accuracy of the proposed technique, with particular attention to the effects of sampling, quantization, and other issues commonly associated with the numerical method. We will analyze how each of these factors may impact the final result.

The first analysis concerns the effects of the sampling rate used to digitize the voltage signal, which significantly affects the accuracy of the measurement technique [22]. Starting from the same test condition of the previous subsection, i.e. $V_{DC} = 300$ V, $V_{GG} = 5$ V, two values of the *on* gate resistance, i.e. $R_{Gon} = 47$ Ω and $R_{Gon} = 10$ Ω, were used to obtain two different rise times in the drain current. The vector of the V_{meas} values was evaluated using a time step of 0.1 ns. The file was subsequently decimated to obtain several vectors with different time steps, as would be obtained experimentally with an A/D converter or an oscilloscope. By reducing the number of samples provided by PSpice, we extracted data with sampling periods of 0.1 ns, 1 ns, 2 ns, and 10 ns, yielding sampling rates of 10 GS/s, 1 GS/s, 500 MS/s, and 100 MS/s, respectively.

The results related to SC for two values of the I_D rise time, i.e. $t_r = 20$ ns and $t_r = 5$ ns, are reported in Fig. 5(a) and (b), respectively. As expected, Fig. 5 clearly shows that a too low sampling rate causes a strong distortion of the current waveform. Acquiring fewer than 5 samples during the current rise time results in an overshoot in the extracted current. This

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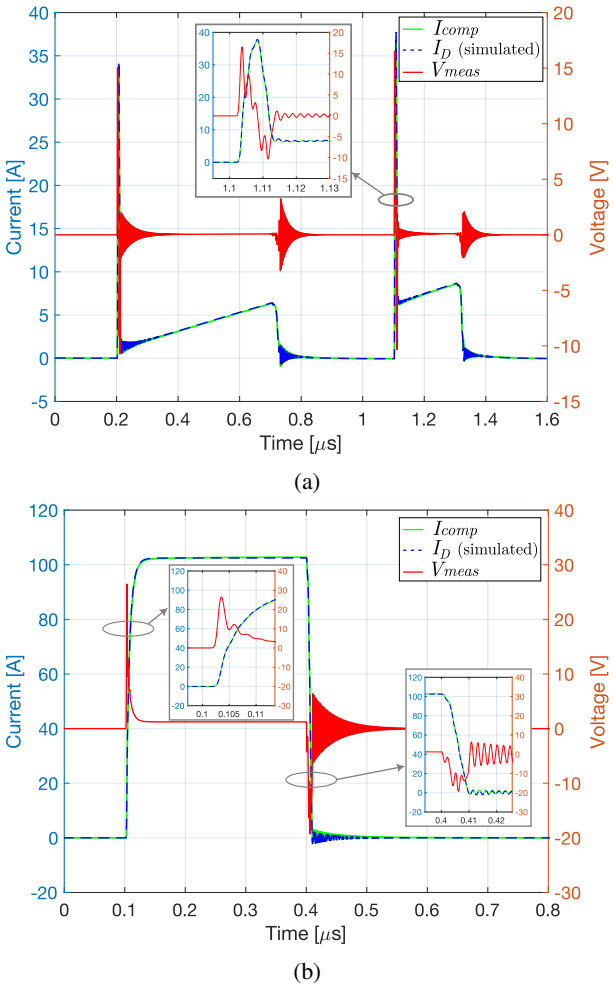

Fig. 4: Simulated drain current waveforms of GaN HEMT Q_2 using Simulink compensation network (green), derived from the voltage V_{meas} measured across the shunt (red) and provided directly by the simulator (blue), for the DPT at 6 A load current (a) and type-I SC (b). The insets report the zoom at the turn-on and turn-off transients.

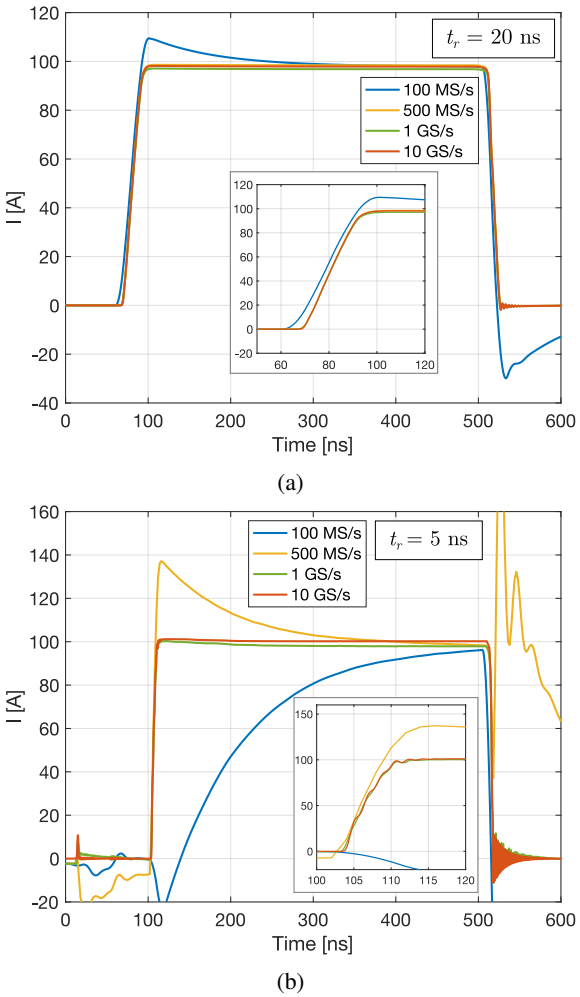

Fig. 5: Simulated I_D waveforms during SC extracted by the proposed procedure using different sampling rates for a rise time of (a) 20 ns and (b) 5 ns. The insets highlight the differences in the evolution of I_D during the rise time using different sampling rates.

happens for the blue curve of Fig. 5(a) at 100 MS/s and the yellow curve of Fig. 5(b) at 500 MS/s, for which 2 and 3 samples were acquired, respectively. This result is consistent with reference [23], which shows that to correctly reproduce a rise time of about 500 ps, a sample rate of 10 GS/s is required. This last comment allows us to correlate the minimum sampling rate to be used, SR_{min}, with the potential bandwidth BW of the proposed measurement technique. Considering the well-known relationship $t_r = 0.35/BW$ between minimum rise time t_r and the bandwidth BW requested to measure the signal, the maximum sampling time must be $\Delta T_{max} = t_r/5$, which corresponds to a minimum sampling rate of:

$$SR_{min} = \frac{1}{\Delta T_{max}} = 14.3 \cdot BW \quad . \tag{6}$$

As a final comment on Fig. 5, it is worth pointing out that the obtained current becomes exponential when no sample is detected along the current rise, as in the blue curve in Fig. 5(b). Indeed, in this case, a sampling rate of 100 MS/s yields a time step of 10 ns, which is greater than the current rise time of 5 ns. Consequently, V_{meas} appears as a step function, and the solution of (3) becomes an exponential waveform with time constant $L_c/(2R_{50}) = 91$ ns.

To examine how the signal quantization affects the measurement accuracy, V_{meas} vector sampled at 1 GS/s, used to obtain the green current of Fig. 5(b), was quantized with different quantization step values. The extracted currents corresponding to 8, 10 and 12-bit resolutions are reported in Fig. 6. The poor accuracy of the blue curve (8-bit resolution) indicates that 256 quantization levels are not sufficient to represent V_{meas} where a large overshoot (30 V) due to parasitic inductance, is present together with the voltage induced by the current through the resistive shunt ($\approx$ hundreds of mV) (see Fig. 4). The green curve with 10-bit resolution has a reasonable accuracy; 12 bits guarantee a very accurate result (red curve).

The circuit simulation was finally used to perform a sensitivity analysis of the measurement method with respect to possible errors on L_c, whose value, according to (5), depends

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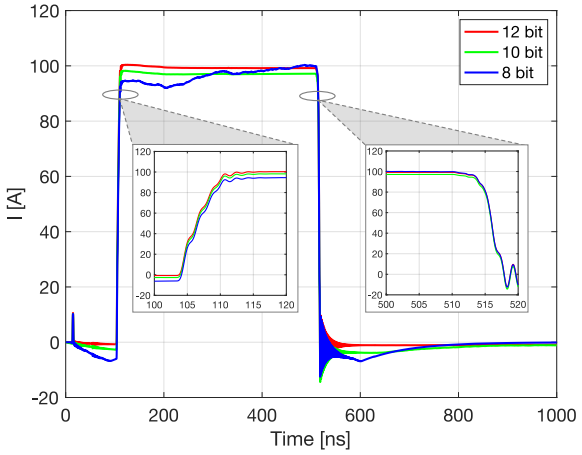

Fig. 6: Simulated I_D waveforms during SC extracted by the proposed procedure using different resolutions of the A/D converter.

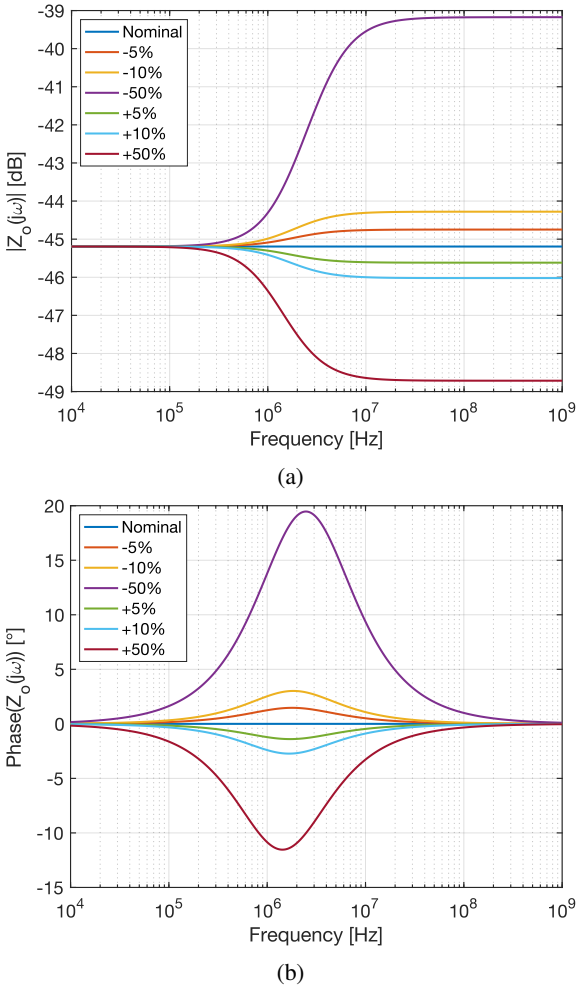

Fig. 7: Frequency response of the equivalent impedance $V_m(j\omega)/I_D(j\omega)$ of the circuit in Fig. 3(a): (a) magnitude and (b) phase.

on the measured values of L_{sh} and R_{sh}. In this case PSpice was only used to carry out an AC analysis of the circuit in Fig. 3(a).

The magnitude and the phase of the equivalent impedance $Z_o(j\omega) = V_m(j\omega)/I_D(j\omega)$ are reported in Fig. 7 for the nominal value of L_c and its variations ΔL_c by $\pm$ 5%, $\pm$ 10% and $\pm$ 50% with respect to the nominal value. The frequency response is flat in magnitude (a) and phase (b) only for the nominal value of L_c (blue curves), assuming a value of -45.19 dB (= 181.8 A/V) for the magnitude and 0° for the phase. For the values of $|\Delta L_c| \leq 10\%$ both magnitude and phase start to deviate from these values at about 100 kHz, and even before for $|\Delta L_c| = 50\%$. At frequencies higher than 10 MHz, the phase returns to zero, and an error independent of the frequency appears in the magnitude, whose sign is positive or negative according to the sign of ΔL_c. The error entity increases with ΔL_c and reaches about –6 dB for $\Delta L_c = -50\%$. It is worth noting that for $|\Delta L_c| \leq 10\%$ the error is below 1 dB in magnitude and 3° in phase at any frequency. Moreover, the solution is affected by a derivative or integral effect for L_c smaller or larger than the nominal value, respectively.

III. Experimental Validation of the Method

A half-bridge test circuit was constructed based on the electrical scheme of Fig. 1 to experimentally validate the proposed method. Its picture is shown in Fig. 8, where the main sections are also highlighted. The GaN HEMTs Q_1 and Q_2 are two 600 V – 23 A CoolGaN™ enhancement-mode devices [21]. The PCB was designed to minimize the parasitic inductance of the connections. Each device is driven by an isolated driver with *on* and *off* resistances that can be set independently. An FPGA-based circuit generates the control signals.

The drain current of the low-side GaN HEMT (Q_2) is measured using CVRs placed between the source power terminal and the power ground. Three solutions were considered, namely a single 33 mΩ SMD resistor, three 33 mΩ SMD resistors stacked on top of each other, and three 33 mΩ SMD resistors mounted on their respective pads on the PCB (see the top left of Fig. 8(a)). A 49.9-Ω resistance is used to match the output impedance of the circuit with the coaxial cable connected to the 50-Ω input resistance of a high sample rate (2.5 GS/s), high-definition (12 bit) and high-bandwidth (1 GHz) digital oscilloscope HDO 6104. To ensure the accuracy and noise immunity of the proposed method under fast switching transients, the coaxial cable must meet specific high-frequency criteria. First, a precise 50-Ω characteristic impedance is mandatory to achieve proper impedance matching with the oscilloscope, thereby eliminating signal reflections that could distort the transient reconstruction. Second, high shielding effectiveness is required to protect the low-amplitude sensor signal from the severe electromagnetic interference due to the high *dv/dt* and *di/dt* of the GaN devices. Lastly, the physical length of the cable must be minimized to mitigate propagation delays and frequency-dependent attenuation. For this application, we adopted a 50-cm RG-58U coaxial cable, suitable up to 5 GHz, with an expected attenuation of 0.65 dB/m at 1 GHz and a propagation delay of 4 ns/m.

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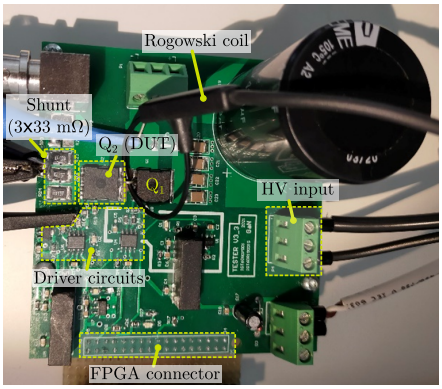
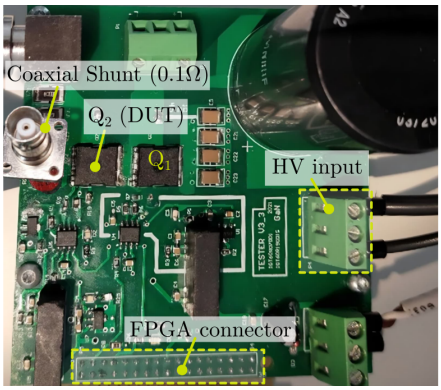


(a)



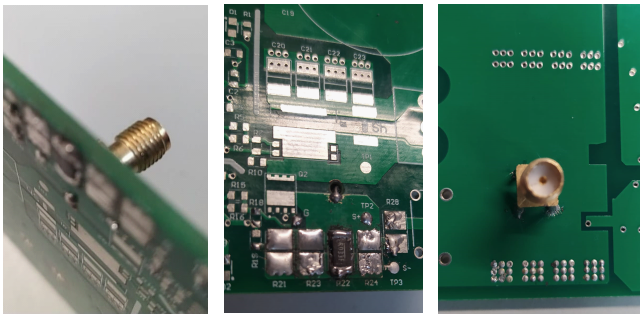
(b)

Fig. 8: Picture of the board used for the experimental validation of the proposed method: PCB equipped with the CVRs and the Rogowski coil (a); PCB with the coaxial shunt mounted in place of the CVRs (b).

To validate the proposed method, the results relating to the measurements with low current gradients were compared with those obtained from the T3RC0300-UM Rogowski coil inserted in the circuit, thanks to a very small external jumper placed between the drain of Q_2 and the source of Q_1 (see Fig. 8(a)). For tests with larger current gradients, where the Rogowski coil could not be used due to its bandwidth limitations, the proposed method's results were compared with those from the SDN-414-10, 100 mΩ coaxial shunt. In this case, it was not possible to insert the two sensors in series to measure the same current, since both sensors must have a terminal connected to the oscilloscope ground. Consequently, two tests were performed: first, inserting the CVR, then replacing it with the coaxial shunt, between the same PCB pads. The picture of the PCB with the coaxial shunt mounted in place of the three SMD shunts is shown in Fig. 8(b).

A. Measure of CVR stray inductance

The measurement of the CVR's leakage inductance is one of the elements that most limits the extraction of current from the voltage measurement on the CVR [18]–[20]. To perform this measurement, a PCB similar to that of Fig. 8 without other mounted components was slightly modified to insert an SMA RF connector on its back-side, as shown in Fig. 9 which shows a side view (a), a front view (b) and a rear view (c) of the modified portion of the board. This PCB was used to measure the inductance L_{sh} in the range between 50 kHz and 4.4 GHz using a SV4401A Vector Network Analyzer, VNA. Measuring this inductance is quite critical because its value is comparable to that of the parasitic elements of the measurement circuit. Therefore, it was necessary to perform a very careful VNA calibration. As usual, three types of loads were used: open circuit, short circuit, and 50 ohm load. In particular, it was necessary to both create the short circuit and mount the 50 ohm load directly on the PCB being measured. To illustrate the measurement methodology, Fig. 10(a) shows a cross-sectional sketch of the portion of the PCB on which the TL3A SMD CVR is mounted. The dimensions of this CVR are $L = 6.4$ mm, $W = 3.2$ mm, and $H_1 = 0.6$ mm, and it is mounted on a PCB whose thickness $H_2 = 1.6$ mm, as shown in Fig. 10(a). To better explain the measurement result, the current path (red lines and arrows on the surfaces) and the dashed blue region, where the magnetic field associated with the CVR leakage inductance is concentrated, are highlighted in Fig. 10(b). The inductance measurement performed at the CVR terminals provides the value of the inductance associated only with region A of Fig. 10(b), that is, the region between the CVR surface and the PCB top surface. In fact, since the calibration was performed by imposing a short circuit directly on the PCB surface, region B of Fig. 10(b), between the two PCB surfaces, was included in the circuit's leakage inductance and therefore does not contribute to the value measured between the two CVR terminals. However, it is possible to extract the actual value of the CVR inductance by considering that the magnetic field flux lines are strictly concentrated in the entire dashed region of Fig. 10(b), as demonstrated in [24]. Therefore, the CVR inductance is directly proportional



(a) (b) (c)

Fig. 9: Pictures of the modified circuit for measuring CVR stray inductance: side (a), front (b), and back (c) views.

to the area where the field concentrates. Consequently, the value of CVR inductance can be obtained by multiplying the measured inductance associated with region A, by the ratio of the total area (region A + B) to the area of region A alone, a ratio which in our case is equal to 3.67. Using this approach, it was possible to obtain the results in Fig. 11, which reports the values of the CVR leakage inductance in the three cases: single SMD resistor (green curve), three SMD resistors mounted one on top of the other (blue curve), and three SMD resistors mounted on their respective pads

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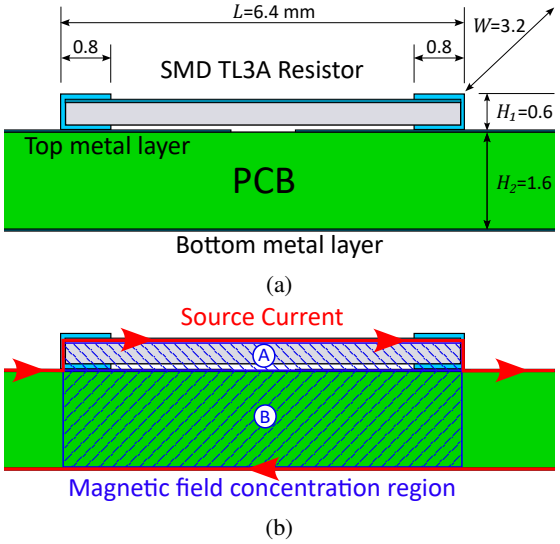


Fig. 10: Side section of the PCB portion on which the CVR is mounted (a). Evidence of the source current path and the region below the CVR where the magnetic field that originates the CVR's stray inductance is concentrated (b).

on the PCB (red curve). The resonances between the CVR inductances and their respective parasitic capacitances appear in all three cases at frequencies above 1 GHz. Thus, apart from the measurement noise, the inductance values are practically constant over a wide frequency range, and, in principle, the proposed technique's potential bandwidth can reach 1 GHz. In practice, it is limited by the sampling frequency adopted in the experimental setup. In our case, using (6) with a sampling frequency of 2.5 GS/s yields a bandwidth of 175 MHz. In this frequency range, the inductance values measured in the three cases remain practically constant, as shown in the inset of Fig. 11, which reports the zoom of the three inductance values in the range between 80 MHz and 200 MHz.

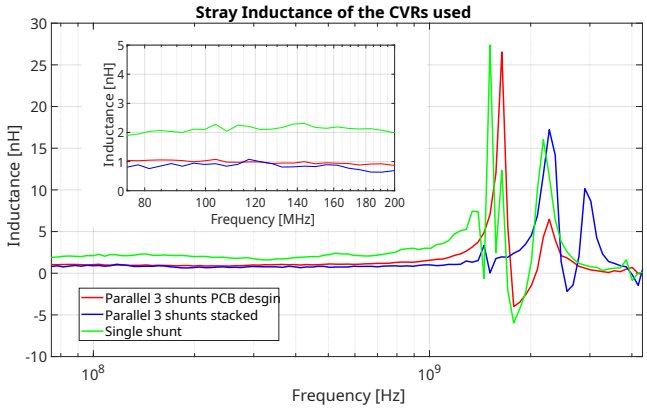


Fig. 11: Measurement of the CVR leakage inductance as a function of frequency in three cases: Single SMD resistor (green curve), three SMD resistors mounted one on top of the other (blue curve), and three SMD resistors mounted on their respective pads on the PCB (red curve).

For the first configuration, where the CVR is constructed with a single shunt resistor, an analytical expression for the leakage inductance as a function of the structure's geometric parameters can be derived. Indeed, this situation is very similar to that of a strip line constructed on the top surface of a PCB, with the ground plane on its bottom surface. To calculate the leakage inductance of this structure, the following formula can be used [25]:

$$L_{sh} = \frac{120\pi L}{v_o}\left[\frac{1}{\frac{W}{H} + 1.393 + 0.667 \cdot \ln\left(\frac{W}{H} + 1.444\right)}\right] \quad (7)$$

which is valid for $W/H > 1$, and where: W and L are the width and length of the strip line, respectively, H is its distance from the ground plane, and v_o is the speed of light in vacuum. Dimensions are expressed in meters. The assumptions made for (7), namely that the ground plane is a perfect conductor, of infinite extension, and that the conductor has zero thickness and uniform height with respect to the ground plane, are well respected in our case (7) and provides $L_{sh} = 2.15$ nH, which is in excellent agreement with the experimental data in Fig. 11. This value is obtained by considering the following values: $L = 6.2$ mm, $W = 3.2$ mm, and $H = H_1 + H_2 = 2.1$ mm, which can be deduced from Fig. 10(a).

As a final comment to this paragraph, and before the experimental validation, it is worth noting that, based on the already cited formula $t_r = 0.35/BW$, the minimum rise time that can be achieved with the proposed method is 2 ns, much lower than that of the Rogowski, equal to 12 ns. The coaxial shunt employed, in principle, has an even lower rise time, but its performance is limited by the stray parameters introduced into the power branch of the circuit. Therefore, for a first validation of the method, the current waveforms detected in short circuit were compared with those measured with the Rogowski coil, which have rise times compatible with those detected experimentally. Validation of lower rise times was performed by comparing the GaN DUT hard-switching waveforms measured with the proposed method with those measured with the coaxial shunt.

B. *Short-circuit tests*

The first test was carried out considering a type-I SC test with a duration of 400 ns in the test conditions: $V_{dc} = 300$ V, $V_{GG} = 4$ V (power supply of the DUT driver) and $R_{Gon} = R_{Goff} = 47\ \Omega$ (on gate resistance of the DUT). In this case, due to the large values of the current, a parallel of three stacked shunt resistors was used, for which the resistance was $0.011\ \Omega$, and the stray inductance was settled to 1 nH (see Fig. 11). The results are shown in Fig. 12(a). As expected, the voltage measured across the shunt (yellow curve) exhibits an overshoot at turn-on and an undershoot at turn-off due to the parasitic inductance. The rise times and fall times of the current measured with Rogowski coil (subscript RC) and the software procedure (subscript SP) are: $t_{r,RC} = 20$ ns, $t_{r,SP} = 21$ ns, $t_{f,RC} = 21$ ns, and $t_{f,SP} = 17$ ns, respectively. For the reader's convenience, these values are summarized in Table I, along with the other SC switching times described in this section. Apart from a 9 ns delay introduced by the Rogowski coil, the waveforms measured with the two methods are very similar and accurately reproduce the expected current,

TABLE I: Switching times of the drain current for the short-circuit tests described in this section.

	Rogowski Coil		Software Procedure	
	Rise time (ns)	Fall time (ns)	Rise time (ns)	Fall time (ns)
SC with $R_{Gon} = R_{Goff} = 47\ \Omega$	20	21	21	17
SC with $R_{Gon} = R_{Goff} = 10\ \Omega$	14	14	8	9.6

with rise and fall times compatible with the bandwidth of both methods.

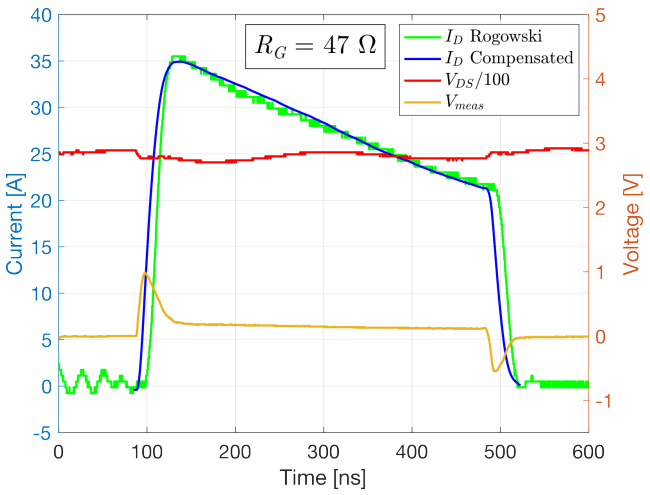
The second test was still a type-I SC but using $R_{Gon} = R_{Goff} = 10\ \Omega$ and the same test conditions as the previous test. The resulting waveforms are shown in Fig. 12(b). The reduced gate resistance results in faster transients and therefore a more significant influence of parasitic parameters on the measured voltage across the shunt (yellow curve). As a first comment on the result, to confirm the validity of the proposed method, it is essential to note that it allows the detection of the current tail observed when the GaN HEMTs are turned off after a short-circuit. Moreover, the current rise and fall times measured with Rogowski coil and software procedure are: $t_{r,RC} = 14$ ns, $t_{r,SP} = 8$ ns, $t_{f,RC} = 14$ ns and $t_{f,SP} = 9.6$ ns, respectively. These switching times fall within the range measurable with the proposed technique but not with the Rogowski coil, which provides an unreliable current waveform (green curve in Fig. 12(b)), exhibiting noncoherent switching times along with high-frequency oscillations in addition to the 9 ns delay because the sensor starts to behave like a resonant circuit [26], [27].

C. Hard Switching tests

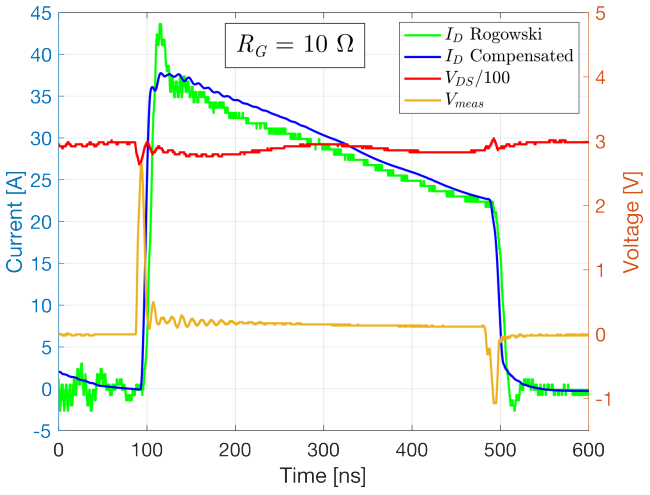
The proposed method was then used to extract the drain current of a GaN power HEMT during inductive hard-switching tests, which exhibit faster switching times. The test circuit was obtained from that of Fig. 1 where an inductance $L_o = 66\ \mu$H was connected in parallel to Q_1. The driver of Q_1 was set to the off state with $V_{GS} = 0$ V, leaving the device as a freewheeling diode. Double-pulse tests were performed on Q_2, used as the DUT. The test current was settled by varying the duration of the first pulse. In these tests, due to lower drain currents, a single shunt resistor with $R_{sh} = 0.033\ \Omega$ was used as the CVR to improve measurement sensitivity. $L_{sh} = 2.15$ nH obtained from (7) was used in the extraction procedure. Additionally, to align the current waveform with the voltage ones, the current was advanced by 0.4 ns.

The coaxial shunt SDN-414-10 was used for the waveforms comparison in place of the Rogowski coil, which could not be used due to its limited bandwidth, incompatibility with very fast switching times, and the oscillatory, very noisy waveforms it produces (not reported here for brevity).

Fig. 13 shows the comparison between the turn-on waveforms of the drain voltage (solid red curve), gate voltage (dashed red curve), and the drain current (solid blue curve) extracted with the proposed method (Fig. 13(a)) and measured with the coaxial shunt (Fig. 13(b)). The figures refer to inductive hard turn-on under the following test conditions: $+V_{DC} = 400$ V, $V_{GG} = 4$ V, and $R_{Gon} = 22\ \Omega$.



(a)



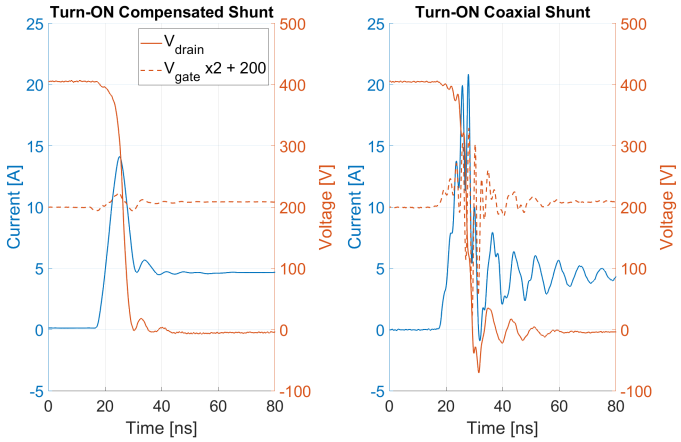
(b)

Fig. 12: Waveforms of V_{DS} (red), V_{meas} (yellow), I_D measured with the Rogowski coil (green) and I_D obtained with the proposed software procedure (blue). Test conditions: $V_{dc} = 300$ V, $V_{GG} = 4$ V, (a) $R_G = 47\ \Omega$, (b) $R_G = 10\ \Omega$.

As previously mentioned, since both the CVR and the coaxial shunt require a voltage measurement referred to ground, it was not possible to mount them in the same circuit. Therefore, the measurement in Fig. 13(a) was performed on the CVR mounted between the source and ground, while, for the test of Fig. 13(b), the CVR was disconnected, and the coaxial shunt was mounted in its place. The test conditions were the same for the two figures.

The current waveform extracted with the proposed method (see Fig. 13(a)) is consistent with the capacitive switching associated with the charge of Q_1 and Q_2 capacitances. Indeed, after a small step in the drain voltage, due to the circuit's stray inductance, the current exhibits impulsive behavior, corresponding to the derivative of the drain voltage during its descent. In particular, after a peak of 14.1 A at 25.1 ns and some oscillations in the final part of the turn-on due to the resonance between DUT capacitance and circuit inductance, the current reaches the on value of 4.7 A. The rise time

measured between 10% and 90% of the current peak is $t_{r,SP} = 5.6$ ns. The analysis of the waveforms of Fig. 13(a) allows the estimate of the circuit stray parameters. In particular, considering the drain voltage jump in the first phase and the related dI/dt, a total leakage inductance of $L_{s,tot} = 5.3$ nH was estimated, of which 2.2 nH are attributable to the CVR, as previously mentioned, and the remaining 3.1 nH to the output mesh of the power circuit. Moreover, assuming the value of the total stray inductance and the oscillation frequency ($f_{Osc,CVR} \approx 170$ MHz) in the final phase of the turn-on transient, it is possible to estimate a total parasitic capacitance of $C_{s,tot} = 160$ pF, which includes: $C_{OSS,Q_2} = 110$ pF (@$V_{DS,1} \simeq 0$ V) [21], $C_{OSS,Q_1} = 28$ pF (@$V_{DS,2} \simeq 400$ V) [21], in addition to the parasitic capacitance of the busbar, which is difficult to determine.



(a) (b)

Fig. 13: Comparison between the drain voltage (solid red curve), gate voltage (dashed red curve), and the drain current (solid blue curve), extracted with the proposed method (a) and measured with the coaxial shunt (b). Test conditions: $+V_{DC} = 400$ V, $V_{GG} = 4$ V and $R_{Gon} = 22\ \Omega$.

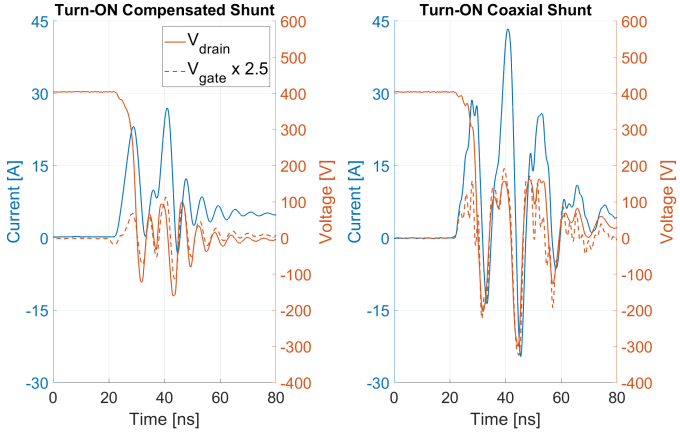
On the other hand, the waveforms of Fig. 13(b) compared to those of Fig. 13(a), show the strong impact of the coaxial shunt insertion in place of the CVR. Before the discussion, it is worth outlining that aligning the waveforms in Fig. 13(b) required a current advance of 1.8 ns, typical for coaxial shunts [28].

Fig. 13(b) shows an oscillation at $f_{Osc,CS,1} \approx 480$ MHz (period of 2.1 ns) in the initial turn-on phase, which overlaps with the impulsive current transient related to the charging of the Q_1 and Q_2 capacitances. After the very high-frequency oscillations disappear, resonance-related oscillations between the parasitic inductance and the total circuit capacitance appear, with greater amplitude, less damping, and lower oscillation frequency ($f_{Osc,CS,2} \approx 130$ MHz), compared to the waveforms of Fig. 13(a). From $f_{Osc,CS2}$, and the previously estimated total parasitic capacitance, we estimated the overall parasitic inductance of the output mesh of the power circuit with the coaxial shunt to be 8.9 nH. Considering the previously estimated value of the circuit inductance (3.1 nH), it is possible to assign to the coaxial shunt a stray inductance of 5.8 nH, in line with the values reported in the literature [28].

Let's focus now on the initial high-frequency oscillations. Their initially divergent behavior suggests that it is due to a positive feedback mechanism within the switching circuit. A detailed layout analysis reveals that the physical insertion of the bulky coaxial shunt introduces a significantly higher common-source inductance compared to the compact SMD shunt configuration. According to the instability and oscillation analysis reported in the literature [29], the common-source inductance acts as a shared impedance between the main power loop and the gate-drive loop. During fast switching transients, the high *di/dt* flowing through this common path induces an overvoltage that actively perturbs the internal V_{GS}. This interaction establishes a critical positive feedback loop that triggers severe and sustained high-frequency oscillations in both I_D and V_{DS}. Conversely, when the proposed SMD shunt is utilized, its ultra-low profile and optimized PCB footprint keep the common-source inductance at the minimum. As a result, dynamic instabilities are not triggered, even if they could occur with higher *di/dt*.

As a final comment on Fig. 13(b), it is worth noting that the rise time measured between 10% and 90% of the peak drain current is $t_{r,CS} = 4.74$ ns, which is lower than that obtained with the CVR. However, it should be emphasized that time measurements with the coaxial shunt are compromised by the presence of the high-frequency oscillation.

To test the procedure for shorter switching times, a test was carried out with $R_{Gon} = 4.7\ \Omega$, leaving the other test conditions unchanged compared to the previous test. Fig. 14 shows the results obtained. The line colors chosen for the waveforms are the same as those in Fig. 13.



(a) (b)

Fig. 14: Comparison between the drain voltage (solid red curve), gate voltage (dashed red curve), and the drain current (solid blue curve), extracted with the proposed method (a) and measured with the coaxial shunt (b). Test conditions: $+V_{DC} = 400$ V, $V_{GG} = 4$ V and $R_{Gon} = 4.7\ \Omega$.

As can be seen in Fig. 14(a), the reduction of the on-gate resistance causes an increase in the current and voltage slopes, with a significant increase of the current peak (≈ 23 A). The drain voltage amplitude increases as well, leading to a higher gate voltage and a further current peak (≈ 27 A) at about 41 ns. Afterward, a dumped oscillation appears at the same

frequency as the last part of the waveforms in Fig. 14(a), associated with the resonance between the capacitances of Q_1/Q_2 and the output circuit's stray inductance. Fig. 14(b), concerning the circuit with the coaxial shunt, confirms the presence of a high frequency oscillation at $\approx$ 470 MHz, involving the gate voltage, of the same nature as that observed in Fig. 13(b). This oscillation overlaps with that related to the resonance between the capacitances of Q_1/Q_2 and the parasitic inductance of the power circuit, but with amplitudes greater than those in Fig. 14(a) due to the higher stray inductance. The current rise times measured between 10% and 90% of the current first peak are: $t_{r,SP} = 4.4$ ns, and $t_{s,CS} = 4.7$ ns, extracted with the software procedure and measured with the coaxial shunt, respectively. Here, too, the measurement with the coaxial shunt is corrupted by the high-frequency oscillation. A synoptic comparison of the switching times extracted using the software procedure and those measured with the coaxial shunt is presented in Table II.

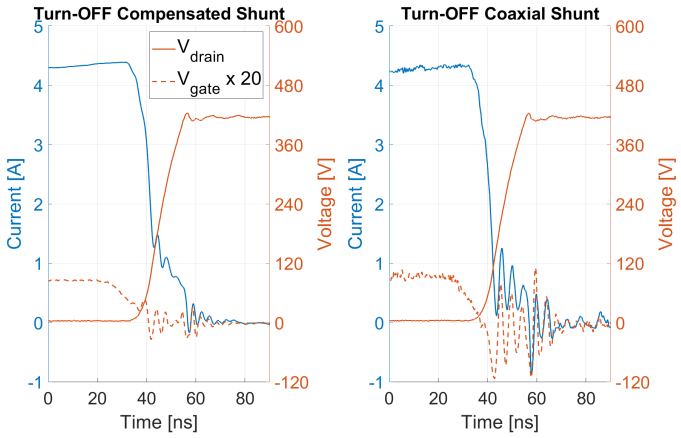
It is worth noting that with the devices used in the circuit, it is not possible to achieve switching times of 2 ns to fully test the full potential of our measurement setup. In fact, a further reduction in gate resistance would yield only a minimal reduction in switching times, but would be associated with particularly noisy, difficult-to-interpret waveforms.

TABLE II: Switching times of the drain current for the hard switching tests described in this section.

	Coaxial Shunt		**Software Procedure**	
	Rise time (ns)	Fall time (ns)	Rise time (ns)	Fall time (ns)
Turn-on with $R_{Gon} = 22\ \Omega$	4.74	-	5.6	-
Turn-on with $R_{Gon} = 4.7\ \Omega$	4.7	-	4.4	-
Turn-off with $R_{Goff} = 3.3\ \Omega$	-	5.5	-	5.9

A double-pulse test was also used to measure the inductive turn-off waveforms. Fig. 15 shows the waveforms of the drain voltage (red curve), gate voltage (red dashed curve), and drain current (blue curve) extracted using the software procedure (Fig. 15(a)) and measured with the coaxial shunt (Fig. 15(b)). Both figures show that the current decay occurs in two phases: a very fast one and a slower one, the latter characterized by high-frequency oscillations. Without delving into the physics of switching, it is noteworthy that in the first phase, the software procedure provides a waveform very similar to that measured with the coaxial shunt, with comparable fall times of $t_{f,SP} = 5.9$ ns and $t_{f,CS} = 5.5$ ns, respectively. The presence of oscillations in the second phase renders it difficult to unequivocally determine 10% of the current; therefore, the two fall times were measured between 90% and 33% of the peak current at the onset of the turn-off.

A marked difference between the two current waveforms is observed in the second phase of the current descent. In both cases, the oscillation does not involve the drain voltage, which maintains a practically identical waveform. Instead, the oscillation appears to be triggered by small oscillations in the drain current during the first phase of descent and sustained by the stray inductance between the source and ground, which reflects a voltage on the gate through the current derivative. The larger value of the coaxial shunt's stray inductance causes



(a) (b)

Fig. 15: Comparison between the drain voltage (solid red curve), gate voltage (dashed red curve), and the drain current (solid blue curve), extracted with the proposed method (a) and measured with the coaxial shunt (b). Test conditions: $+V_{DC} = 400$ V, $V_{GG} = 4$ V and $R_{Goff} = 3.3\ \Omega$.

a larger amplitude and more persistent oscillation in the related circuit (Fig. 15(b)). This oscillation could be mitigated by connecting the gate driver between the gate and the DUT's Kelvin source, if available, which is not the case in our circuit. From Fig. 15, however, it can be observed that using the CVR in the power circuit is less invasive than the coaxial shunt.

Finally, we used the experimental measurements presented above in Fig. 13, 14 and 15 to evaluate the switching energy losses and the peak drain current of the DUT to provide a quantitative assessment of the practical impact of the compensated CVR and the coaxial shunt. The computed turn-on energy (E_{on}), turn-off energy (E_{off}), and peak drain current ($I_{D,pk}$) for $R_{Gon} = 22\ \Omega$ and $R_{Gon} = 4.7\ \Omega$ are summarized in Table III. Due to the non-negligible insertion inductance physically introduced into the power loop by the coaxial shunt, severe high-frequency ringing is triggered at turn-on. This parasitic resonance causes an artificial inflation of the calculated turn-on losses compared to the non-invasive SMD shunt setup, showing an increase of approximately +2% when $R_{Gon} = 22\ \Omega$ and +4% when $R_{Gon} = 4.7\ \Omega$. Correspondingly, the physical insertion inductance distorts the current-voltage overlap profile during turn-off, leading to a slightly lower calculated E_{off} when the coaxial shunt is adopted. This severe alteration of the circuit dynamics is further highlighted by the peak drain current values: under fast switching conditions ($R_{Gon} = 4.7\ \Omega$), the coaxial shunt configuration exhibits an artificial current peak of 28.6 A, whereas the native compact layout equipped with the SMD shunt experiences a much lower peak of 23.1 A. For the sake of clarity, the considered $I_{D,pk}$ is the first peak reached by the drain current during the turn-on, neglecting subsequent oscillations. These metrics demonstrate the inherent advantage of the proposed software-compensated SMD shunt for fast switching application. By utilizing a standard SMD footprint, the physical integrity and low inductance of the power loop

TABLE III: Comparison of switching losses and peak drain current extracted from the experimental tests in the conditions: $V_{DC} = 400$ V, $V_{GG} = 4$ V, $R_{G,off} = 3.3\ \Omega$, load current $= 5$ A.

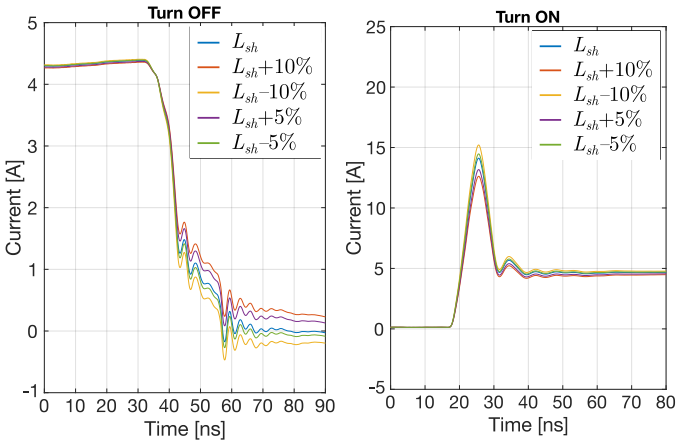
$R_{Gon}(\Omega)$	Current Sensor	E_{on} (μJ)	E_{off} (μJ)	$I_{D,pk}$ (A)*
22	Coaxial Shunt	37.71	2.22	20.0
22	Compensated SMD Shunt	36.84	3.10	14.1
4.7	Coaxial Shunt	44.47	2.74	28.6
4.7	Compensated SMD Shunt	42.46	4.93	23.1

*First peak of drain current during the turn-on.

are fully preserved, ensuring that the power switch operates in its unperturbed state. The localized parasitic inductance of the SMD shunt is then cleanly suppressed in the digital domain by the software algorithm, providing an accurate, non-invasive measurement framework that avoids the hardware-induced distortions typical of coaxial sensors.

D. Sensitivity analysis

To complete the experimental verification of the software procedure, a sensitivity analysis was performed on the leakage inductance L_{sh} used in the extraction procedure. Fig. 16 reports the drain current waveforms extracted using the software procedure at the turn-off (Fig. 16(a)) and at the turn-on (Fig. 16(b)) using different values of the stray inductance, namely, the nominal value $L_{sh} = 2.15$ nH, supplied by (7), $L_{sh}\pm5\%$ and $L_{sh}\pm10\%$. The test conditions are the same as in the previous figures, which are: $+V_{DC} = 400$ V, $V_{GG} = 4$ V, $R_{Gon} = 22\ \Omega$ and $R_{Goff} = 3.3\ \Omega$.



(a) (b)

Fig. 16: Drain current waveforms extracted using the software procedure at the turn-off (a) and at the turn-on (b) using different values of the stray inductance, namely, the nominal value $L_{sh} = 2.15$ nH, $L_{sh} \pm 5\%$ and $L_{sh} \pm 10\%$. Test conditions: $+V_{DC} = 400$ V, $V_{GG} = 4$ V, $R_{Gon} = 22\ \Omega$. and $R_{Goff} = 3.3\ \Omega$.

Focusing on the turn-off waveforms (Fig. 16(a)), only the blue curve, corresponding to the nominal L_{sh}, reaches zero at the end of turn-off. The waveforms obtained with lower inductances (yellow and green curves) show an undershoot corresponding to a derivative effect, as expected from the results in Fig. 7. Conversely, the purple and red curves, relating to higher inductance values, show an integral behavior, also confirmed by the results in Fig. 7. Referring to Fig. 16(b), higher inductance values (red and purple curves) cause an underestimation of the peak and steady-state current due to the integral effect. Conversely, lower values (yellow and green curves) cause an overestimation due to the derivative effect.

E. Final remarks on experimental results

The experimental results presented in the previous subsections have demonstrated that the proposed software procedure allows for the extraction of the drain current with a significantly wider bandwidth than that of a Rogowski coil with the introduction of a comparable parasitic inductance. Furthermore, for signals measured on commercial GaN HEMTs, the procedure enabled correct current measurement with rise times of 4.4 ns, slightly higher than those achievable with the used measurement setup (2 ns). For these signals, the waveforms obtained with the proposed method are comparable to those obtained using a coaxial shunt, which, however, introduces parasitic inductances and capacitances that alter the switching transient and, in some cases, favor the triggering of very annoying high-frequency oscillations.

In practice, for the rise times measured on the DUT, it would be sufficient to use less performing A/D converters. In particular, cost-effective converters with lower sampling rates can be used to test the DUT and GaN devices with similar switching characteristics. Furthermore, the low parasitic inductance introduced by our CVR results in overvoltage during the on-off transients of a few volts, not much greater than the shunt resistive voltage drop (hundreds of mV). Therefore, to measure the shunt voltage, a lower-resolution A/D converter is sufficient. This is demonstrated by the waveforms in Fig. 17, which shows both the current waveform in Fig. 15(a) (blue curve), obtained with a sampling rate of 2.5 GS/s and a resolution of 12 bits, and the red curve, which was obtained from the measured voltage vector V_{meas}, taking 1 sample out of 4, for a sampling rate of 625 MS/s. Each sample was represented with 8 bits of resolution rather than 12. The two waveforms are virtually indistinguishable. This operation was performed on the turn-off current, which has the highest dI/dt values and the highest frequency oscillations among the CVR-achieved waveforms presented here. This result is in line with (6), which indicates an expected bandwidth of approximately 45 MHz for a sampling rate of 625 MS/s. With this rate, 16 samples are acquired in the approximately 26 ns duration of the current descent, sufficient to faithfully reconstruct the current waveform.

The aforementioned considerations indicate that the proposed software procedure enables real-time measurement of the converter switching current, with a bandwidth limited primarily by the sampling rate of the ADC. Given the variety of ADCs on the market, the component selection involves a trade-off between performance and cost, tailored to the specific requirements of the target application. For instance,

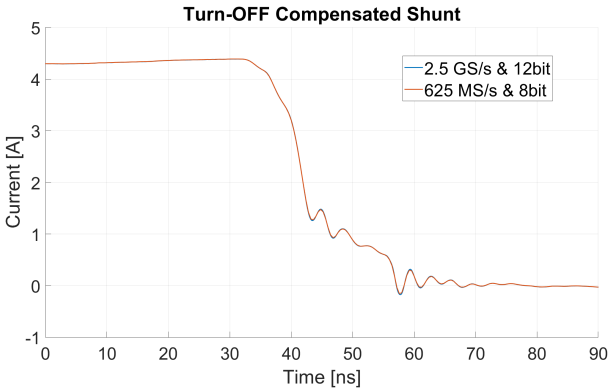


Fig. 17: Comparison between the drain current waveforms derived from applying the software procedure to the vector extracted from V_{meas}, acquired at 2.5 GS/s with 12-bit resolution (blue curve), and the red curve with 625 MS/s and 8-bit resolution obtained by reducing the number and the resolution of samples.

8-bit ADCs with a sampling rate of 600 MS/s – available at a competitive price point – can provide a measurement bandwidth of approximately 45 MHz, which is sufficient for many high-frequency industrial and automotive power stages. However, superior performance can be achieved by utilizing a 1.5-GS/s ADC, yielding a bandwidth of about 100 MHz, albeit at a significantly higher system cost.

IV. Conclusion

A software procedure for extracting the drain current in a fast-switching device from the voltage measured across a resistive shunt (CVR) placed in series with its source has been presented. The accuracy and the bandwidth of the measurement depend on the acquisition system. We demonstrated, through circuit simulations and experimental tests, that measurements with a 175 MHz bandwidth are possible with a high-resolution 2.5 GS/s oscilloscope.

The software was implemented as an implicit solution of a Simulink block schematic, but, in principle, can be numerically solved on any processor or FPGA. Only the stray inductance associated with the CVR is used as a parameter of the model. It can be measured on the test circuit or, in a very common case, employing a single shunt resistor as a CVR, the parameter to be used can be calculated using the formula for the strip-line stray inductance.

The software procedure was applied for the offline extraction of the current measured in a double-pulse test. Based on the results obtained, we also propose using it to measure the current in a power converter in real time. To this end, we propose a cost-effective solution, compatible with implementation in a realistic converter, based on an 8-bit A/D converter with a sampling rate of 600 MS/s, controlled by an FPGA that should also implement the numerical solution of the proposed model. This solution guarantees a bandwidth of 45 MHz corresponding to a rise time of 8 ns, and can be used in converters based on WBG devices.

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