electronics

MDPI

Article

Feedback Injection for Low-Cost Dynamic Testing of DC–DC Power Supplies

Nicola Femia [1] and Giulia Di Capua [2,*]

[1] Department of Information Engineering, Electrical Engineering, and Applied Mathematics (DIEM), University of Salerno, Via Giovanni Paolo II, 132, 84084 Fisciano, Italy; femia@unisa.it
[2] Department of Electrical and Information Engineering "Maurizio Scarano" (DIEI), University of Cassino and Southern Lazio, Via di Biasio, 43, 03043 Cassino, Italy
* Correspondence: giulia.dicapua@unicas.it

Abstract

Dynamic characterization of DC–DC power supplies typically requires dedicated dynamic voltage sources and electronic loads, which are often expensive and not readily available in low-cost laboratory environments. This creates a need for simple and flexible solutions capable of performing reliable line and load transient tests without complex auxiliary hardware. This paper presents a cost-effective technique for the dynamic testing of DC–DC power supplies, which can be applied with high versatility to both line and load transient testing. It is shown that injecting a perturbation signal into the feedback loop of a standard DC–DC regulator enables the regulator to operate either as a dynamic voltage source or as a dynamic electronic load, thus supporting both transient and small-signal AC characterization of a power supply under test. Analytical guidelines are provided to determine the static operating conditions and the achievable bandwidth of regulators operating in Dynamic Source Mode (DSM) and Dynamic Load Mode (DLM). The impact of voltage-mode and current-mode control strategies, as well as different error amplifier implementations, is investigated. Experimental line and load transient tests are carried out on interconnected switching and linear power supplies using Texas Instruments PMLK Series BUCK, BOOST, and LDO boards operating from 3.6 W to 36 W, with crossover frequencies up to 20 kHz. Measured injection gains and transient responses confirm the analytical predictions and demonstrate that FIT provides a simple, reliable, and cost-effective solution for dynamic testing of low-power DC–DC converters.

Keywords: DC–DC power supplies; dynamic testing techniques; feedback injection; dynamic load emulation; dynamic source emulation; line and load transients; low-power converters; voltage-mode control; current-mode control

Academic Editor: Ahmed Abu-Siada

Received: 4 February 2026
Revised: 20 February 2026
Accepted: 21 February 2026
Published: 27 February 2026

1. Introduction

A wide range of tests is required to evaluate a power supply's performance and verify its compliance with specifications and standards. Line transient, load transient, power supply rejection ratio (PSRR), and output impedance (OI) measurements are commonly performed to assess the noise rejection and dynamic behavior of power supplies [1,2]. These tests require an input voltage source and an output current load capable of superimposing a DC component on an AC perturbation, thereby implementing a power-summing amplifier function, as illustrated in Figure 1.

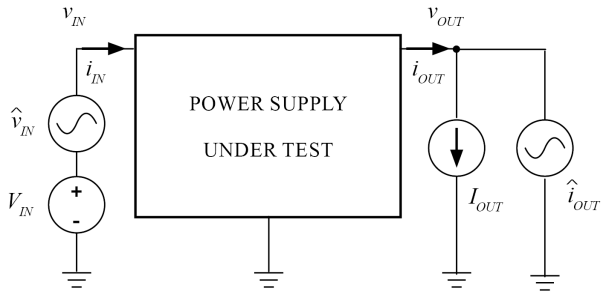


Figure 1. Dynamic load and line transient test configurations for a power supply under test.

In line and load transient tests, the AC component of the source or load is typically a square-wave signal with a fixed frequency [3]. Conversely, PSRR and OI measurements require a sinusoidal excitation with an adjustable amplitude and a frequency sweep from a few hertz to the megahertz range [4]. Line and load transient responses are generally measured using an oscilloscope, whereas PSRR and output impedance are measured using a vector network analyzer. Professional power electronics laboratories are usually equipped with high-performance instrumentation, including dynamic voltage sources and electronic loads, to perform the full set of required dynamic tests. These instruments are often implemented as dedicated and distinct pieces of equipment. The design challenges and limitations of dynamic voltage sources are discussed in [5], while [6] provides a comprehensive overview and classification of electronic loads.

Enhanced transient measurement strategies for DC–DC converters have been investigated to enable precise characterization of input/output dynamics during rapid load or source variations, like in maximum power point tracking systems [7] or in converters operating under discontinuous conduction mode [8]. Several solutions have been proposed in the literature to improve dynamic testing performance or address specific application requirements. For example, energy-regenerative electronic loads are discussed in [9,10], while an inverter-based solution for real-time induction motor emulation is presented in [11]. Hardware-in-the-loop approaches for testing power electronics control systems are investigated in [12], and dedicated circuits for input/output impedance measurements in point-of-load regulators are proposed in [13]. The Z-source converter architecture is used in [14] to implement high-efficiency energy-recycling electronic loads for testing photovoltaic cells, power converters, and stand-alone microgeneration systems. Electronic load implementations for self-excited induction generators are discussed in [15]. A converter-based electronic load featuring a very large operational bandwidth, specifically designed for testing computer power supplies, is presented in [16]. All the solutions rely on auxiliary circuits or systems specifically designed for the target application. While they effectively reduce the need for sophisticated, expensive commercial instrumentation, they still require significant development effort, setup time, and calibration procedures. In many industrial and academic laboratory environments, there is instead a strong demand for fast, low-cost, and effective testing solutions for low-power DC–DC converters.

Several auxiliary circuits have been proposed in industrial technical literature to simplify power supply dynamic testing. In [17–19], simple load-transient tester circuits are discussed, using an N-FET as a switch that allows current to flow through a parallel load resistance when its gate is driven on. The same approach is adopted in [20], where the performance of FET-based and BJT-based load transient tester circuits is compared, and the tester bandwidth issues are discussed. These solutions support only load transient testing and are often constrained by bandwidth, power, or measurement accuracy limits, thereby significantly reducing their effectiveness. The Feedback Injection Technique (FIT), originally proposed in [21–23], enables a standard DC–DC regulator to operate either in Dynamic Load Mode (DLM) or Dynamic Source Mode (DSM), allowing it to behave as a

dynamic load or a dynamic source for a power supply under test (PSUT). The FIT is based on the non-invasive injection of a perturbation signal into the feedback loop of the DC–DC regulator operating in DLM or DSM. This approach does not require cutting the feedback loop, does not rely on custom auxiliary circuits, and allows dynamic testing with standard laboratory instrumentation.

This paper presents the analytical models required to understand the FIT principle and its application to the dynamic testing of DC-DC power supplies. The fundamentals of the FIT are introduced in Section 2. Section 3 investigates the impact of the error amplifier implementation on FIT behavior. Sections 4 and 5 address the calculation of the operating bandwidth of DC–DC regulators in DLM and DSM. Representative applications of FIT-based dynamic testing are discussed in Section 6, while Section 7 presents experimental results obtained with both linear and switching DC power supplies.

2. DC-DC Regulators in DLM and DSM Operation

Figure 2 shows the basic schematic of a DC–DC voltage regulator. The error amplifier can be implemented using either a feedback operational amplifier or a transconductance operational amplifier, combined with the impedances Z_i and Z_f, which define the error amplifier gain. Type I, Type II, and Type III compensators are commonly adopted in the feedback control of DC power supplies [3]. These compensators are designed according to a target crossover frequency ω_c and phase margin φ_m of the loop gain.

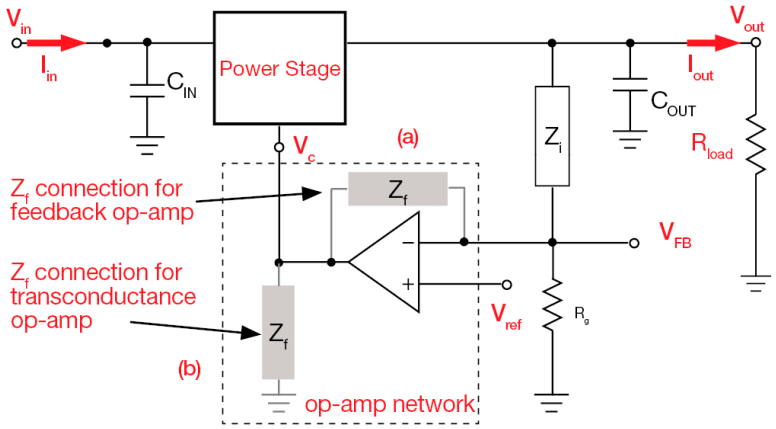


Figure 2. DC–DC voltage regulator architecture with (a) feedback operational amplifier compensation and (b) transconductance operational amplifier compensation.

The impedance Z_f introduces a pole at the origin and, in the case of Type II and Type III compensators, an additional zero–pole pair (ω_z, ω_p), given by Equation (1)

$$Z_f = \frac{\omega_0}{s}\frac{1+s/\omega_z}{1+s/\omega_p} \quad (\omega_z = \omega_p \ \text{for Type I}) \tag{1}$$

where $\omega_z = \omega_c/K$ and $\omega_p = \omega_c\, K$ for Type II, and $\omega_z = \omega_c/\sqrt{K}$ and $\omega_p = \omega_c\sqrt{K}$ for Type III. The K factor depends on the desired phase margin [24]. The impedance Z_i is a pure resistance R_i in Type I and Type II, whereas in Type III, it introduces a zero-pole couple (ω_z,ω_p) coincident with the zero and pole of Z_f, as expressed in Equation (2):

$$Z_i = R_i\frac{1+s/\omega_p}{1+s/\omega_z} \quad (\omega_z = \omega_p \ \text{for Type I and Type II}) \tag{2}$$

The DC resistance R_i of Z_i, together with the ground resistance R_g, determines the regulator's nominal output voltage V_{out}. Assuming an ideal operational amplifier, the steady-

state output voltage is given by $V_{out} = V_{ref}\ (1 + R_i/R_g)$, and the error amplifier gain is $G_{ea} = Z_f/Z_i$. Under normal operating conditions, the error amplifier adjusts the control voltage V_c such that the feedback voltage V_{FB} equals the reference voltage V_{ref}. In steady state, and in the absence of perturbations in the input voltage V_{in} or output current I_{out}, the control voltage V_c remains constant, and the output voltage V_{out} is regulated at its nominal value.

Figure 3 illustrates a DC–DC voltage regulator operating in DLM. The regulator output is terminated on a fixed load resistance R_{load}, while a waveform generator injects a signal V_j into the feedback loop through an additional resistance R_j. Under these conditions, the error amplifier senses a perturbation in the feedback voltage V_{FB} and adjusts the control voltage V_c in an attempt to restore the condition $V_{FB} = V_{ref}$. As a result, an AC component is generated at the output voltage V_{out}, which represents an inverted and scaled replica of the injected signal V_j, provided that the frequency content of V_j lies within the crossover frequency of the regulator loop gain. The PSUT regulates its own output voltage, which corresponds to the input voltage V_{in} of the DLM regulator. Consequently, the perturbation induced at V_{out} of the DLM regulator produces a corresponding perturbation in its input current I_{in}, effectively causing the regulator to behave as a dynamic load for the PSUT. The resistance R_j and the DC component of the injected voltage V_j influence both the DC operating point of the regulator and its loop gain. In particular, R_j must be selected such that the bandwidth of the injection voltage–to–input current transfer function of the DLM regulator exceeds the bandwidth of the injected signal V_j.

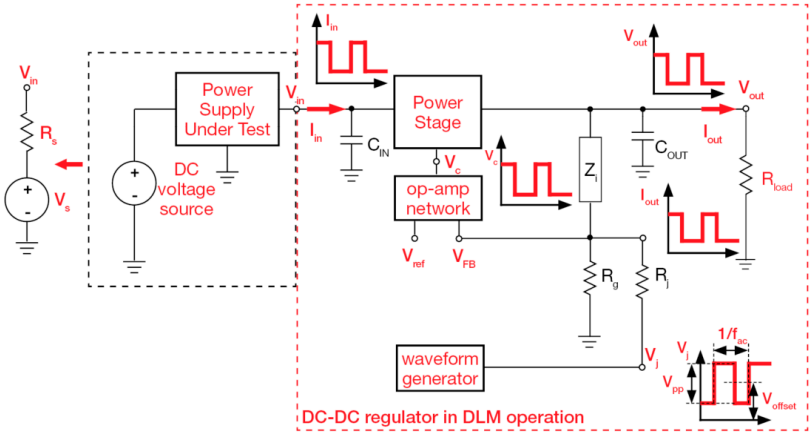


Figure 3. DC–DC voltage regulator operating in DLM with feedback signal injection.

Figure 4 shows a DC–DC voltage regulator operating in Dynamic Source Mode (DSM). In this configuration, the DSM regulator is supplied by a DC voltage source, and its output is connected to the PSUT, which is assumed to regulate its own output voltage while supplying a fixed load resistance R_{load}. The operating principle is analogous to that of the DLM configuration. In the DSM operation, the injected signal V_j, applied through the resistance R_j, produces a perturbation at the output voltage V_{out}. If the PSUT is a linear regulator, it behaves as a DC current sink, whereas if it is a switching regulator, it behaves as a DC power sink. Accordingly, the small-signal input impedance of a PSUT supplying a fixed load is theoretically infinite in the linear case, while it corresponds to a finite negative resistance in the switching case [3]. Also in the DSM operation, the resistance R_j must be selected to ensure that the bandwidth of the injection voltage–to–output voltage transfer function of the DSM regulator is wider than the bandwidth of the injected signal V_j.

The next section presents the DC analysis and the derivation of the injection voltage–to–input current gain, injection voltage-to-output voltage gain, reference voltage–to–output voltage gain, and loop gain of DC–DC regulators operating in DLM and DSM. The analysis

is carried out for both feedback and transconductance error amplifier implementations, as illustrated in Figure 2.

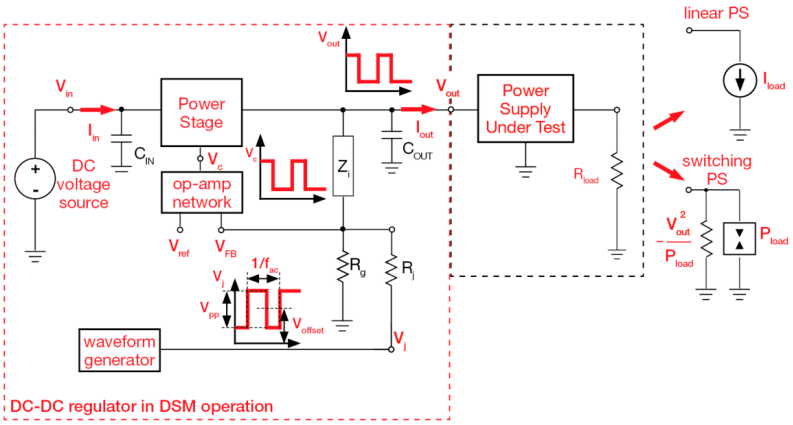


Figure 4. DC–DC voltage regulator operating in DSM with feedback signal injection.

3. Analysis of DLM and DSM Operation

3.1. Feedback Op-Amp Compensation

The output voltage of the compensation network shown in Figure 2, when a feedback operational amplifier is employed, can be expressed as in Equations (3a) and (3b):

$$V_c = A\,(V_{ref} - V_{FB}); \tag{3a}$$

$$A = A_{dc}\left(1 + \frac{A_{dc}s}{2\pi UGB}\right)^{-1} \tag{3b}$$

where A_{dc} and UGB are the DC gain and the unity-gain bandwidth of the operational amplifier, respectively. The linearized small-signal AC model of the power stage of the DC–DC regulator operating in DLM and DSM, as illustrated in Figures 3 and 4, can be written as in Equations (4a) and (4b), where the symbol "^" is conventionally adopted to represent the "small perturbation" of the relevant variable:

$$\hat{v}_{out} = G_{vi}\hat{v}_{in} + G_{vc}\hat{v}_c - Z_{out}\,\hat{i}_{out} \tag{4a}$$

$$\hat{i}_{in} = G_{ii}\hat{v}_{in} + G_{ic}\hat{v}_c + G_{iout}\hat{i}_{out} \tag{4b}$$

where $\hat{v}_{out}$, $\hat{v}_{in}$, $\hat{v}_c$, $\hat{i}_{in}$ and $\hat{i}_{out}$ represent the AC components of the output voltage, input voltage, control voltage, input current, and output current, respectively. The transfer functions G_{vi}, G_{vc}, Z_{out}, G_{ii}, G_{ic}, and G_{iout} depend on the power stage topology and component values [3], as well as on the specific operating mode (DLM or DSM). They correspond to the open-loop input-to-output voltage gain, control-to-output gain, output impedance, input admittance, control-to-input gain, and output-to-input current gain of the power supply, respectively, and are defined as in Equations (5a–f):

$$G_{vi} = \left.\frac{\hat{v}_{out}}{\hat{v}_{in}}\right|_{\substack{\hat{v}_c = 0 \\ \hat{i}_{out} = 0}} \tag{5a}$$

$$G_{vc} = \left.\frac{\hat{v}_{out}}{\hat{v}_c}\right|_{\substack{\hat{v}_{in} = 0 \\ \hat{i}_{out} = 0}} \tag{5b}$$

$$Z_{out} = -\left.\frac{\hat{v}_{out}}{\hat{i}_{out}}\right|_{\substack{\hat{v}_{in}=0 \\ \hat{v}_c=0}} \tag{5c}$$

$$G_{ii} = \left.\frac{\hat{i}_{in}}{\hat{v}_{in}}\right|_{\substack{\hat{v}_c=0 \\ \hat{i}_{out}=0}} \tag{5d}$$

$$G_{ic} = \left.\frac{\hat{i}_{in}}{\hat{v}_c}\right|_{\substack{\hat{v}_{in}=0 \\ \hat{i}_{out}=0}} \tag{5e}$$

$$G_{iout} = \left.\frac{\hat{i}_{in}}{\hat{i}_{out}}\right|_{\substack{\hat{v}_{in}=0 \\ \hat{v}_c=0}} \tag{5f}$$

The output voltage of the error amplifier network shown in Figures 3 and 4 can be expressed as in Equation (6):

$$\hat{v}_c = H_o\hat{v}_{out} + H_r\hat{v}_{ref} + H_j\hat{v}_j \tag{6}$$

where $\hat{v}_{ref}$ and $\hat{v}_j$ are the AC components of the reference voltage and the injected voltage, respectively. The coefficients H_o, H_r and H_j are obtained by analyzing the operational amplifier network of Figures 2–4 using Equation (3). These coefficients depend on the operational amplifier gain A, the impedances Z_i and Z_f, and the resistances R_g and R_j.

For a regulator operating in the DLM, the power supply under test (PSUT) can be modeled in small-signal AC analysis as a very small resistance R_s, while the DLM regulator is loaded by a resistance R_{load}, as shown in Figure 3. Conversely, for a regulator operating in DSM, the PSUT is modeled as either an infinite positive resistance (linear PSUT) or a finite negative resistance (switching PSUT), as illustrated in Figure 4.

Therefore, for the purpose of calculating the transfer functions in Equation (5), the FIT-driven regulator can be assumed to be resistively loaded in both DLM and DSM configurations. Under this assumption, the resulting closed-loop injection-to-input current gain, injection-to-output voltage gain, and reference-to-output voltage gain are given by Equations (7)–(11):

$$G_{ij}^{cl} = \left.\frac{\hat{i}_{in}}{\hat{v}_j}\right|_{\hat{v}_{in}=0,\hat{v}_{ref}=0,\hat{i}_{out}=0} = -\frac{Z_f}{R_j}G_{ic}H_A \tag{7}$$

$$G_{vj}^{cl} = \left.\frac{\hat{v}_{out}}{\hat{v}_j}\right|_{\hat{v}_{in}=0,\hat{v}_{ref}=0,\hat{i}_{out}=0} = -\frac{Z_f}{R_j}G_{vc}H_A \tag{8}$$

$$G_{vr}^{cl} = \left.\frac{\hat{v}_{out}}{\hat{v}_{ref}}\right|_{\hat{v}_{in}=0,\hat{v}_j=0,\hat{i}_{out}=0} = G_{vc}A_zH_A \tag{9}$$

$$H_A = \left(1 + G_{ea}G_{vc} + \frac{A_z}{A}\right)^{-1} \tag{10}$$

$$A_z = 1 + \frac{Z_f}{Z_i} + \frac{Z_f}{R_j} + \frac{Z_f}{R_g} \tag{11}$$

where the error amplifier gain $G_{ea} = Z_f/Z_i$ corresponds to the ideal operational amplifier case, obtained by assuming A $\to \infty$ and UGB $\to \infty$. The closed-loop injection-to-output voltage gain in Equation (8) and the reference-to-output voltage gain in Equation (9) allow the effect of the injection resistance R_j and the injected voltage V_j on the regulator output

voltage V_{out} in DLM operation to be analyzed. In DC conditions, these gains reduce to Equation (12):

$$\begin{aligned} V_{out} &= \left[\lim_{s\to 0} G_{vr}(s)\right] V_{ref} + \left[\lim_{s\to 0} G_{vj}(s)\right] V_j = \\ &= \frac{r}{1+r\lambda} V_{ref} - \frac{R_i}{R_j}\frac{1}{1+r\lambda} V_j \underset{A_{dc}\to\infty}{\cong} rV_{ref} - \frac{R_i}{R_j} V_j \end{aligned} \tag{12}$$

where

$$r = 1 + \frac{R_i}{R_g} + \frac{R_i}{R_j} \tag{13a}$$

$$\lambda = \frac{1}{G_{vc0} A_{dc}} \tag{13b}$$

$$G_{vc0} = \lim_{\omega\to 0} G_{vc} \tag{13c}$$

and G_{vc0} is the DC value of the control-to-output gain, which depends on the power stage topology [3].

Equation (12) shows that, for $V_j \leq 0$, the DC output voltage increases with respect to normal operation, as the factor r becomes larger than $1 + R_i/R_g$, whereas for $V_j > 0$, the DC output voltage decreases. Equation (12) also defines the admissible range of the injected voltage V_j required to maintain proper operation of the DC–DC regulator, depending on its step-up or step-down characteristics, as expressed by Equations (14) and (15):

$$V_{out} < V_{in} \Rightarrow V_j > \frac{R_j}{R_i}\left(rV_{ref} - V_{in}\right) \quad \text{step-down} \tag{14}$$

$$V_{out} > V_{in} \Rightarrow V_j < \frac{R_j}{R_i}\left(rV_{ref} - V_{in}\right) \quad \text{step-up} \tag{15}$$

The voltage V_j can therefore be interpreted as an external reference that allows controlled modification of the DC output voltage V_{out}. For given values of R_i, R_j, R_g and V_{ref}, the value of V_j required to obtain a desired output voltage V_{out} is given by Equation (16):

$$V_j = \frac{R_j}{R_i}\left[rV_{ref} - (1+r\lambda)V_{out}\right] \underset{A_{dc}\to\infty}{\cong} \frac{R_j}{R_i}\left(rV_{ref} - V_{out}\right) \tag{16}$$

The resulting loop-gain T of the circuit in Figure 3 can be written as:

$$T = G_{vc}\left.\frac{\hat{v}_c}{\hat{v}_{out}}\right|_{\hat{v}_{in}=0,\hat{v}_j=0,\hat{v}_{ref}=0} = G_{vc}G_{ea}\left(1 + \frac{A_z}{A}\right)^{-1} \tag{17}$$

The impact of the injection resistance R_j on the loop gain is determined by the ratio A_z/A. By letting $R_j \to \infty$ in Equation (11), the loop gain of the regulator without the injection resistance is obtained as:

$$T_0 = G_{vc}\left.\frac{\hat{v}_c}{\hat{v}_{out}}\right|_{\hat{v}_{in}=0,\hat{v}_j=0,\hat{v}_{ref}=0,R_j=\infty} = G_{vc}G_{ea}\left(1 + \frac{A_{z0}}{A}\right)^{-1} \tag{18}$$

$$A_{z0} = \lim_{R_j\to\infty} A_z = 1 + \frac{Z_f}{Z_i} + \frac{Z_f}{R_g} \tag{19}$$

From Equations (17) and (18), it follows that:

$$T = T_0\left(1 + \frac{Z_f}{R_j}\frac{1}{A + A_{z0}}\right)^{-1} \tag{20}$$

Equations (7), (8) and (20) provide practical guidelines for selecting the value of R_j to achieve the desired closed-loop injection-to-input or injection-to-output gain. Equation (20) also shows that the influence of the injection resistance R_j on the magnitude and phase of the loop gain is limited, owing to the high open-loop gain of the operational amplifier.

3.2. Trans-Conductance Op-Amp Compensation

When the error amplifier is implemented by means of a transconductance operational amplifier, the output voltage of the compensation network shown in Figure 2 can be expressed as in Equations (21a) and (21b):

$$V_c = G_m Z_f (V_{ref} - V_{FB}) \tag{21a}$$

$$G_m = gm_{dc}\left(1 + \frac{s}{\omega_B}\right)^{-1} \tag{21b}$$

where gm_{dc} and ω_B are the DC transconductance and the bandwidth of the operational amplifier, respectively. Under closed-loop operation, the output voltage of the error amplifier network can still be formally written as in Equation (6). In this case, however, the coefficients H_o, H_r and H_j are obtained by analyzing the operational amplifier network of Figures 2–4 using Equation (21). These coefficients depend on the transconductance gain G_m, the impedances Z_i, Z_f, and the resistances R_g and R_j. As in the case of feedback operational amplifiers, the FIT-driven regulator can be assumed to be resistively loaded in both DLM and DSM configurations for the purpose of deriving the transfer functions in Equation (5). Under this assumption, the resulting closed-loop injection-to-input current gain, injection-to-output voltage gain, and reference-to-output voltage gain are given by Equations (22)–(26):

$$G_{ij}^{cl} = -G_{ic} G_m Z_f H_{ig} H_m \tag{22}$$

$$G_{vj}^{cl} = -G_{vc} G_m Z_f H_{ig} H_m \tag{23}$$

$$G_{vr}^{cl} = G_{vc} G_m Z_f H_m \tag{24}$$

$$H_m = \left(1 + G_{vc} G_m Z_f H_{jg}\right)^{-1} \tag{25}$$

$$H_{jg} = \left(1 + \frac{Z_i}{R_g} + \frac{Z_i}{R_j}\right)^{-1} \tag{26}$$

$$H_{ig} = \left(1 + \frac{R_j}{R_g} + \frac{R_j}{Z_i}\right)^{-1} \tag{27}$$

The effect of the injected voltage V_j on the DC output voltage V_{out} can be evaluated by means of the closed-loop injection-to-output gain in Equation (23) and the reference-to-output gain in Equation (24). In DC conditions, the output voltage can be expressed as

$$V_{out} = \left[\lim_{s\to 0} G_{vr}(s)\right] V_{ref} + \left[\lim_{s\to 0} G_{vj}(s)\right] V_j = r V_{ref} - \frac{R_i}{R_j} V_j \tag{28}$$

where the factor r is defined as in Equation (13).

A comparison between Equations (12) and (28) shows that a real transconductance operational amplifier with finite bandwidth produces the same qualitative effect on the DC output voltage as an ideal feedback operational amplifier. Given R_i, R_j, R_g, and V_{ref}, the DC

component of the injected voltage V_j can be used to adjust the DC output voltage V_{out}. The value of V_j required to obtain a desired output voltage is given by Equation (29):

$$V_j = \frac{R_j}{R_i}\left(rV_{ref} - V_{out}\right) \tag{29}$$

The resulting loop gain of the regulator operating in DLM can be written as in Equation (30):

$$T = G_{vc}\left.\frac{\hat{v}_c}{\hat{v}_{out}}\right|_{\hat{v}_{in}=0,\hat{v}_j=0,\hat{v}_{ref}=0} = G_{vc}G_mZ_fH_{jg} \tag{30}$$

In this case, the impact of the resistance R_j on the loop gain is determined by the ratio Z_i/R_j through the coefficient H_{jg}. By letting $R_j \to \infty$ in Equation (26), the loop gain of the regulator without the injection resistance is obtained as

$$T_0 = G_{vc}\left.\frac{\hat{v}_c}{\hat{v}_{out}}\right|_{\hat{v}_{in}=0,\hat{v}_j=0,\hat{v}_{ref}=0,R_j=\infty} = G_{vc}G_mZ_fH_{jg0} \tag{31}$$

$$H_{jg0} = \frac{R_g}{R_g + Z_i} \tag{32}$$

From Equations (30) and (31), it follows that:

$$T = T_0\frac{H_{jg}}{H_{jg0}} = T_0\left(1 + \frac{Z_i}{R_j}H_{jg0}\right)^{-1} \tag{33}$$

Equations (22) and (33) can be used to select the value of the injection resistance R_j such that the desired closed-loop injection-to-input gain is achieved while maintaining the loop crossover frequency and phase margin within acceptable limits. Equation (33) also shows that when the error amplifier is implemented with a Type I or Type II compensation network and a transconductance operational amplifier, as is typical in current-mode controlled regulators, the impedance Z_i reduces to the resistance R_i. In this case, Equation (33) simplifies to Equation (34):

$$T = T_0\frac{H_{jg}}{H_{jg0}} = T_0\left[1 + \frac{R_iR_g}{R_j(R_i + R_g)}\right]^{-1} \tag{34}$$

A comparison between Equations (20) and (34) shows that the injection resistance R_j has a more pronounced effect on the magnitude of the loop gain when a transconductance operational amplifier is used than when a feedback operational amplifier is employed. At the same time, this dependence is more straightforward to predict analytically.

4. Injection-to-Input Bandwidth in DLM

In this section, the DLM is analyzed with reference to a buck converter. Analytical expressions are derived to determine the bandwidth of the injection-to-input current gain. Both voltage-mode control with a Type III compensator and peak current-mode control with a Type II compensator are considered.

4.1. Voltage-Mode DLM Regulator

The resistances R_i and R_g of the feedback voltage divider are selected to achieve the desired steady-state average output voltage, $V_{out} = V_{ref}(1 + R_i/R_g)$. Equations (1) and (2) define the impedances Z_i and Z_f of the feedback compensator needed to achieve a specified crossover frequency f_c and phase margin φ_m. The zero ω_z and pole ω_p of the compensator

are determined using standard controller design techniques applied to the voltage-mode control-to-output transfer function $G_{vc,vm}$ [3,24]. The resulting injection-to-input current gain of the DLM regulator is governed by the compensator impedances Z_i and Z_f, the grounding resistance R_g and the injection resistance R_j. The bandwidth of the injection-to-input gain can be evaluated by combining Equations (7), (10) and (17), which yields Equation (35):

$$G_{ij}^{cl} = -\frac{Z_i}{R_j}\frac{G_{ic,vm}}{G_{vc,vm}}\frac{T}{1+T} \xrightarrow[frequency]{low} -\frac{R_i}{R_j}\frac{G_{ic,vm}}{G_{vc,vm}} \tag{35}$$

Equation (35) shows that the low-frequency injection-to-input gain is determined by the ratio $G_{ic,vm}/G_{vc,vm}$ of the voltage-mode control-to-input ($G_{ic,vm}$) and voltage-mode control-to-output $G_{vc,vm}$ transfer functions, respectively. This behavior can be explained by observing that the impedance Z_i introduces a zero–pole pair around the loop crossover frequency, while the ratio Z_i/R_j reduces to R_i/R_j at low frequency. Moreover, since the loop gain T is much larger than unity below the crossover frequency, the factor $T/(1+T)$ approaches unity in the low-frequency range of interest.

The ratio $G_{ic,vm}/G_{vc,vm}$ can be derived using the averaged state-space model of the buck converter [3], leading to Equation (36):

$$\frac{G_{ic,vm}}{G_{vc,vm}} = \frac{G_{PWM}}{Z_{load}}\left[D + \frac{I_{out}}{V_{in}}(sL + Z_{load})\right] \tag{36}$$

where $G_{PWM} = \hat{d}/\hat{v}_c$ is the PWM modulator gain, which defines the proportionality between the AC component of the duty cycle and the AC component of the control voltage, and Z_{load} is the equivalent impedance of the output capacitor and load connected in parallel.

A simplified expression for the low-frequency behavior of the ratio $G_{ic,vm}/G_{vc,vm}$ can be obtained by neglecting the equivalent series resistance (ESR) of the output capacitor. This approximation is justified because the ESR introduces a high-frequency zero that does not affect the low-frequency range relevant to the determination of the injection-to-input bandwidth. Under this assumption, the ratio for a buck converter reduces to Equation (37):

$$\left.\frac{G_{ic,vm}}{G_{vc,vm}}\right|_{LF} = 2\frac{I_{out}}{V_{in}} + \frac{I_{out}^2 L + C_{out}V_{out}^2}{V_{in}V_{out}}s + \frac{C_{out}I_{out}L}{V_{in}}s^2 \tag{37}$$

The zeros of Equation (37) are given by Equation (38):

$$\omega_{ij} = -\frac{L + C_{out}R_{load}^2 \pm \sqrt{L^2 + C_{out}^2 R_{load}^4 - 6C_{out}LR_{load}^2}}{2LC_{out}R_{load}} \tag{38}$$

The lowest frequency among the values given by Equation (38) corresponds to the bandwidth of the injection-to-input gain of the voltage-mode controlled buck regulator operating in DLM.

4.2. Current-Mode DLM Regulator

The analysis of Dynamic Load Mode (DLM) operation under current-mode control follows the same approach adopted for voltage-mode control. The main difference lies in the design of the feedback compensator, whose zero ω_z and pole ω_p are now determined based on the current-mode control-to-output transfer function $G_{vc,cm}$ [3]. The bandwidth

of the injection-to-input current gain for a current-mode controlled regulator operating in DLM can be obtained by combining Equations (22), (25) and (30), resulting in Equation (39):

$$G_{ij}^{cl} = -\frac{Z_i}{R_j}\frac{G_{ic,cm}}{G_{vc,cm}}\frac{T}{1+T} \xrightarrow[\text{frequency}]{\text{low}} -\frac{R_i}{R_j}\frac{G_{ic,cm}}{G_{vc,cm}} \tag{39}$$

Equation (39) is formally identical to Equation (35), derived for voltage-mode control. This indicates that the low-frequency injection-to-input bandwidth is primarily determined by the power stage dynamics rather than by the control strategy. In fact, the two ratios $G_{ic,vm}/G_{vc,vm}$ and $G_{ic,cm}/G_{vc,cm}$ are proportional to each other. The PWM modulator equation for peak current-mode control can be expressed as Equation (40):

$$\hat{d} = F_m\left(\hat{v}_c - A_s\hat{i}_L - F_v\hat{v}_{out} - F_g\hat{v}_{in}\right) \tag{40}$$

where A_s is the current sensing gain, and the coefficients F_m, F_v, and F_g depend on the converter topology, as detailed in [25]. By applying the modulator model in Equation (40) together with the averaged small-signal model of the buck converter [3], the ratio $G_{ic,cm}/G_{vc,cm}$ is obtained as Equation (41):

$$\frac{G_{ic,cm}}{G_{vc,cm}} = \frac{F_m}{Z_{load}}\left[D + \frac{I_{out}}{V_{in}}(sL + Z_{load})\right] \tag{41}$$

Equation (41) is identical to Equation (36) except for the factor F_m, which replaces the voltage-mode PWM gain G_{PWM}. As a consequence, the bandwidth of the injection-to-input gain in DLM operation is independent of whether voltage-mode or current-mode control is adopted, and it is instead determined solely by the components and dynamics of the converter power stage.

Therefore, both voltage-mode and current-mode regulators can be effectively employed in FIT-based DLM operation, since the achievable injection-to-input bandwidth is fundamentally limited by the converter power stage.

5. Injection-to-Output Bandwidth in DSM

As previously highlighted, when a DC–DC regulator operates in DSM during line transient testing, its load is represented as a DC current sink if the PSUT is linear, or as a DC power sink if the PSUT is switching.

The input capacitor of the PSUT plays an important role in determining the line transient response and, therefore, influences the small-signal model to be adopted for the analysis of the regulator operating in DSM. In practical line transient tests, the dynamic source and the PSUT are usually connected through very short cables. Under these conditions, the input capacitor of the PSUT can be considered effectively in parallel with the output capacitor of the DSM regulator, and thus incorporated into its equivalent output network. On the other hand, if the PSUT's inherent input noise rejection capability must be evaluated, the PSUT input capacitor should be disconnected and neglected in the DSM regulator analysis.

Therefore, the following operating conditions apply.

- If the PSUT is linear, it behaves as a DC current sink drawing a constant current I_{load}, and its small-signal AC model corresponds to an open circuit.
- If the PSUT is switching, it behaves as a DC power sink drawing a constant power P_{load}, and its small-signal AC model can be represented by a negative resistance $R_{dyn} = -V_{out}{}^2/P_{load}$, where V_{out} is the average DC output voltage of the DC–DC regulator operating in DSM.

In the following subsections, voltage-mode and current-mode controlled buck regulators operating in DSM are analyzed with reference to both linear and switching PSUT configurations.

5.1. Voltage-Mode DSM Regulator-Linear PSUT

Feedback operational amplifiers are typically employed in voltage-mode control architectures. The bandwidth of the injection-to-output voltage gain for a voltage-mode controlled regulator operating in DSM with a linear PSUT can be obtained by combining Equations (8), (10) and (17), which yields Equation (42):

$$G_{vj}^{cl} = -\frac{Z_i}{R_j}\frac{T}{1+T} \xrightarrow[frequency]{low} -\frac{Z_i}{R_j} \tag{42}$$

Unlike the injection-to-input case discussed in Section 4, the impedance Z_i is not reduced to its resistive component R_i in Equation (42). In fact, the ratio $G_{ic,vm}/G_{vc,vm}$, whose bandwidth is lower than the zero ω_Z introduced by Z_i, does not appear in the DSM injection-to-output formulation. As a result, since the closed-loop factor $T/(1+T)$ approaches unity below the loop crossover frequency ω_c, the bandwidth of the injection-to-output gain in DSM operation with a linear PSUT is mainly determined by the zero ω_z introduced by the compensator impedance Z_i. Therefore, in voltage-mode DSM operation, the compensation network directly sets the achievable bandwidth of the injection-to-output transfer function.

5.2. Current-Mode DSM Regulator-Linear PSUT

Transconductance operational amplifiers are most commonly adopted in current-mode controlled regulators. In the DSM operation, the resulting loop gain is significantly influenced by the injection resistance R_j, as indicated by Equation (34). In particular, the loop crossover frequency decreases as R_j is reduced. By combining Equations (23), (25) and (30), the closed-loop injection-to-output voltage gain for a current-mode controlled regulator operating in DSM with a linear PSUT can be expressed as Equation (43)

$$G_{vj}^{cl} = -\frac{Z_i}{R_j}\frac{T}{1+T} \xrightarrow[frequency]{low} \begin{cases} -\frac{Z_i}{R_j} & if\ \omega_Z < \omega_c \\ -\frac{R_i}{R_j}\frac{T}{1+T} & if\ \omega_c < \omega_Z \end{cases} \tag{43}$$

Equation (43) highlights that the bandwidth of the injection-to-output gain in this configuration is determined by the minimum between the compensator zero frequency ω_z and the actual loop crossover frequency ω_c. Unlike the nominal crossover frequency, the effective value of ω_c depends on the injection resistance R_j.

Therefore, in DSM operation with a linear PSUT, current-mode control introduces an additional sensitivity of the injection-to-output bandwidth to the choice of R_j. This contrasts with the voltage-mode case, where R_j primarily affects the DC gain but has a limited impact on bandwidth.

5.3. Voltage-Mode DSM Regulator-Switching PSUT

When the PSUT is a switching regulator, its small-signal dynamic model corresponds to a negative resistance, namely $R_{dyn} = -{V_{out}}^2/P_{load}$, where P_{load} is the constant power delivered to the load. The presence of this negative input resistance can significantly influence the stability of the DC–DC regulator operating in DSM.

For a voltage-mode controlled buck converter in DSM, the poles of the control-to-output transfer function are given by Equations (44) and (45):

$$\omega_{vc}^{vm} = \frac{P_{load}L - C_{out}ESR_{out}V_{out}^2 \pm \Delta}{2LC_{out}V_{out}^2} \tag{44}$$

$$\Delta = \sqrt{\left(P_{load}L - C_{out}ESR_{out}V_{out}^2\right)^2 - 4C_{out}LV_{out}^4} \tag{45}$$

The poles defined in Equation (44) remain in the left half of the complex plane (LHP) only below a threshold value of P_{load}, which depends on the DC output voltage V_{out} and on the parameters C_{out} and ESR_{out}. These parameters are determined by the parallel combination of the output capacitor of the DSM regulator and the input capacitor of the PSUT. This behavior is associated with the well-known instability issue of switching power supplies operating under constant-power load conditions [26,27]. Nevertheless, even if the control-to-output poles move into the right half plane (RHP), the voltage-mode controlled regulator operating in DSM with a switching PSUT can still remain stable, provided that the poles of the closed-loop factor $T/(1+T)$, which determines the injection-to-output gain in Equation (42), remain in the LHP. Under these conditions, the bandwidth of the injection-to-output gain is still determined by Equation (42) and corresponds to the frequency ω_z of the zero introduced by the error amplifier compensation network.

5.4. Current-Mode DSM Regulator-Switching PSUT

The stability analysis of a current-mode controlled buck converter operating in DSM with a switching PSUT can be performed using a simplified model of the current-mode regulator. In the low-frequency range, the approximation $i_L \approx v_c/A_{sns}$ is well satisfied [3]. Under this assumption, the control-to-output transfer function reduces to a first-order system characterized by a single real pole located at the frequency

$$\omega_{vc}^{cm} = \frac{P_{load}}{C_{out}(V_{out}^2 - ESR_{out}P_{load})} \tag{46}$$

The pole given in Equation (46) remains in the LHP only above a threshold value of the load power P_{load} threshold $V^2{}_{out}/ESR_{out}$. This condition, however, is generally not feasible, as it would imply operation beyond the regulator's rated load capability. Nevertheless, also in this case, stability of the overall DSM configuration can still be ensured provided that the poles of the closed-loop factor $T/(1+T)$, which determines the injection-to-output gain in Equation (43), remain in the LHP. Therefore, even though the loop gain T may exhibit RHP poles due to the negative input resistance of the switching PSUT, the cascade connection of the two power supplies can remain stable if the closed-loop injection response is properly shaped.

The stability considerations discussed above for DSM regulators with both linear and switching PSUTs can also be extended to PSUTs loaded by DLM regulators, provided that the appropriate dynamic model of the interconnected system is used.

In summary, the achievable injection-to-output bandwidth in DSM operation depends on both the compensation network and the interaction with the PSUT, especially in the presence of constant-power load effects.

6. Voltage-Mode Versus Current-Mode Control in DLM

6.1. Voltage-Mode DLM Regulator

Figure 5 shows a voltage-mode controlled buck regulator operating in DLM. The power circuit parameters of this buck regulator are taken from the documentation for the TI-PMLK BUCK board [28]. The feedback control is implemented using a feedback

operational amplifier with a DC gain $A_{dc} = 10^5$ and a unity-gain bandwidth UGB = 5 MHz. The error amplifier is designed to achieve a phase margin of at least 52° at a crossover frequency of 20 kHz, while ensuring at least 20° of phase shift below the crossover frequency. Assuming R_g = 10 kΩ, the standard compensator design procedures discussed in [24] were used for the DC–DC voltage-mode buck regulator under analysis (Figure 5) to yield a Type III compensator with the following commercial component values: R_{i1} = 31.6 kΩ, C_f = 150 pF, C_{f2} = 3.3 nF, R_{f2} = 10.7 kΩ, C_{i2} = 1.0 nF, R_{i2} = 1.69 kΩ.

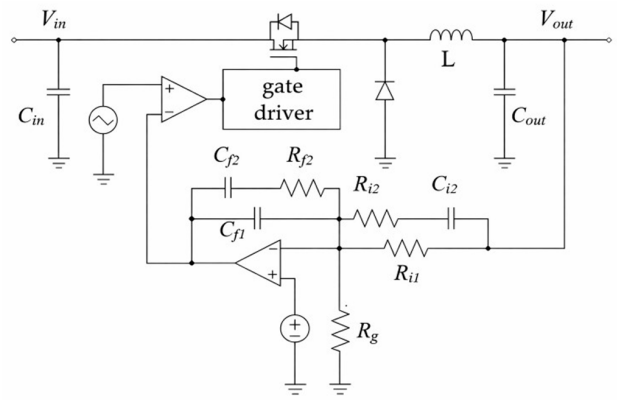
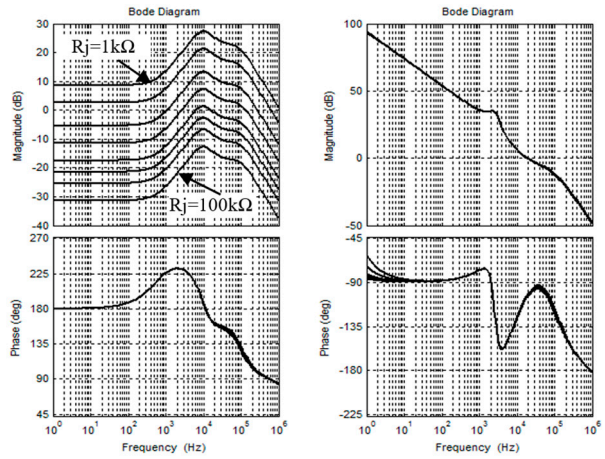


Figure 5. DC–DC voltage-mode buck regulator, with V_{in} = 36 V, V_{out} = 3.3 V, I_{out} = 1.5 A, f_s = 500 kHz, C_{out} = 220 µF/25 mΩ, L = 18 µH/78 mΩ, V_{ref} = 0.8 V.

The voltage-mode DLM regulator model illustrated in the previous section has been implemented in a MATLAB 2025 script. The resulting Bode plots of the injection-to-input gain and the loop gain are reported in Figure 6 for injection resistance values R_j ranging from 1 kΩ to 100 kΩ. The plots in Figure 6a show that the injection-to-input gain bandwidth is approximately 700 Hz. The resistance R_j primarily affects the magnitude of the injection-to-input gain, with limited impact on bandwidth. The loop gain plots in Figure 6b indicate that the crossover frequency remains close to 20 kHz, with a phase margin greater than 52°, due to the additional 20° phase shift introduced below the crossover frequency. Based on the circuit parameters, Equation (38) predicts a low-frequency zero of the injection-to-input gain at 670 Hz, which is in good agreement with the results shown in Figure 6. Finally, Figure 6b confirms that the injection resistance R_j does not significantly affect the regulator's stability, as its primary influence is on the DC bias point rather than the loop dynamics.



(**a**) (**b**)

Figure 6. Bode plots of (**a**) injection-to-input gain and (**b**) loop gain of the voltage-mode buck regulator in DLM for different values of the injection resistance, namely R_j = {1 kΩ, 2 kΩ, 5 kΩ, 10 kΩ, 20 kΩ, 31.6 kΩ, 50 kΩ, 100 kΩ}.

6.2. Current-Mode Controlled DLM Regulator

Figure 7 shows a peak-current-mode-controlled buck regulator operating in DLM. The power circuit parameters of this buck regulator are taken from the documentation for the TI-PMLK BUCK board [28], which is used in the experiments discussed in Section 8. The inner current loop is assumed to be implemented with a sensing gain A_{sns} = 180 mΩ and a compensation ramp of amplitude V_a = 487 mV. The feedback control is based on a transconductance operational amplifier with a DC transconductance $g_{m,\text{dc}}$ = 97 S and a frequency bandwidth ω_B = 17 Mrad/s. The error amplifier is designed to achieve a phase margin of at least 52° at a crossover frequency of 20 kHz. In this case, a Type II compensator is sufficient to meet the design requirements. Assuming R_g = 10 kΩ, the compensator design procedure described in [24] yields the following commercial component values: R_{i1} = 31.6 kΩ, C_{f1} = 4 pF, C_{f2} = 100 pF, R_{f2} = 280 kΩ. The Bode plots of the injection-to-input gain and the loop gain are shown in Figure 8 for injection resistance values R_j ranging from 1 kΩ to 100 kΩ.

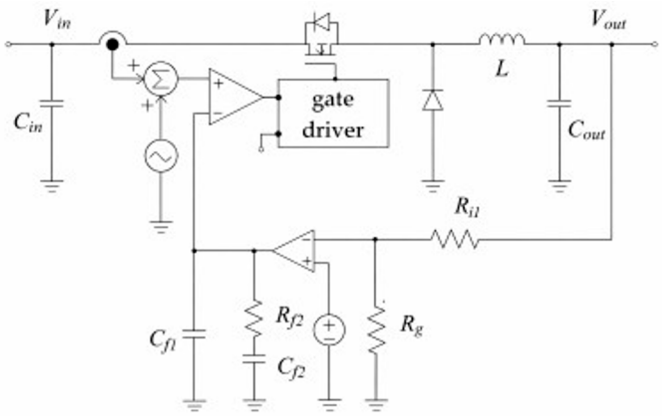
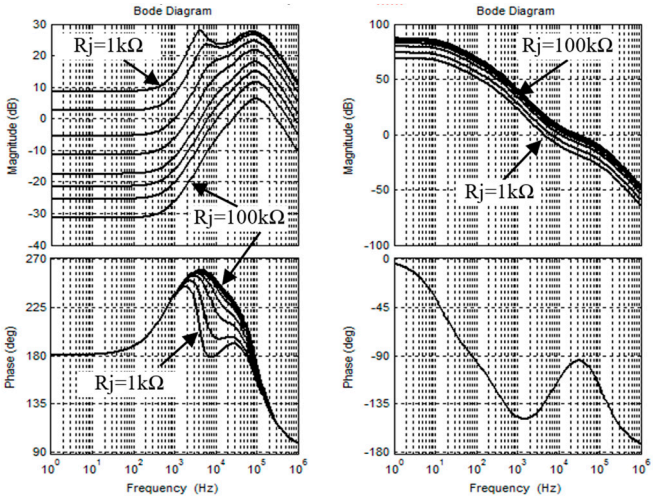


Figure 7. DC–DC current-mode buck regulator, with V_{in} = 36 V, V_{out} = 3.3 V, I_{out} = 1.5 A, f_s = 500 kHz, C_{out} = 220 µF/25 mΩ, L = 18 µH/78 mΩ, V_{ref} = 0.8 V.



(**a**) (**b**)

Figure 8. Bode plots of (**a**) injection-to-input gain and (**b**) loop of the current-mode buck regulator in DLM for different values of the injection resistance, namely R_j = {1 kΩ, 2 kΩ, 5 kΩ, 10 kΩ, 20 kΩ, 31.6 kΩ, 50 kΩ, 100 kΩ}.

The plots in Figure 8a indicate that the injection-to-input gain bandwidth is again approximately 700 Hz, matching the result obtained for voltage-mode control. This confirms that the injection-to-input bandwidth is determined by the ratio G_{ic}/G_{vc}, which depends

on the converter power stage and is independent of the control method, as shown in Equation (41). For completeness, the Bode plot of the ratio G_{ic}/G_{vc} for the buck converter under study is reported in Figure 9. In contrast to the voltage-mode case, the injection resistance R_j has a stronger impact on the loop gain under current-mode control. The plots in Figure 8b show that the loop crossover frequency decreases from 20 kHz down to approximately 4 kHz as R_j is reduced from 100 kΩ to 1 kΩ. As a consequence, the phase margin is also reduced. This erosion of phase margin is reflected in Figure 8a, where a resonance peak appears in the magnitude of the injection-to-input gain near the crossover frequency when R_j decreases to 1 kΩ.

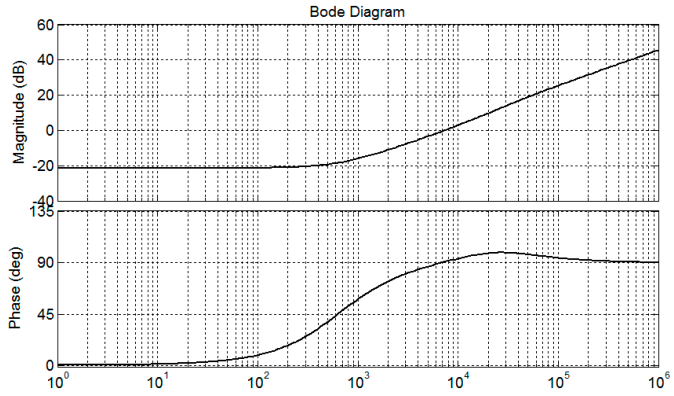


Figure 9. Frequency response of the ratio G_{ic}/G_{vc} for the buck converter under study.

These results highlight the following key observations.

- The bandwidth of the injection-to-input gain of a DC–DC regulator operating in DLM is fundamentally determined by the power stage dynamics.
- Since the bandwidth is fixed by the converter itself, DLM operation can be implemented using either voltage-mode or current-mode regulators without affecting the achievable injection-to-input bandwidth in the low-frequency range.
- The sensitivity of the loop gain to the injection resistance R_j is significantly lower in voltage-mode control using a Type III compensator and feedback operational amplifier than in current-mode control using a Type II compensator and transconductance operational amplifier, in agreement with Equations (20) and (34).
- DLM operation does not compromise the stability of the regulator, since the loop gain poles remain in the left half plane.

7. Voltage-Mode Versus Current-Mode Control in DSM

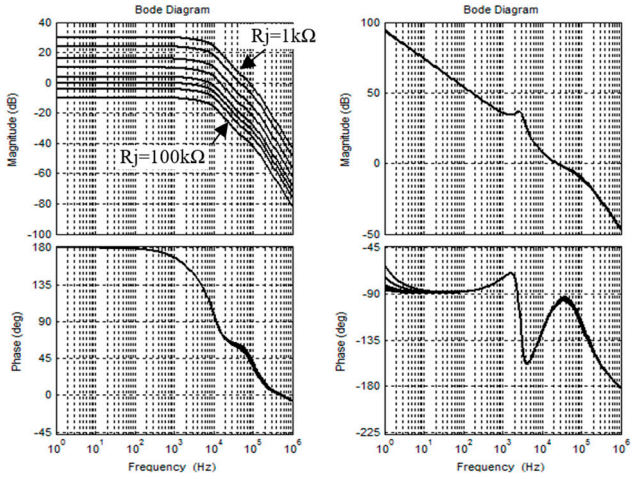
7.1. Voltage-Mode DSM Regulator-Linear PSUT

Figure 10 shows the Bode plots of the injection-to-output gain and the loop gain for the voltage-mode controlled buck regulator operating in DSM with a linear PSUT. The plots in Figure 10a indicate that the injection-to-output gain bandwidth is approximately 4.5 kHz, which is significantly larger than the injection-to-input bandwidth previously calculated for DLM operation.

As in the DLM case, the injection resistance R_j mainly affects the magnitude of the injection-to-output gain, while its influence on the bandwidth remains limited. The loop gain plots in Figure 10b confirm that the crossover frequency remains close to 20 kHz and that the phase margin is greater than 52°, due to the additional 20° phase shift below the crossover frequency.

According to Equation (42), the low-frequency pole that determines the bandwidth of the injection-to-output gain in DSM operation with a linear PSUT corresponds to the

zero ω_z introduced by the impedance Z_i. For the Type III compensator considered in this example, this zero occurs at approximately 4.5 kHz, in good agreement with the results reported in Figure 10.

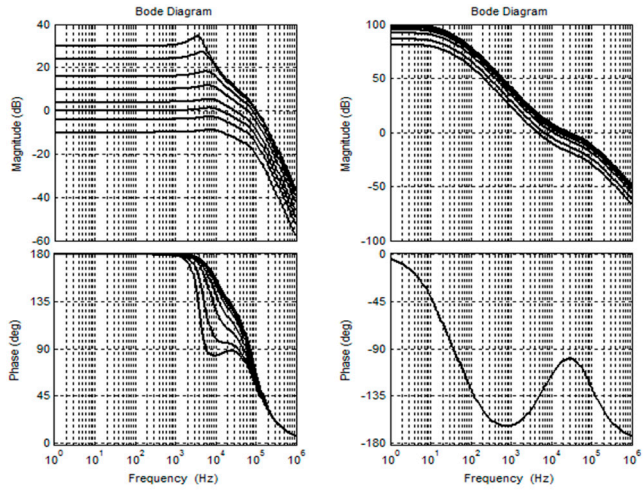


(**a**) (**b**)

Figure 10. Bode plots of (**a**) injection-to-output gain and (**b**) loop gain of the voltage-mode buck regulator operating in DSM with a linear PSUT, for R_j = {1 kΩ, 2 kΩ, 5 kΩ, 10 kΩ, 20 kΩ, 31.6 kΩ, 50 kΩ, 100 kΩ}.

7.2. Current-Mode DSM Regulator-Linear PSUT

Figure 11 shows the Bode plots of the injection-to-output gain and the loop gain for the current-mode controlled buck regulator operating in DSM with a linear PSUT. The plots in Figure 11a show that the injection-to-output gain bandwidth varies with the injection resistance R_j. The loop gain plots in Figure 11b confirm that the crossover frequency decreases significantly as R_j is reduced. In particular, the crossover frequency drifts from approximately 20 kHz down to about 4 kHz when R_j decreases from 100 kΩ to 1 kΩ. Therefore, in DSM operation with a linear PSUT, the injection resistance R_j not only affects the gain magnitude but also directly influences the achievable injection-to-output bandwidth under current-mode control.

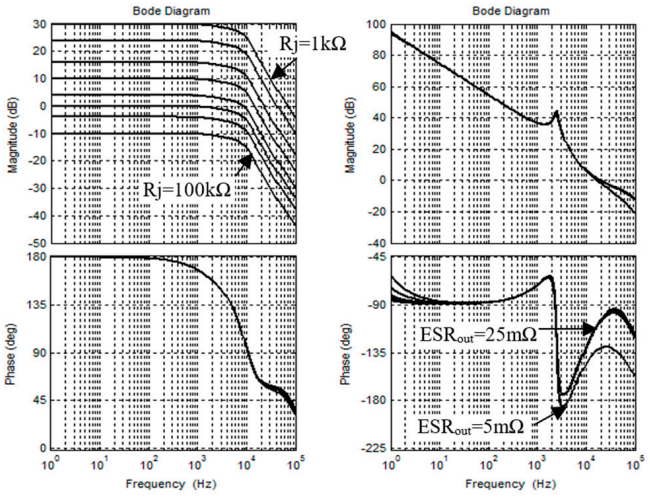


(**a**) (**b**)

Figure 11. Bode plots of (**a**) injection-to-output gain and (**b**) loop gain of the current-mode buck regulator operating in DSM with a linear PSUT, for R_j = {1 kΩ, 2 kΩ, 5 kΩ, 10 kΩ, 20 kΩ, 31.6 kΩ, 50 kΩ, 100 kΩ}.

7.3. Voltage-Mode DSM Regulator-Switching PSUT

Figure 12 shows the Bode plots of the injection-to-output gain and the loop gain obtained for the voltage-mode controlled buck regulator operating in DSM while supplying a switching PSUT. In this example, the operating point corresponds to I_{out} = 1.5 A at V_{out} = 3.3 V, resulting in a load power of P_{load} = 4.95 W. The bandwidth of the injection-to-output gain can be determined according to Equation (42) and is equal to the frequency ω_z of the zero introduced by the feedback error amplifier. This behavior is clearly evident in the plots shown in Figure 12a. The loop gain plots in Figure 12b show that, for a given combination of P_{load}, V_{out}, and C_{out}, the equivalent series resistance ESR_{out} plays a critical role in determining the location of the control-to-output poles.



(**a**) (**b**)

Figure 12. Bode plots of (**a**) injection-to-output gain and (**b**) loop gain of the voltage-mode buck regulator operating in DSM with a switching PSUT, for R_j = {1 kΩ, 2 kΩ, 5 kΩ, 10 kΩ, 20 kΩ, 31.6 kΩ, 50 kΩ, 100 kΩ}.

In this case study, an output capacitor with an ESR value of 25 mΩ produces a positive phase shift, ensuring that the poles remain in the LHP. Conversely, a lower ESR value of 5 mΩ introduces a negative phase shift that causes the poles to drift into the right half plane (RHP). Therefore, the operation of a DC–DC regulator in DSM with a switching PSUT may involve right-half-plane poles in the control-to-output dynamics, depending on the parameters P_{load}, V_{out}, C_{out}, and ESR_{out}. Nevertheless, even in the presence of RHP poles, the voltage-mode DSM regulator can remain stable provided that the poles of the closed-loop factor $T/(1 + T)$, which governs the injection-to-output response, remain in the LHP, as observed in this example.

7.4. Current-Mode DSM Regulator-Switching PSUT

In the current-mode case, the loop gain may exhibit right-half-plane poles due to the negative input resistance of the switching PSUT. Nevertheless, as discussed in Section 5, the overall DSM configuration remains stable as long as the poles of the closed-loop factor $T/(1+T)$, which determines the injection-to-output response, remain in the LHP.

Figure 13 shows the Bode plots of the injection-to-output gain and the loop gain for the current-mode controlled DSM buck regulator supplying a switching PSUT. In this case, the negative phase shift in the loop gain is due to a pole in the RHP.

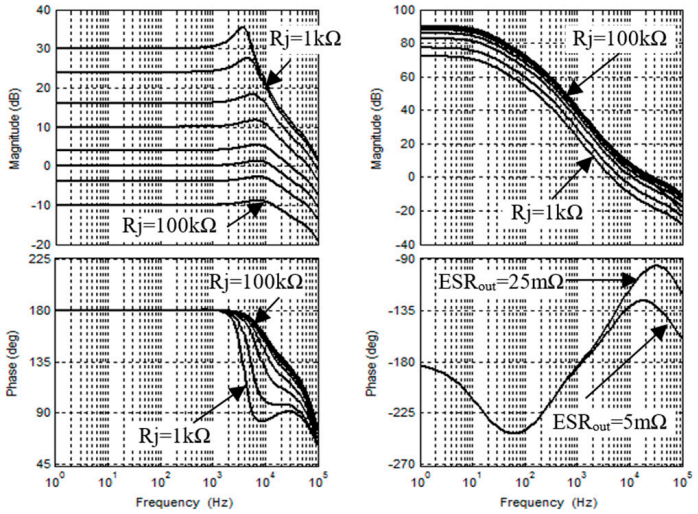


Figure 13. Bode plots of (**a**) injection-to-output gain and (**b**) loop gain of the current-mode buck regulator operating in DSM with a switching PSUT, for R_j = {1 kΩ, 2 kΩ, 5 kΩ, 10 kΩ, 20 kΩ, 31.6 kΩ, 50 kΩ, 100 kΩ}.

The previous analysis highlights the following main points:

- The bandwidth of the injection-to-output gain of a DC–DC regulator operating in DSM with a linear PSUT is determined by the compensation network and depends on the adopted control strategy.
- In the DSM operation with a linear PSUT under current-mode control, the injection resistance R_j affects not only the DC gain but also the injection-to-output bandwidth. In contrast, under voltage-mode control, R_j mainly impacts the DC gain.
- The operation of a DC–DC regulator in DSM with a linear PSUT does not compromise stability, since the poles of the loop gain remain in the LHP.
- In DSM operation with a switching PSUT, the loop gain poles may shift into the right half plane under both voltage-mode and current-mode control due to constant power load effects. Nevertheless, stability of the cascade connection is ultimately determined by the closed-loop factor $T/(1+T)$, which may remain stable even when the loop gain exhibits RHP poles.

7.5. Real Impact of Parasitic and Noise in Line and Load Transient Testing Techniques and Systems

The waveforms of voltages and currents during line and load transients are influenced by several collateral factors, in addition to the inherent dynamic behavior of the power regulator under test, which depends on the power stage and control settings.

One main influencing factor is the parasitic inductance in the line bus and load bus. Such inductance influences the slew rate of the real input voltage during line transients and the real output current during load transients. It can also cause high-frequency ringing due to resonance with input and output capacitances. These phenomena influence the line and load transient results regardless of the testing technique used.

In principle, the mathematical model of the FIT-based method presented in this paper allows for incorporating the effects of input and output parasitic inductances by including a series impedance and rewriting all transfer functions. However, this would just complicate the analysis without a real benefit. In fact, parasitic inductances may vary significantly depending on PCB layout and routing. Nevertheless, a well-designed industry-standard power converter is characterized by very low PCB inductance, and consequently, the

oscillation frequency determined by its resonance with capacitances is much higher than the power converter's switching frequency.

The same consideration applies to other real-world harmonic issues, such as EMI from the waveform generator driving the FIT or from other noise sources.

The sampling effect in peak-current mode-controlled power converters also has a negligible influence on FIT-based line and load transient analysis and design. For this well-known phenomenon, in principle, the model given in Equation (40) could be easily extended to incorporate sampling effects by introducing a pole in the factor F_m or a pair of resonant poles in the factor A_s, as discussed in [25]. But this is not necessary as well.

In fact, the bandwidth needed to implement the DSM and DLM is much lower than half the switching frequency of the regulator used as a line and load transient tester. The frequency range in which we are interested in analyzing the dynamic behavior and setting the injection resistance R_j for a power converter used in DSM or DLM falls within its control bandwidth. This typically ranges from 10 kHz to 20 kHz, which is much lower than the typical switching frequency (hundreds of kHz) and the conducted EMI frequencies of practical interest (hundreds of kHz to tens of MHz).

In general, a line or load transient testing system is not required to generate voltage or current stimuli whose slew rate is so high to excite very high frequency noise; rather, it must excite the power converter under test within the bandwidth of its control, to verify its line and load transient response, which (again) is in the tens kHz range. Testing power converters for high-frequency noise measurement, of interest for good PCB design, requires very high slew-rate sources and loads, which are beyond the scope of this paper.

Finally, uncertainties of any type, arising from aging, thermal drifts, component tolerances, and other causes, can be easily incorporated into the transfer functions of the FIT model discussed in the previous sections by applying worst-case or statistical analysis to predict their impact on DSM and DLM operation.

8. Experimental Results

This section presents experimental measurements of the injection-to-output and injection-to-input gains, loop gain, and line/load transient responses of interconnected linear and switching regulators. In particular, the experimental results were obtained using three power supplies from the Texas Instruments Power Management Lab Kit (TI-PMLK) Series [29], and more precisely:

- the TI-PMLK BUCK board, based on the TPS54160 integrated-FET peak current-mode controlled buck regulator [28];
- the TI-PMLK LDO board, based on the TPS7S8300 N-MOS low-dropout linear regulator [30];
- the TI-PMLK BOOST board, based on the TPS55340 integrated-FET peak current-mode controlled synchronous boost regulator [31].

Line transient tests were performed by operating the TPS54160 buck converter in DSM while supplying the TPS7S8300 LDO regulator. Load transient tests were instead carried out by operating the TPS54160 buck converter in DLM while loading the TPS55340 boost regulator.

8.1. Line Transient Test

The TI-PMLK BUCK TPS54160 regulator was configured to operate in DSM to perform a line transient test on the TI-PMLK LDO TPS7S8300 regulator. The schematic of the interconnected boards is shown in Figure 14.

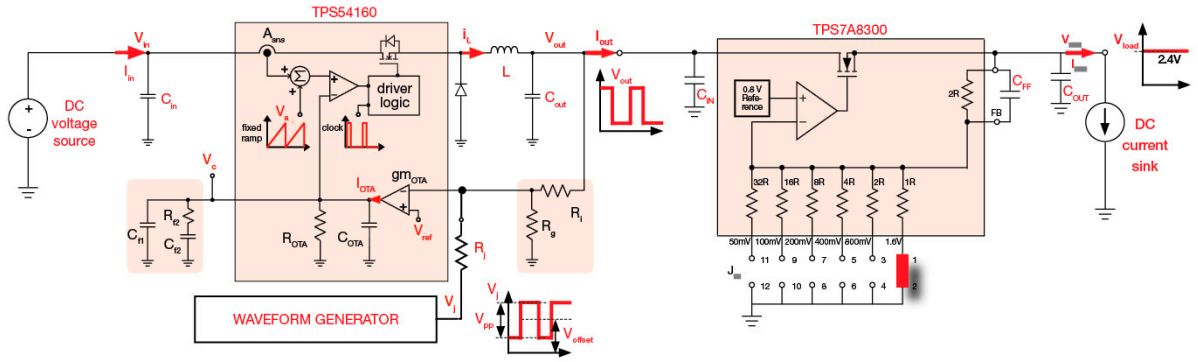


Figure 14. Experimental setup: TPS54160 buck regulator operating in DSM for line transient testing of the TPS7S8300 LDO regulator.

The TPS54160 converter was supplied by a TTi EX354RT 0–35 V/4 A DC power supply. Its feedback pin was connected to the output of an Agilent 33500B 30 MHz waveform generator operating in square-wave mode. A square-wave injection signal with amplitude V_{pp} = 316 mV and offset V_{offset} = 736 mV was applied through a 10 kΩ injection resistance R_j. This configuration produced an output voltage waveform that switches between V_{LOW} = 3 V and V_{HIGH} = 4 V, in accordance with Equations (16) and (29), and the procedure described in [22,23]. The TPS7S8300 regulator was set to 2.4 V output voltage and loaded with a Hoecherl & Hackl ZS1880 800 V/15 A electronic load. The injection-to-output gain and the loop gain of the TPS54160 regulator operating in DSM were measured using an OMICRON Bode 100 vector network analyzer, following the experimental configurations illustrated in Figures 15 and 16, respectively.

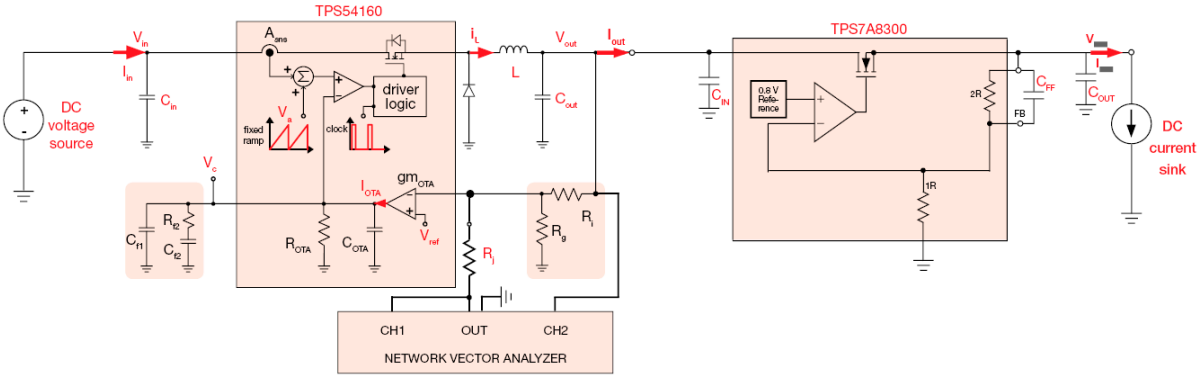


Figure 15. Measurement configuration for the injection-to-output gain of the TPS54160 regulator operating in DSM.

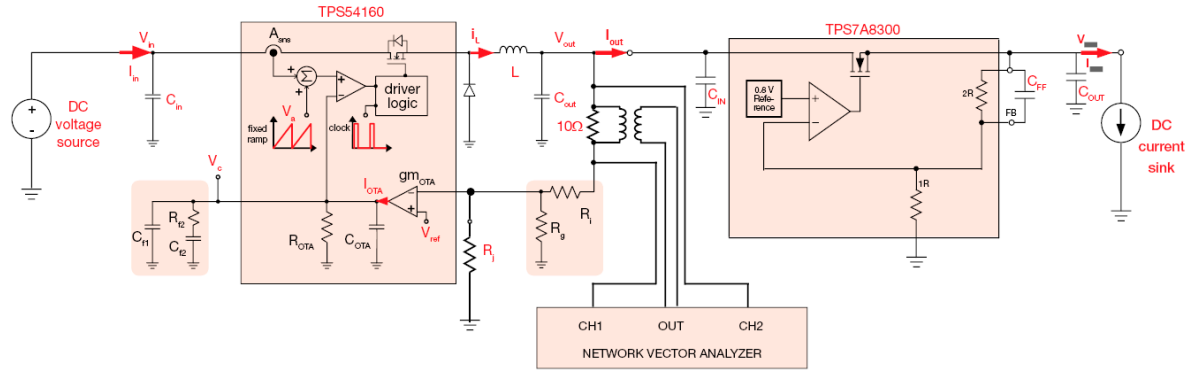
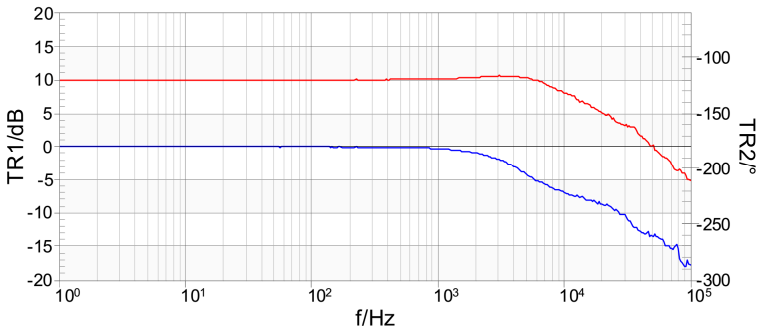
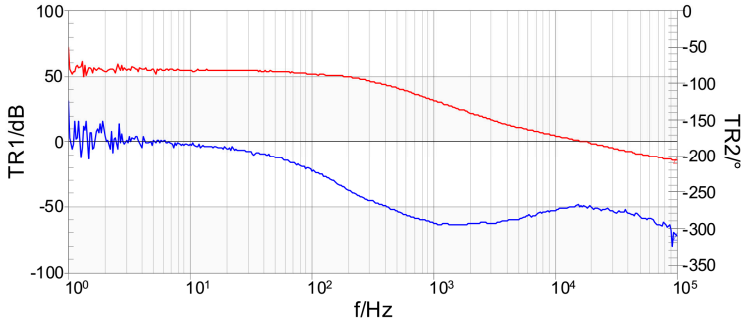


Figure 16. Measurement configuration for loop gain measurement of TPS54160 buck regulator in DSM, loaded by TPS7A8300 LDO regulator.

Figure 17 shows the experimental Bode plots of the injection-to-output gain and loop gain of the TPS54160 buck regulator in DSM. Figure 18 compares the experimental injection-to-output gain with the analytical Bode plot predictions from the model discussed in the previous sections, using nominal values for all circuit parameters. The measured Bode plots agree well with the simulation results. Deviations can be attributed to component tolerances and thermal effects.



(**a**)



(**b**)

Figure 17. Measured injection-to-output gain (**a**) and loop gain (**b**) of the TPS54160 buck regulator in DSM, operating at V_{in} = 36 V, V_{out} = 3.3 V, loaded by TPS7A8300 at V_{out} = 2.4 V, I_{out} = 1.5 A. Red line = TR1, blue line = TR2.

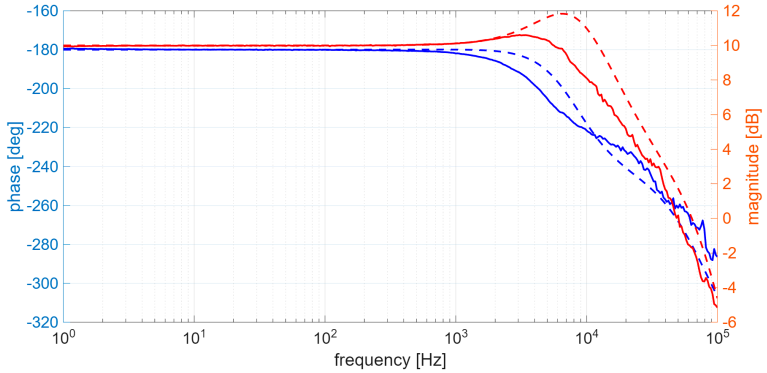


Figure 18. Measured (continuous lines) and simulated (dashed lines) injection-to-output gain of the TPS54160 buck regulator in DSM, operating at V_{in} = 36 V, V_{out} = 3.3 V, loaded by TPS7A8300 at V_{out} = 2.4 V, I_{out} = 1.5 A.

The experimental waveforms shown in Figure 19 were obtained by injecting a 100 Hz square-wave perturbation V_j, which lies well within the injection-to-output bandwidth. The output voltage of the TPS54160 buck converter closely follows the injected waveform, while the higher-frequency harmonics are partially attenuated by the low-pass characteristic of the injection-to-output transfer function.

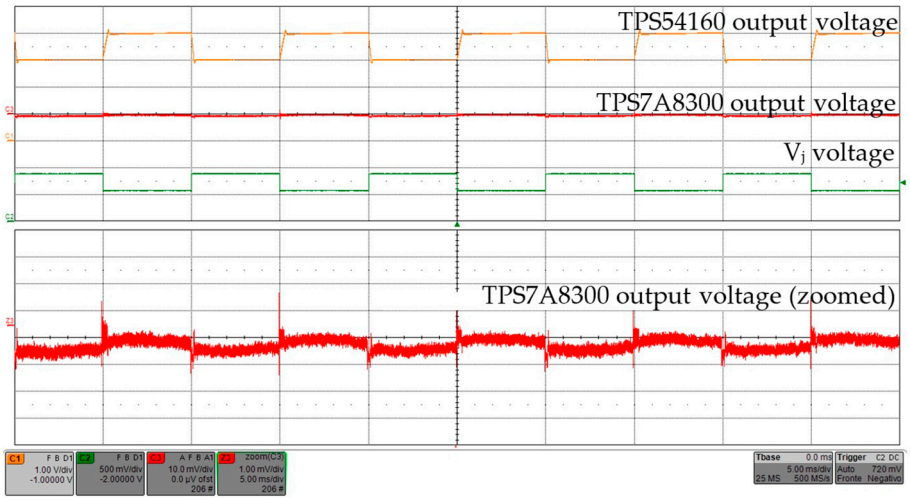


Figure 19. Measured line transient response of the TPS7S8300 LDO regulator supplied by the TPS54160 operating in DSM.

8.2. Load Transient Test

The TI-PMLK BUCK TPS54160 regulator was configured to operate in DLM in order to perform a load transient test on the TI-PMLK BOOST TPS55340 regulator, which provides an output voltage of V_{out} = 24 V. The experimental setup for the injection-to-input gain measurement of the TPS54160 operating in DLM is shown in Figure 20. A 100 Hz square-wave injection signal V_j with amplitude V_{pp} = 310 mV and offset V_{offset} = 840 mV was applied to the feedback pin of the TPS54160 regulator through a 10 kΩ injection resistance R_j. This perturbation produced an output voltage waveform that switches between V_{LOW} = 2.5 V and V_{HIGH} = 3.5 V, as predicted by Equations (16) and (29) and by the procedure described in [22,23]. With a 2 Ω load resistance connected at the regulator output, the resulting square-wave output current varied from 1.25 A to 1.75 A. This corresponds to an input current range of 136–290 mA, including the effect of conversion losses. The input current of the TPS54160 regulator in DLM operation was sensed using a 25 mΩ sensing resistor and a 1 MHz current-sensing amplifier based on the Texas Instruments INA139 device [32].

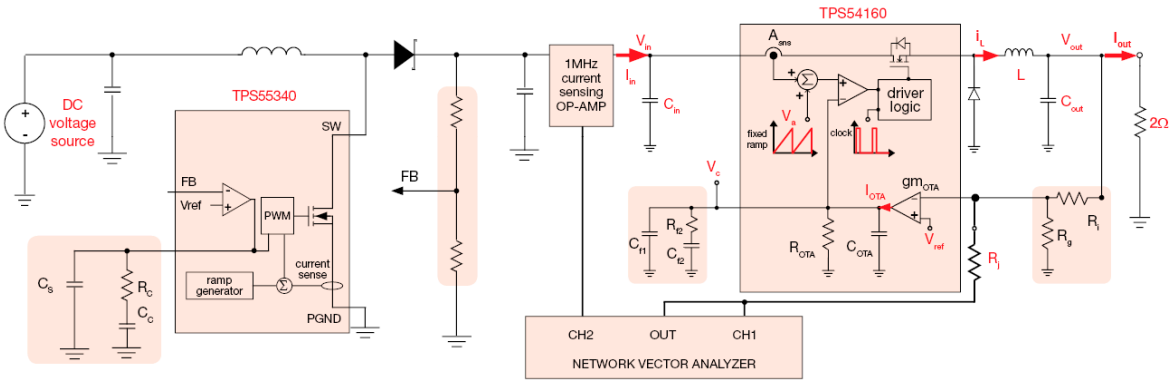


Figure 20. Measurement configuration for injection-to-input gain measurement of TPS54160 buck regulator in DLM, fed by TPS55340 boost regulator.

The measured injection-to-input gain and the corresponding loop gain measurement are presented in Figure 21. Figure 22 compares the experimental injection-to-input gain with the model's analytical Bode plot predictions, using nominal values for all circuit parameters. The experimental data for the injection-to-input current have been scaled up by a factor of 40 to account for the 25 mΩ gain of the current-sensing resistor. Deviations are still due to component tolerances and thermal effects.

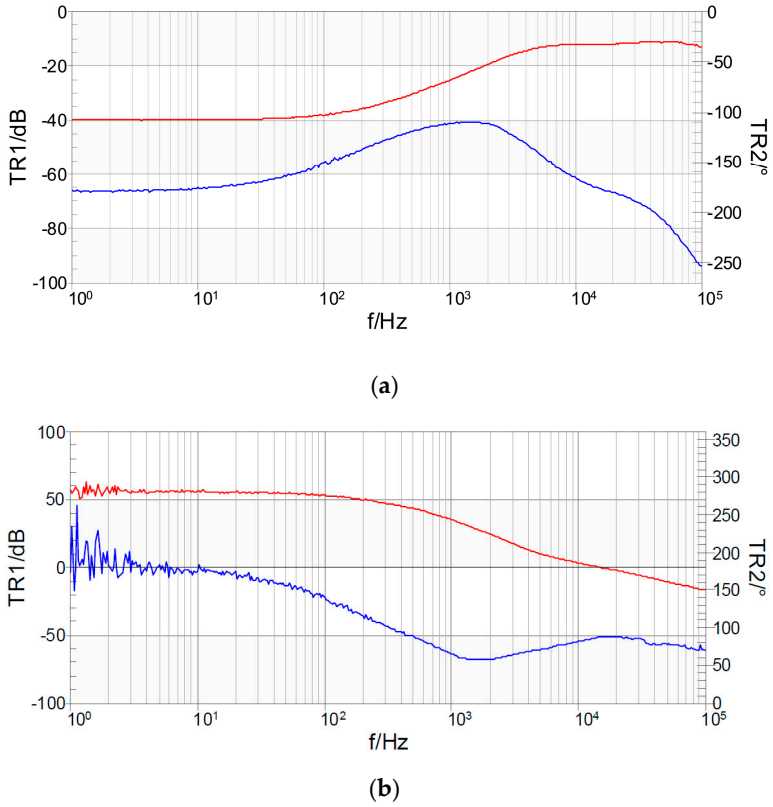


Figure 21. Measured injection-to-input gain (**a**) and loop gain (**b**) of TPS54160 buck regulator in DLM, operating at V_{out} = 3.3 V, I_{out} = 1.5 A, fed by TPS55340 at V_{in} = 8 V, V_{out} = 24 V. Red line = TR1, blue line = TR2.

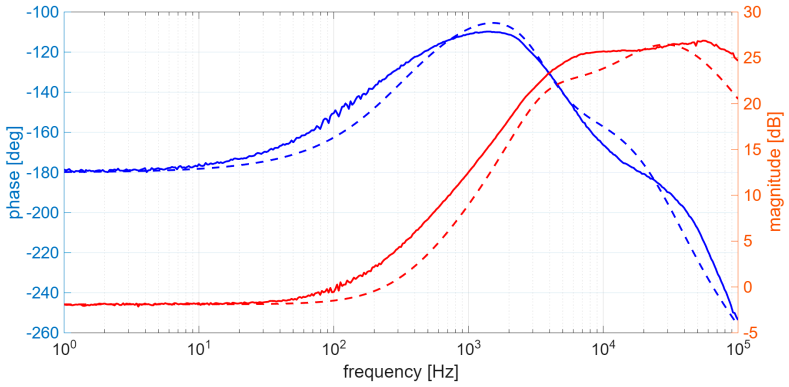


Figure 22. Measured (continuous lines) and simulated (dashed lines) injection-to-input gain of TPS54160 buck regulator in DLM, operating at V_{out} = 3.3 V, I_{out} = 1.5 A, fed by TPS55340 at V_{in} = 8 V, V_{out} = 24 V.

A quantitative evaluation of the results given in Figures 18 and 22 shows that, within the frequency range of interest, namely the effective injection bandwidth of the DSM and DLM configurations, the discrepancy between measured and predicted bandwidth values is limited to a maximum deviation of 10%. This difference is consistent with component tolerances, parasitic effects, and experimental uncertainties.

The measured load transient response of the TPS55340 boost converter loaded by the TPS54160 operating in DLM is shown in Figure 23.

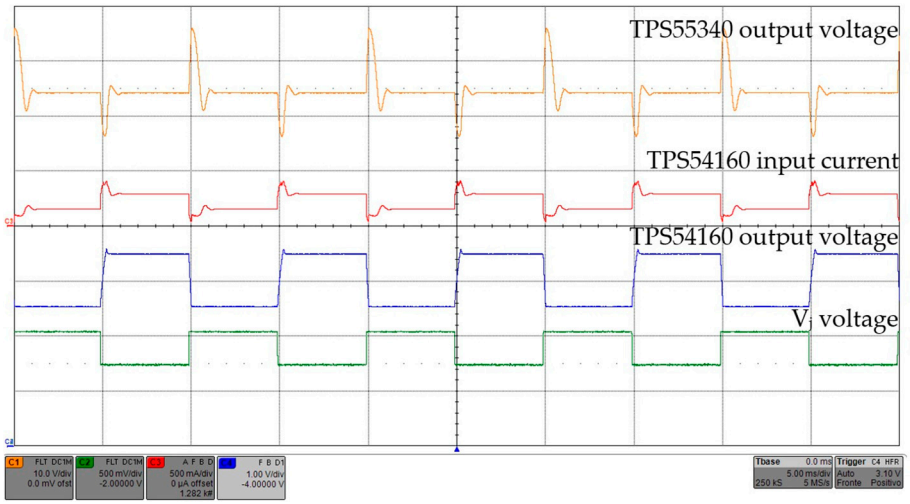


Figure 23. Measured load transient response of the TPS55340 boost regulator loaded by the TPS54160 operating in DLM.

9. Conclusions

The Feedback Injection Technique (FIT) discussed in this paper provides a cost-effective approach for performing dynamic tests on DC–DC power supplies without the need for dedicated high-performance electronic loads or dynamic voltage sources. By injecting a perturbation signal directly into the feedback loop of a standard DC–DC regulator, the regulator can be operated in either Dynamic Source Mode (DSM) or Dynamic Load Mode (DLM), enabling simplified line and load transient testing of the power supply under test.

Unlike state-of-the-art instrumentation and techniques employed for dynamic characterization of DC–DC power supplies, typically requiring dedicated dynamic voltage sources and electronic loads, the FIT approach presented in this paper offers a cost-effective solution for the dynamic testing of DC–DC power supplies, which can be applied with high versatility to both line and load transient testing.

This work presented the fundamental concepts and analytical models required to understand and apply the FIT principle. Closed-loop expressions were derived to characterize the injection-to-output and injection-to-input transfer functions, as well as the associated loop gain, for both voltage-mode and current-mode controlled regulators. Practical guidelines were also provided to determine the achievable operating bandwidth of DC–DC converters in FIT-based DSM and DLM configurations, highlighting the role of the control strategy, the error amplifier implementation, and the injection resistance.

Experimental measurements were carried out using interconnected linear and switching regulators implemented with Texas Instruments TI-PMLK Series BUCK, BOOST, and LDO boards. The measured injection gains and transient responses confirm the validity of the proposed analytical model and demonstrate the effectiveness of FIT as a simple and reliable technique for dynamic characterization and testing of low-power DC–DC power supplies.

The main mandatory requirement for using the FIT solution is that the power converter used in DSM or DLM must have a wider control bandwidth and a higher power rating than the power supply under test, and an accessible feedback control voltage pin.

The analytical developments and illustrative case studies discussed have been carried out with reference to the buck topology, which was deliberately adopted to provide a clear and systematic discussion of the static and dynamic design aspects relevant to line and load transient testing. Nevertheless, the FIT methodology and the derived closed-loop expressions can be extended to other topologies operating in DLM or DSM, for which

additional topology-specific issues can be addressed following the methodological basis established in this work.

Future developments of this work will focus on extending the proposed FIT-based analytical framework to boost and buck–boost converters, in order to systematically investigate topology-specific constraints, stability interactions, and bandwidth limits in both DLM and DSM operation, thereby broadening the applicability of the method to a wider class of DC–DC power supplies.

Author Contributions: N.F.: Conceptualization; methodology; validation; formal analysis; investigation; data curation; writing—original draft preparation; writing—review and editing; visualization. G.D.C.: Validation; formal analysis; investigation; data curation; writing—original draft preparation; writing—review and editing; visualization. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the University of Salerno, grant number 300638FRB24FEMIA, project title "Caratterizzazione di Componenti Di Potenza".

Data Availability Statement: The raw data supporting the conclusions of this article will be made available by the authors on request.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Jiang, W.; Wang, J.; Wang, Q.; Xu, S.; Hashimoto, S.; Liu, Z. Design and Implementation of a Low-Power Low-Cost Digital Current-Sink Electronic Load. *Energies* **2019**, *12*, 2611. [CrossRef]
2. Granda, M.; Fernandez, C.; Barrado, A.; Zumel, P. Nonparametric Frequency Response Identification for DC-DC Converters Based on Spectral Analysis with Automatic Determination of the Perturbation Amplitude. *Sensors* **2021**, *21*, 3234. [CrossRef] [PubMed]
3. Erickson, R.W.; Maksimović, D. *Fundamentals of Power Electronics*, 2nd ed.; Springer: Boston, MA, USA, 2001.
4. Basso, C. *Switch-Mode Power Supplies: SPICE Simulations and Practical Designs*, 2nd ed.; McGraw-Hill Education: New York, NY, USA, 2014.
5. Nguyen-Duy, K.; Knott, A.; Andersen, M.A.E. High Dynamic Performance Nonlinear Source Emulator. *IEEE Trans. Power Electr.* **2016**, *31*, 2562–2574. [CrossRef]
6. Heerdt, J.A.; Ferreira Coutinho, D.; Mussa, S.A.; Lobo Heldwein, M. Control Strategy for Current Harmonic Programmed AC Active Electronic Power Loads. *IEEE Trans. Ind. Electr.* **2014**, *61*, 3810–3822. [CrossRef]
7. Walczak, M.; Bychto, L. Transients in Input and Output Signals in DC–DC Converters Working in Maximum Power Point Tracking Systems. *Energies* **2023**, *16*, 4565. [CrossRef]
8. Li, Q.; Zhang, D.; Zhu, L.; Zhang, W.; Min, R.; Zhang, Q.; Tong, Q. Sample Voltage Dead-Beat Control Based on Differentiative Voltage Prediction and Switching-Cycle Extension for DC-DC Converters. *Electronics* **2024**, *13*, 2319. [CrossRef]
9. Tsang, K.M.; Chan, W.L. Fast-Acting Regenerative DC Electronic Load Based on a SEPIC Converter. *IEEE Trans. Power Electr.* **2012**, *27*, 269–275. [CrossRef]
10. Tsai, M.-T.; Tsai, C. Energy recycling for electrical AC power source burn-in test. *IEEE Trans. Ind. Electr.* **2000**, *47*, 974–976. [CrossRef]
11. Srinivasa Rao, Y.; Chandorkar, M.C. Real-Time Electrical Load Emulator Using Optimal Feedback Control Technique. *IEEE Trans. Ind. Electron.* **2010**, *57*, 1217–1225. [CrossRef]
12. Lu, B.; Wu, X.; Figueroa, H.; Monti, A. A low-cost real-time hardware-in-the-loop testing approach of power electronics controls. *IEEE Trans. Ind. Electr.* **2007**, *54*, 919–931. [CrossRef]
13. Panov, Y.; Jovanovic, M. Practical issues of input/output impedance measurements in switching power supplies and application of measured data to stability analysis. In Proceedings of the 2005 XX Annual IEEE Applied Power Electronics Conference and Exposition, Austin, TX, USA, 6–10 March 2005; pp. 1339–1345. [CrossRef]
14. Rosas-Caro, J.C.; Peng, F.Z.; Cha, H.; Rogers, C. Z-Source-Converter-Based Energy-Recycling Zero-Voltage Electronic Loads. *IEEE Trans. Ind. Electr.* **2009**, *56*, 4894–4902. [CrossRef]
15. Ramirez, J.M.; Torres, E. An electronic load controller for the self-excited induction generator. *IEEE Trans. Energy Convers.* **2007**, *22*, 546–548. [CrossRef]
16. Upadhyay, S.; Mishra, S.; Joshi, A. A Wide Bandwidth Electronic Load. *IEEE Trans. Ind. Electr.* **2012**, *59*, 733–739. [CrossRef]

17. AN-1733, Load Transient Testing Simplified, November 2007. Available online: https://www.ti.com/lit/an/snoa507/snoa507.pdf?ts=1769705415475 (accessed on 20 February 2026).
18. AN-3443, Line and Load Transient Testing for Power Supplies, February 2005. Available online: https://www.analog.com/en/resources/technical-articles/line-and-load-transient-testing-for-power-supplies.html (accessed on 20 February 2026).
19. AN-038, DC/DC Converter Testing with Fast Load Transient, April 2023. Available online: https://www.richtek.com/Design%20Support/Technical%20Document/AN038 (accessed on 20 February 2026).
20. AN-104, Load Transient Response Testing for Voltage Regulators, October 2006. Available online: https://www.analog.com/media/en/technical-documentation/application-notes/an104f.pdf (accessed on 20 February 2026).
21. Femia, N. A cost-effective technique for dynamic testing of DC-DC power supplies. In Proceedings of the 2017 IEEE International Conference on Industrial Technology (ICIT), Toronto, ON, Canada, 22–25 March 2017; pp. 6–11. [CrossRef]
22. Femia, N. Feedback injection-based technique for dynamic load/line tests of DC power supplies part I: Theory. In Proceedings of the 2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL), Trondheim, Norway, 27–30 June 2016; pp. 1–7. [CrossRef]
23. Femia, N. Feedback injection-based technique for dynamic load/line tests of DC power supplies part II: Applications. In Proceedings of the 2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL), Trondheim, Norway, 27–30 June 2016; pp. 1–7. [CrossRef]
24. Venable, H.D. The K-Factor: A New Mathematical Tool for Stability Analysis and Synthesis, Proc. of PowerCon10. 1983. Available online: https://www.venableinstruments.com/hubfs/The%20K%20Factor%20a%20New%20Mathematical%20Tool%20for%20Stability%20Analysis.pdf (accessed on 20 February 2026).
25. Tan, F.D.; Middlebrook, R.D. A Unified Model for Current-Programmed Converters. *IEEE Trans. Power Electron.* **1995**, *10*, 397–408. [CrossRef]
26. Emadi, A.; Khaligh, A.; Rivetta, C.H.; Williamson, G.A. Constant power loads and negative impedance instability in automotive systems: Definition, modeling, stability, and control of power electronic converters and motor drives. *IEEE Trans. Veh. Technol.* **2006**, *55*, 1112–1125. [CrossRef]
27. Zhang, F.; Yan, Y. Start-Up Process and Step Response of a DC–DC Converter Loaded by Constant Power Loads. *IEEE Trans. Ind. Electr.* **2011**, *58*, 298–304. [CrossRef]
28. TI-PMLK Buck Experiment Board Using TPS54160 & LM3475. Available online: http://www.ti.com/tool/pmlkbuckevm (accessed on 20 February 2026).
29. Power Management Lab Kit PMLK PRO. Available online: https://www.ti.com/lit/ml/snvq001/snvq001.pdf?ts=1772055976328&ref_url=https%253A%252F%252Fwww.google.com%252F (accessed on 20 February 2026).
30. TI-PMLK LDO Experiment Board Using TPS7A4901 and TPS7A8300. Available online: http://www.ti.com/tool/pmlkldoevm (accessed on 20 February 2026).
31. TI-PMLK Boost Experiment Board Using TPS55340 & LM5122. Available online: http://www.ti.com/tool/pmlkboostevm (accessed on 20 February 2026).
32. Ina139. Available online: http://www.ti.com/product/INA139 (accessed on 20 February 2026).