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Ion-Induced Charge and Single-Event Burnout in Silicon Power UMOSFETs

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Abstract: The U-shaped Metal-Oxide-Semiconductor Field-Effect Transistor (UMOS or trench FET) is one of the most widely used semiconductor power devices worldwide, increasingly replacing the traditional vertical double-diffused MOSFET (DMOSFET) in various applications due to its superior electrical performance. However, a detailed experimental comparison of ion-induced Single-Event Burnout (SEB) in similarly rated silicon (Si) UMOS and DMOS devices remains lacking. This study presents a comprehensive experimental comparison of ion-induced charge collection mechanisms and SEB susceptibility in similarly rated Si UMOS and DMOS devices. Charge collection mechanisms due to alpha particles from ^{241}Am radiation source are analyzed, and SEB cross sections induced by heavy ions from particle accelerators are directly compared. The implications of the unique gate structure of Si UMOSFETs on their reliability in harsh radiation environments are discussed based on technology computer-aided design (TCAD) simulations.

Keywords: radiation effects; power transistor; UMOSFET; trench gate MOSFET; heavy ion; Single-Event Effect (SEE); Single-Event Burnout (SEB)

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1. Introduction

It is estimated that at least 50% of the global electricity consumption is controlled by power devices, which are primarily characterized by their ability to withstand high voltages [1]. When operating in radiation environments, power devices are susceptible to Single-Event Effects (SEEs) [2], which can disrupt their normal operation or even cause permanent damage. Due to their intense internal electric fields, power electronic devices are particularly susceptible to destructive SEEs [3]. Among the widely used power devices, Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are predominant and are susceptible to Single-Event Burnout (SEB) destructive failure mode due to heavy ions [4], as present in an outer space environment, or neutrons [5], as present in a terrestrial atmospheric environment.

Figure 1 illustrates key MOSFET technologies relevant to this study. The vertical double-diffused MOSFET (DMOSFET) represents the most traditional technology in the power electronics industry, whereas the U-groove MOSFET (UMOSFET), also known as

trench FET, is a more modern technology with notable advantages. For instance, UMOSFET fabrication processes enable significantly higher transistor cell densities on semiconductor wafers compared to DMOSFETs [6,7]. Additionally, UMOSFETs exhibit lower power dissipation than similarly rated DMOSFETs [7]. In recent years, DMOSFET technology has been gradually replaced by UMOSFET technology, establishing UMOSFETs as one of the most widely used semiconductor devices globally [7]. Although UMOSFETs generally exhibit superior electrical characteristics, their structural differences relative to DMOSFETs can lead to significantly different responses under radiation exposure. Therefore, it is essential to evaluate the reliability of UMOS technology and improve its radiation hardness before integrating it into high-reliability applications, such as space missions, terrestrial autonomous vehicles, and avionic systems operating at flight altitudes.

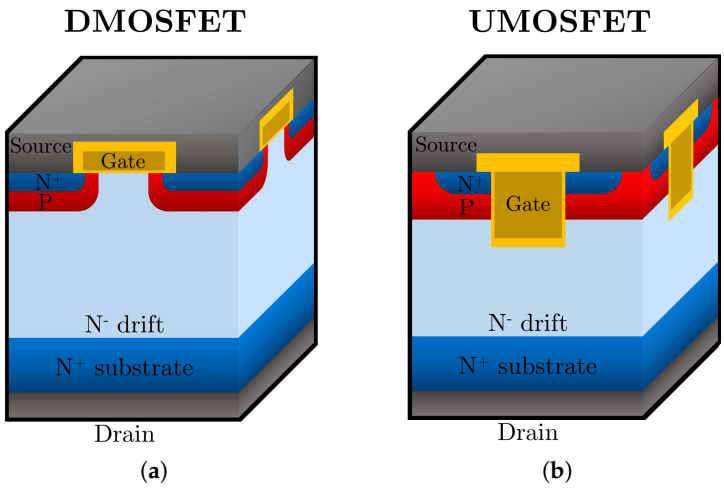

Figure 1. Three–dimensional cross sections of (**a**) DMOSFET and (**b**) UMOSFET structures.

In the past decade, the absence of detailed experimental comparisons of SEB responses between similarly rated UMOS and DMOS devices has been emphasized in the literature [8]. An early computational study on heavy ion-induced SEB in a 70 V-rated silicon (Si) UMOSFET concluded that these devices are less sensitive to SEB than Si DMOSFETs [9]. However, this conclusion was not supported by experimental validation. Recent experimental research on atmospheric neutron-induced SEB in silicon-carbide (SiC)-based UMOS and DMOS power FETs concluded superior robustness of SiC UMOS architectures [10,11]. In contrast, a very recent systematic investigation of Si-based UMOS and DMOS devices demonstrated that Si UMOSFETs are more vulnerable to atmospheric neutron-induced SEB than their DMOSFET counterparts [5]. This apparent contradiction underscores fundamental differences in SEB mechanisms between Si and SiC technologies and highlights the need for a deeper investigation into charge collection dynamics in UMOSFET structures. Such understanding is essential for improving the reliability of next-generation UMOS devices.

In the context of space applications, this study investigates the SEE response of similarly rated Si-based N-type UMOS and DMOS power FETs under energetic ion irradiation. Charge collection mechanisms are analyzed by using alpha particles from a ^{241}Am radiation source, whereas the SEB susceptibility of UMOS and DMOS devices is directly compared by using heavy ion beams provided by particle accelerators. Technology computer-aided design (TCAD) simulations are conducted to support analysis of experimental findings.

2. Materials and Methods

The SEEs induced by alpha particles and heavy ions were detected using techniques based on charge collection spectroscopy and transient current analysis, respectively.

2.1. Devices Under Test

Prior to electric characterization and irradiation, the encapsulation layers of the devices under test (DUTs) were removed through chemical etching, enabling the exposition of the device's die area to impinging radiation. The DUTs were the IXFA220N06T3 UMOSFET and the IRLZ34NPbF DMOSFET parts, with rated drain-source breakdown voltages (BV_{rated}) of 60 V and 55 V, respectively. Although their BV_{rated} values differ slightly, these parts were specifically chosen for accurate comparisons of charge collection and SEE responses due to their nearly equivalent actual drain-source breakdown voltages (BV_{DS}), as confirmed by precision measurements.

Figure 2 shows representative breakdown voltage curves, with both UMOS and DMOS devices exhibiting equivalent breakdown voltages of $BV_{\text{DS}} \cong 70$ V. The BV_{DS} measurements were performed using high-precision SMUs (HP 41420A Source/Monitor Unit, 40 µV − 200 V / 20 fA − 1 A) connected to a high-performance modular system (HP 4142B Modular DC Source/Monitor) controlled by a computer. During these measurements, the DUTs were placed inside a Faraday cage to minimize electronic noise. They were configured in the non-negative gate OFF-state regime, with gate and source grounded ($V_{\text{GS}} = 0$ V), while V_{DS} was gradually increased until the drain-source leakage current (I_{DSS}) reached a predefined limit. Following standard practice, the BV_{DS} was defined as the condition where $I_{\text{DSS}} = 250$ µA at $V_{\text{DS}} = BV_{\text{DS}}$.

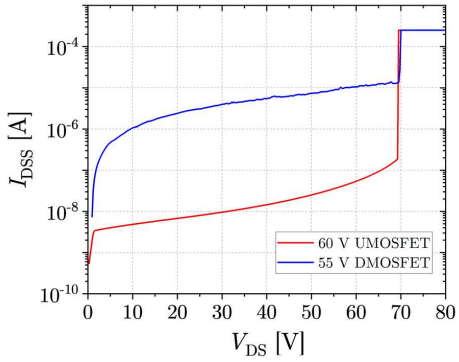

Figure 2. Breakdown voltage measurements of UMOSFET and DMOSFET devices with nominal rated voltages of 60 V and 55 V, respectively. Both DUTs exhibit similar actual breakdown voltages of approximately 70 V. Electrical characterization measured after decapsulation of the devices through chemical etching.

2.2. Alpha Particle Irradiation

The alpha particles were provided by a ^{241}Am radioactive source, with a measured activity of $3.42(10) \times 10^5$ particles.s^{-1} over a 4π solid angle. The decapsulated DUTs were mounted under vacuum for frontal irradiation at room temperature, configured in the non-negative gate OFF-state ($V_{\text{GS}} = 0$ V and $V_{\text{DS}} \geq 0$ V). Charge collection spectroscopy of SEEs induced by alpha particles was performed by using the acquisition system of the SAFIIRA facility [12], Brazil, which utilizes Nuclear Instrumentation Module (NIM) electronics. The system was calibrated with a high-precision charge signal generator (Ortec 419 Precision Pulse Generator). The charge collection spectra of the DUTs were recorded as a function of V_{DS}. Since the UMOSFET and DMOSFET devices studied have similar breakdown voltages, this approach allows for a direct comparison of the main charge collection mechanisms between these FET technologies.

2.3. Heavy Ion Irradiation

Since extensive studies on the ion-induced SEB response of the IRLZ34NPbF DMOSFET have already been published [4], the IXFA220N06T3 UMOSFET was irradiated with

heavy ions in order to enable a direct comparison between SEB cross section measurements. Although a single MOSFET part was tested, SEB response is not expected to vary significantly among devices from the same production batch. The heavy ion irradiations were conducted in two campaigns using the 8 MV São Paulo Pelletron accelerator at the *Laboratório Aberto de Física Nuclear* (LAFN–USP), Brazil, and the 14 MV Tandem-XTU accelerator at the *Istituto Nazionale di Fisica Nucleare—Laboratori Nazionali di Legnaro* (INFN–LNL), Italy. The accelerators were used complementarily to cover a wide range of ion energies: low-energy experiments were performed at LAFN–USP using the SAFIIRA facility [12], and high-energy experiments were conducted at INFN–LNL using the SIRAD facility [13].

Figure 3 shows the schematic diagram of the experimental setup, which is based on the current-limiting technique [14], a standard non-destructive method for protective SEB measurements in power MOSFETs [15–17]. Using this setup, potential SEBs are detected and recorded as current pulse signals by an oscilloscope. At the LAFN–USP, a Rohde & Schwarz RTE 1104 oscilloscope (5 GSa/s, 1 GHz) and a Cemipro ESHV 1500-010 power supply (+1500 V DC, 10.00 mA DC) were used. At the INFN–LNL, a LeCroy WaveRunner 640Zi oscilloscope (40 GSa/s, 4 GHz) and a Keithley 248 power supply (±5000 V DC, 5.000 mA DC) were utilized. In both setups, the input impedance of oscilloscopes were set to 50 Ω to avoid signal reflections, and an Agilent 355D VHF logarithmic attenuator (1 GHz, 50 Ω) prevented them from overcurrent.

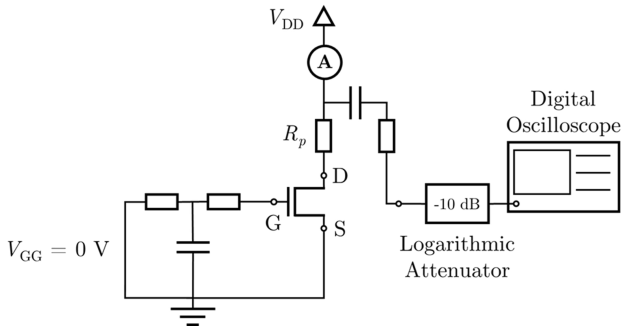

Figure 3. Schematic diagram of the experimental setup used for protective SEB measurements in power transistors.

Heavy ion irradiation experiments were performed using ^{28}Si beams (50.2 to 120.0 MeV) and ^{58}Ni beams (100.0 to 198.0 MeV). Table 1 summarizes the characteristic parameters of the distinct ion beams used in this study. The particle fluence rates were maintained between 5×10^3 and 1×10^4 ions.s^{-1}.cm^{-2}, adjusted for each test run to avoid dead time losses. Frontal irradiation was performed at room temperature under high vacuum ($\lesssim 10^{-5}$ Torr), with devices biased at $V_{GS} = 0$ V and $V_{DS} > 0$ V. For each V_{DS}, irradiation continued until the typical beam fluence of $\Phi = 10^6$ ions.cm^{-2} was reached [15,17]. The SEB cross section was calculated as the number of recorded SEB signals per unit fluence. This procedure was repeated at progressively higher V_{DS} values, covering all ion-energy combinations.

Table 1. Energy, range, and surface linear energy transfer (LET) in silicon for the ion species used in our experimental study.

Ion	Energy [MeV]	Range [µm]	LET_{surf} [MeV.cm^2.mg^{-1}]
^{4}He	5.486	28.0	0.6
^{28}Si	50.2	17.4	13.3
	72.0	24.8	12.1
	96.0	33.8	10.9
	120.0	43.9	9.9
^{58}Ni	100.0	20.1	30.9
	140.0	25.7	31.3
	196.0	33.5	30.1

3. Results

3.1. Alpha Particle Irradiation

Only non-destructive SEEs of the Single-Event Transient (SET) type were detected during alpha particle irradiation experiments in similarly rated DMOS and UMOS transistors with $BV_{DS} \cong 70$ V.

Figure 4 exhibits their charge collection spectra at different V_{DS} levels. The charge collection spectra induced by alpha particles in the DUTs can be categorized into three main components: (i) a low-charge collection tail, (ii) a principal collection peak, and (iii) a high-charge collection tail. The dependence of the principal charge collection peaks on V_{DS} is shown in Figure 5.

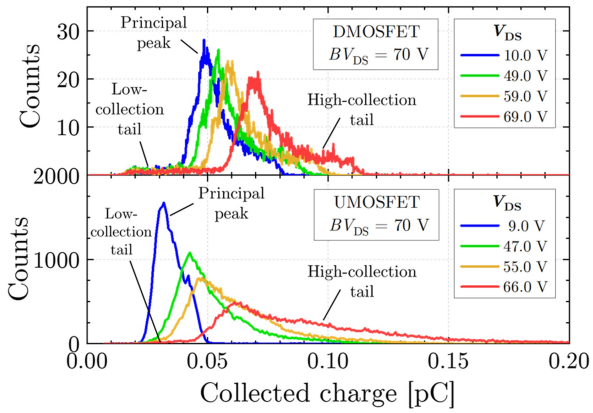

Figure 4. Representative charge collection spectra of alpha particle-induced SEEs in DMOS (**top**) and UMOS (**bottom**) power transistors for selected V_{DS} values. Spectra normalized to the same fluence of $3.8(2) \times 10^5$ particles.cm^{-2}.

Regarding the charge collection mechanisms in the DMOSFET, it is first noted that the low-charge collection tail remains nearly independent on V_{DS}. A previous study has reported detailed temporal analysis of ion-induced charge spectroscopy in a P-channel MOSFET, identifying similar low-collection tail and principal peak as due to diffusion and drift/funneling mechanisms, respectively [18]. These facts confirm that the observed low-charge collection tail results from a diffusion mechanism, where charge carriers are generated by the impinging ions in field-free regions of the device. In the absence of electric field, these carriers diffuse into the sensitive volume of the DMOSFET, where they are partially collected, thereby triggering a SEE. For instance, this scenario corresponds to ions impinging over the gate pad region, as denoted by (i) in Figure 6a. By contrast, the principal peak shifts forward as the applied V_{DS} increases. As shown in Figure 5, the asymptotic dependence of collected charge on V_{DS} at low voltages suggests depletion-

region modulation, consistent with the interpretation of prompt charge collection [18]. Thus, the principal peaks in Figure 4 are attributed to ion impacts on the P-body/N-drift depletion region beneath the source contact, resulting in a diode current response (mechanism (ii) in Figure 6a). The high-charge collection tail, however, arises from ion impacts near the PN junction edges beneath the gate contact (mechanism (iii) in Figure 6a), where the electric fields are stronger than in parallel junctions [1]. The shape of the high-charge collection component is found to be even more dependent on V_{DS} than the prompt collection peak. Ions impinging in this region may ultimately result in a parasitic BJT response [19,20].

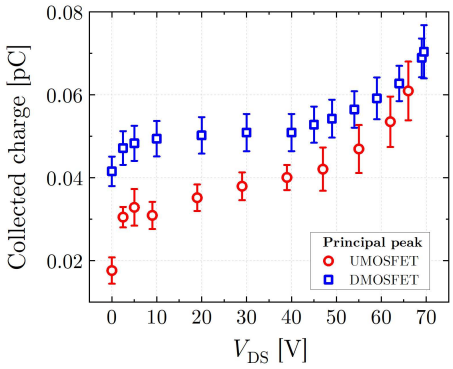

Figure 5. Dependence of the principal charge collection peaks on drain-source voltage in power transistors irradiated with alpha particles.

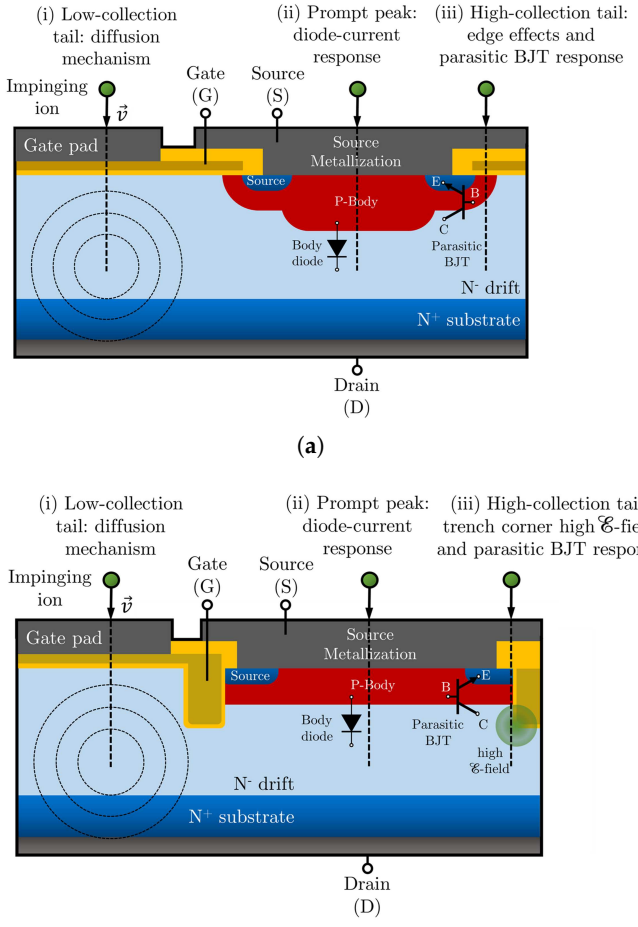

Figure 6. Schematic representation of the main ion-induced charge collection mechanisms in (**a**) DMOS and (**b**) UMOS power transistors. E, B, and C correspond to the emitter, base, and collector, respectively, of the parasitic bipolar junction transistor (BJT) structure.

Similarly to that observed in the DMOSFET, the low-collection tail in the UMOSFET is attributed to diffusion transport due to particle impact over field-free regions, such as the gate pad (mechanism (i) in Figure 6b). The UMOS response also exhibits a (ii) prompt collection peak and (iii) high-charge collection tail. As shown in Figure 4, at lower voltages, the charge collection in the UMOSFET resembles a Gaussian curve with slight positive skewness. However, as V_{DS} increases, the high-energy tail becomes prominent. Notably, SEEs associated with high collected charge values are observed at high voltages, indicating that the influence of V_{DS} on high-charge SEEs is even more pronounced in the UMOSFET than in the DMOSFET. Relatively high electric fields occur near the trench corners in the UMOSFET structure [1]. Therefore, the impact ionization process, which is highly dependent on the electric field intensity, is likely responsible for charge carrier multiplication in UMOSFETs operating at higher voltages (mechanism (iii) in Figure 6b).

Figure 5 shows the dependence of the principal charge collection peak on V_{DS}. As previously noted, charge collection approximately follows a $\sqrt{V_{DS}}$ dependence at lower voltages ($V_{DS} < 50$ V), apart from a constant offset, due to depletion-region modulation. In this regime, the DMOSFET exhibits superior collection efficiency, which likely arises from its usually deep P-body/plug extension, as illustrated in Figure 6a. At higher voltages ($V_{DS} > 50$ V), the prompt collected charge exhibits exponential growth. This behavior provides clear evidence that impact ionization plays a significant role in the charge multiplication mechanism of the high-collection tail, as the data reflect the exponential dependence of impact ionization on electric field intensity [21]. Figure 4 reveals that impact ionization is more pronounced in the UMOSFET, evidenced by its maximum collected charge surpassing that of the DMOSFET at higher voltages. Additionally, Figure 5 shows that the average prompt collected charge increases more rapidly in the UMOSFET as V_{DS} increases, further supporting the conclusion that internal electric field favors charge multiplication through impact ionization.

Table 2 presents the non-destructive SEE cross section (σ_{SEE}) for irradiated power transistors. The UMOSFET exhibits a higher absolute SEE cross section than the DMOSFET, indicating a higher susceptibility to alpha particle-induced SEEs. Power transistors typically consist of multiple parallel identical transistor cells, with UMOSFETs achieving significantly higher cell densities than DMOSFETs [6,7]. This structural difference explains the increased SEE sensitivity of the UMOSFET, which arises from both a higher transistor cell density and a larger total die area. In order to evaluate the intrinsic SEE vulnerability of each technology independently of die area dimensions, it is convenient to normalize the σ_{SEE} by die area. The normalized results, also presented in Table 2, reveal that both technologies exhibit comparable SEE susceptibility per unit area, with approximately 50% of the irradiated device areas being sensitive to SEEs induced by alpha particles.

Table 2. SEE cross sections (σ_{SEE}) and normalized SEE cross sections of transients induced by alpha particles in power transistors.

Technology	σ_{SEE} [cm^2]	σ_{SEE} Normalized per Die Area [a]
UMOSFET	$1.02(5) \times 10^{-1}$	$4.70(21) \times 10^{-1}$
DMOSFET	$4.42(23) \times 10^{-3}$	$4.55(23) \times 10^{-1}$

[a] Die area subtracting the total shadowing area from thick bond wires.

Although alpha particle irradiation results provide limited insight into overall device reliability, experimental data confirm significant charge multiplication due to impact ionization in UMOSFETs operating at high bias voltages. Contrary to early computational prediction [9], this enhanced charge multiplication suggests UMOSFETs may be more prone to destructive radiation effects like SEBs, which critically depend on impact ion-

ization. To validate this hypothesis, heavy ion irradiation experiments are required for a comprehensive SEB reliability comparison between UMOS and DMOS technologies.

3.2. Heavy Ion Irradiation

Heavy ion-induced SEB cross sections in the IRLZ34NPbF DMOSFET from previous studies [4] were compared with SEB measurements in the IXFA220N06T3 UMOSFET. Both devices have actual breakdown voltages of approximately 70 V. No significant ion-induced microdose effects [22] were observed in the UMOSFET during irradiation runs, where the measured I_{DSS} of the UMOSFET remained below 1 µA, consistent with its maximum characteristic value of 10 µA, according to the device datasheet [23]. Unlike the UMOSFETs investigated in [22], the IXFA220N06T3 UMOSFET is not particularly designed in a stripe geometry. In order to enable direct comparison between devices with different die areas, the measured σ_{SEB} were normalized by the die area of each DUTs, enabling a more accurate reliability analysis.

Figure 7 shows the dependence of heavy ion-induced SEBs on V_{DS} for similarly rated DMOS and UMOS devices under ^{28}Si irradiation. Although the irradiation energy values differ between devices, their energy ranges overlap within the 50–70 MeV interval ensures valid comparative analysis. Despite having equivalent breakdown voltages, the UMOS device triggers SEBs at significantly lower operating voltages than the DMOS device across the studied energy range. By fitting cumulative Weibull distributions to the experimental data [24], we determined statistical SEB threshold voltages. Whereas the DMOSFET exhibits SEBs at voltage ratios $V_{DS}/BV_{DS} \gtrsim 75\%$, SEBs can be triggered in the UMOS transistor at ratios as low as $V_{DS}/BV_{DS} \cong 50\%$. Based on results from alpha particle irradiation presented in Section 3.1, the heavy ion data presented in Figure 7 indicate that enhanced charge multiplication through impact ionization in UMOSFETs is likely the primary cause of their higher SEB vulnerability compared to DMOSFETs.

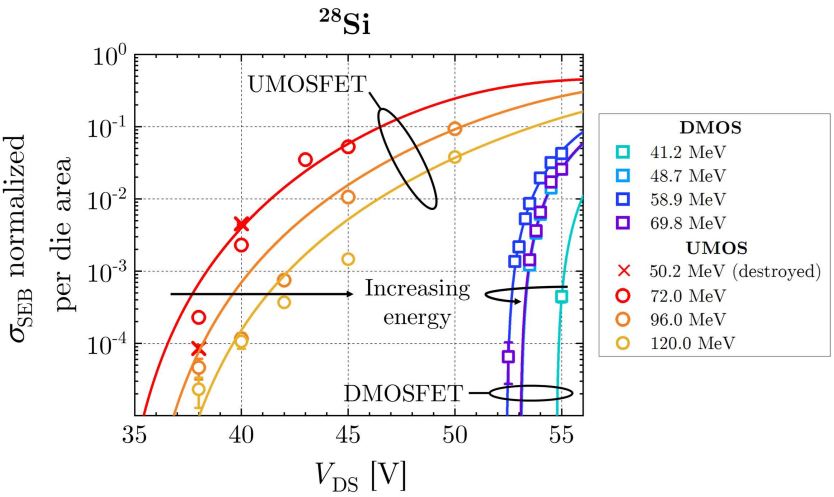

Figure 7. Normalized SEB cross sections of the IRLZ34NPbF DMOSFET and IXFA220N06T3 UMOSFET, both with breakdown voltages of approximately 70 V, irradiated with ^{28}Si ($Z = 14$) ion beams. The DMOS data are reproduced from [4]. The plot incorporates all experimental uncertainties, with non-visible values indicating magnitudes smaller than the representative data point dimensions. Values are normalized by the irradiated die areas of the devices.

It should be mentioned that the protective circuitry ($R_p = 33$ kΩ) failed to prevent SEBs induced by 50.2 MeV ^{28}Si ions in the UMOSFET, ultimately resulting in device destruction (drain-source short-circuit). In order to contextualize this result, we applied the model of Titus and Wheatley for worst-case SEE prediction [25]. For a fully depleted Si-based vertical MOSFET ($V_{DS} = BV_{DS} = 70$ V) without a buffer layer, the model predicts

critical irradiation conditions for ^{28}Si ($Z = 14$) at 68 MeV. For the energy range considered in our experiments, the data shown in Figure 7 confirm that the critical energy for ^{28}Si impinging the UMOSFET lies between 50.2 MeV and 72.0 MeV, consistent with model prediction. For the DMOSFET under a fully depleted condition, the prediction of the Titus–Wheatley model (68 MeV) aligns with experimental worst-case (58.9 MeV) within approximately 15% variation.

Figure 8 presents additional SEB cross section measurements for the IRLZ34NPbF DMOSFET and the IXFA220N06T3 UMOSFET due to distinct ion species with atomic numbers ranging from $Z = 26$ to $Z = 29$. These ion species include ^{56}Fe ($Z = 26$), ^{58}Ni ($Z = 28$), and ^{63}Cu ($Z = 29$) at distinct energies. The DMOSFET data are sourced from prior studies [4], whereas the UMOSFET data are from original experimental measurements. Complementing the ^{28}Si ($Z = 14$) irradiation results shown in Figure 7, the data in Figure 8 further confirm the higher susceptibility of the UMOSFET to SEB compared to the similarly rated DMOSFET under heavy ion irradiation in the Z = 26–29 range. The SEB response of both transistors can be qualitatively explained by examining energy deposition in their epitaxial regions. Figure 9 shows the Linear Energy Transfer (LET) curves of the heavy ions from Figure 8 impinging on a fully depleted 70 V generic MOSFET structure, simulated by using the SRIM code [26]. For simplicity, the simulated generic MOSFET structure consists of a 5 µm-thick aluminum metallization layer, a 2 µm-thick P-base layer, and a 4.1 µm-thick N-drift layer. As shown in Figure 9, the energy deposition within the epitaxial region increases progressively from 65.0 MeV ^{56}Fe to 196.0 MeV ^{58}Ni irradiation. This trend aligns with the observed variation in SEB threshold voltages (V_{SEB}) in Figure 8, where higher energy deposition correlates with lower V_{SEB}. The relationship between V_{SEB} and the deposited charge in the epitaxial region (Q_{dep}) can be estimated for both devices using LET curves simulated with SRIM for the ion-energy combinations presented in Figures 7 and 8. This analysis reinforces the superior SEB susceptibility of the UMOS device based solely on deposited charge, regardless of the ion-energy combination adopted.

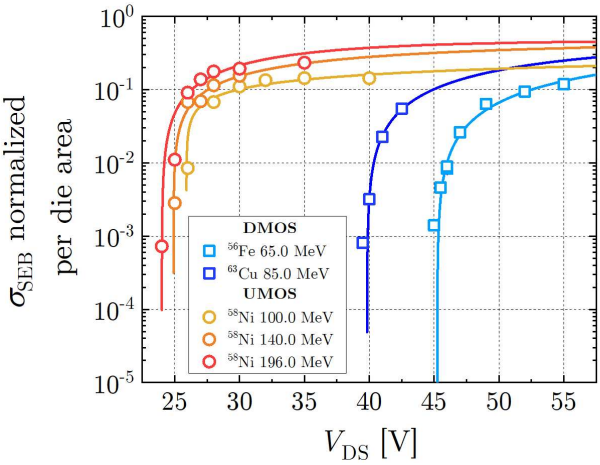

Figure 8. Normalized SEB cross sections of the IRLZ34NPbF DMOSFET and IXFA220N06T3 UMOSFET, both with breakdown voltages of approximately 70 V, irradiated with ^{56}Fe ($Z = 26$), ^{58}Ni ($Z = 28$), and ^{63}Cu ($Z = 29$) ion beams. The DMOS data are reproduced from [4]. The plot incorporates all experimental uncertainties, with non-visible values indicating magnitudes smaller than the representative data point dimensions. Values are normalized by the irradiated die areas of the devices.

Figure 10 presents the dependence of V_{SEB} on Q_{dep} for both UMOS and DMOS devices. Across the investigated Q_{dep} range, the UMOSFET consistently exhibits significantly lower SEB threshold voltages compared to the DMOSFET. These results complement the earlier demonstration in Figure 7, which demonstrated the greater vulnerability of the

UMOSFET under identical ion species. The experimental data include several ion species at various energies. The relationship between V_{SEB} and Q_{dep} for both device types can be approximated by a power-law model of the form $y = ax^b$. Table 3 presents the power law curve fit parameters a and b for UMOS and DMOS data. From this model, one estimates the minimum deposited charge within the epitaxial region required to induce SEB (Q_{SEB}) to be 0.12 pC for the UMOSFET and 0.51 pC for the DMOSFET. These results demonstrate that a UMOSFET with $BV_{DS} = 70$ V not only exhibits the lower SEB threshold voltages but also requires less deposited charge to initiate SEBs, approximately 20% of the critical charge needed for a DMOSFET counterpart. This simple model can explain why alpha particles from a ^{241}Am source cannot induce SEB in the DUTs. SRIM simulations reveal that 5.486 MeV alpha particles deposit a maximum of 0.043 pC in the fully depleted epitaxial region of a 70 V generic MOSFET structure, which remains below the Q_{SEB} thresholds for both device types. The combination of reduced V_{SEB} and lower Q_{SEB} thresholds makes current UMOSFET designs more susceptible to heavy ion-induced SEB compared to similarly rated DMOSFETs.

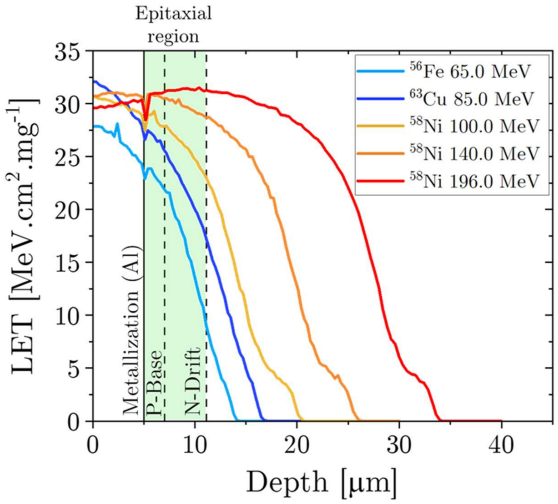

Figure 9. Linear Energy Transfer (LET) curves for heavy ion beams from Figure 8 impinging on a fully depleted 70 V generic MOSFET structure.

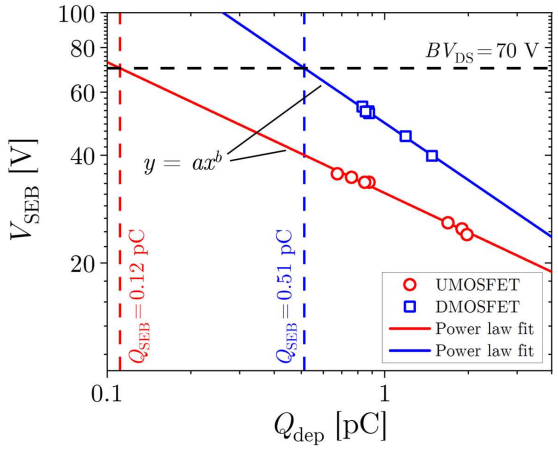

Figure 10. Dependence of SEB threshold voltage (V_{SEB}) on the deposited charge within the epitaxial region (Q_{dep}) in similarly rated UMOS and DMOS power transistors for ion-energy combinations from Figures 7 and 8. Q_{SEB} represents an estimate of the minimum charge deposited within the epitaxial region required to trigger SEB. The plot incorporates all experimental uncertainties, with non-visible values indicating magnitudes smaller than the representative data point dimensions.

Table 3. Curve fit parameters for the power law relationship ($y = ax^b$) between V_{SEB} and Q_{dep}, in SI units, in similarly rated UMOS and DMOS power transistors.

Technology	*a*	*b*
UMOSFET	$1.3(6) \times 10^{-3}$	$-0.366(16)$
DMOSFET	$2.2(11) \times 10^{-5}$	$-0.529(18)$

4. Discussion

Two-dimensional TCAD simulations were performed using ECORCE software (v 2.26) [27] on a generic UMOSFET with $BV_{DS} = 70$ V to analyze the SEB dynamics in this device and corroborate experimental observations induced by heavy ions. Although detailed design and process parameters for the IXFA220N06T3 UMOSFET are unavailable, the simulated UMOS structure was engineered to replicate its key electrical characteristics. The implications of potential parameter variations were not considered in this study. For instance, the simulated devices achieves a breakdown voltage of $BV_{DS} = 70$ V, consistent with measurements in Figure 2, and a threshold voltage of $V_{th} = 3.1$ V, which is acceptable as a typical value according the datasheet (V_{th} = 2.0–4.0) [23]. The blocking and transfer characteristics of the simulated UMOSFET are presented in Figure 11.

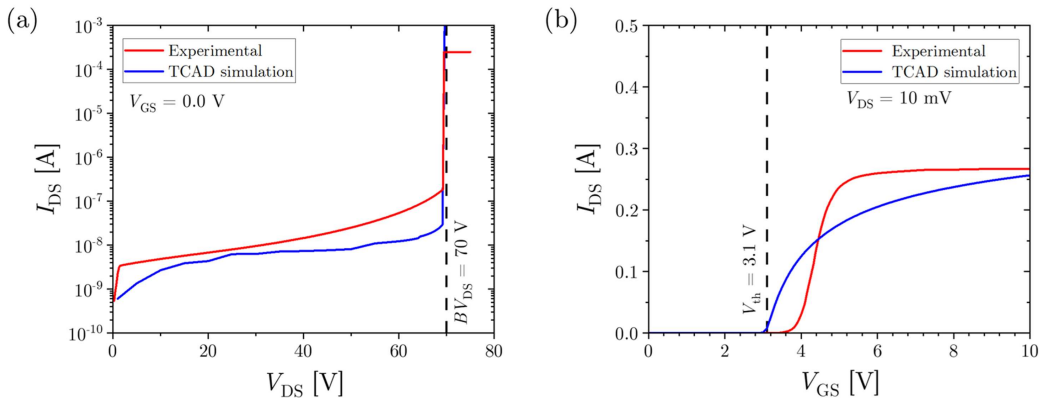

Figure 11. Comparison of (**a**) blocking and (**b**) transfer characteristics between the simulated UMOSFET structure and experimental measurements. Since 2–D simulations were performed, a calibration factor of $f = 10^6$ was applied when converting simulated currents to physical units. Simulated using ECORCE [27].

The simulated structure comprises a N-drift region with a doping concentration of 4.5×10^{15} cm^{-3} and a thickness of 5.1 µm below the P-base/N-drift junction. The N-source region features a doping concentration of 1.0×10^{19} cm^{-3} and a depth of 0.5 µm, whereas the P-base region was assumed with a doping concentration of 1.0×10^{17} cm^{-3} and a depth of 1.5 µm. The gate oxide was modeled with a thickness of 50 nm along the trench sidewalls and 0.5 µm-thick at the bottom surface. A half-cell with a width of 1.5 µm was adopted as a representative unit cell [6]. The adopted physics models incorporate carrier generation by impact ionization and band-to-band tunneling, recombination via Shockley–Read–Hall and Auger processes, radiation-induced electron-hole pair separation (through a yield function), band-gap narrowing, and carrier mobility dependent on electric field and doping concentration [27].

Figure 12 presents a visualization of the simulated doping profiles, device geometry, and the peak electric field distributions following a 50 MeV ^{28}Si strike at $x = 0.75$ µm, as marked by the dashed green line. This ion energy represents one of the most severe irradiation conditions observed experimentally in the UMOSFET under ^{28}Si exposure, as previously shown in Figure 7. Under high-bias conditions ($V_{DS} = 55$ V), the electric field

peak shifts toward the drift/substrate junction due to the Egawa effect [28], surpassing the critical electric field of silicon ($\mathcal{E}_{crit} \approx 0.3$ MV.cm^{-1} [29]) and triggering a SEB. However, in alignment with experimental results, SEB does not occur at sufficiently lower bias voltages, such as $V_{DS} = 25$ V. Recent TCAD simulations of ion-induced SEB in 150 V-rated UMOS and DMOS devices revealed significantly higher peak electric field intensities in the UMOS structure compared to the DMOS counterpart with equivalent voltage ratings [5].

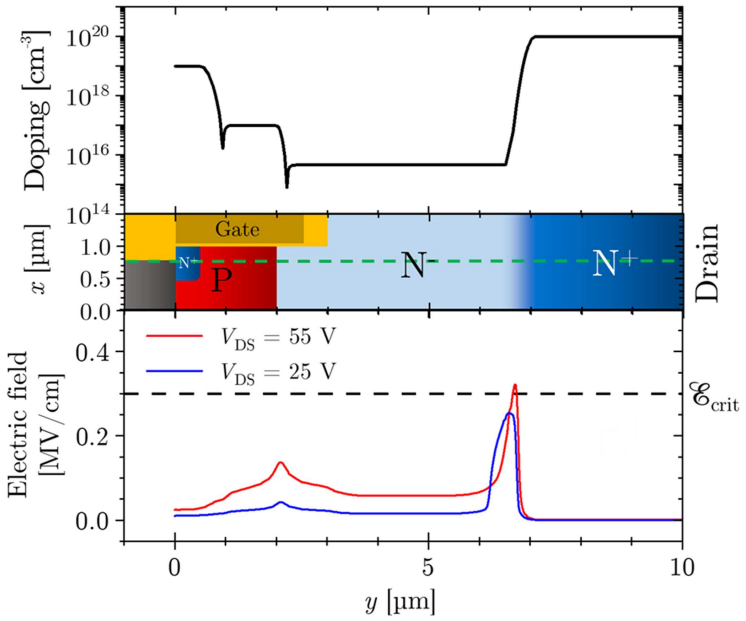

Figure 12. Simulated device structure and spatial distributions of the peak electric field in a 70 V UMOSFET at $x = 0.75$ µm (dashed green line), induced by a ^{28}Si at 50 MeV striking the N–source region. Simulated using ECORCE [27].

Figure 13 shows peak electric field distributions resulting from a 50 MeV ^{28}Si striking the trench gate column at $x = 1.20$ µm, as marked by the dashed green line. The SEB response resembles that obtained for ion strikes over the N-source region. However, while the field in the drift/substrate junction reaches the silicon critical field, intense electric fields also develop in the vicinity of trench gate structure. Figure 13 exhibits the field distributions along the ion impact position (position A, dashed green line, $x = 1.20$ µm) and the vicinity of trench sidewalls in silicon (position B, dashed blue line, $x = 0.99$ µm). Along the ion strike position (position A), the electric field in the gate dielectric exceeds that in the semiconductor material due to distinct relative permittivities for SiO_2 ($\varepsilon_r = 3.9$) and Si ($\varepsilon_r = 11.9$) [30]. Comparatively, the dielectric strength of SiO_2 is approximately 10 MV.cm^{-1} [30]. After the ion strike, as the gate oxide is unshielded from the drain potential, it experiences rapid increase in electric field intensity, especially at high voltages. For ions with sufficiently high LETs and depending on the device gate oxide thickness, the resulting electric field spikes can ultimately induce the gate oxide rupture, also referred to as Single-Event Gate Rupture (SEGR) [31]. The ion impact further amplifies the electric field near the trench sidewall in silicon (position B), with the local field exceeding 0.3 MV.cm^{-1} at the trench corner. The peak field intensity at this location surpasses that observed for strikes at $x = 0.75$ µm. These elevated fields promote carrier multiplication in silicon via impact ionization, as experimentally confirmed in Section 3.1. Although not experimentally observed in this study, elevated electric fields in the vicinity of channel regions can also promote hot-carrier injection into the gate oxide [6], generating oxide charge accumulation and the formation of interface traps. Over prolonged radiation exposure, these effects may lead to enhanced threshold voltage shifts and transconductance degradation [30].

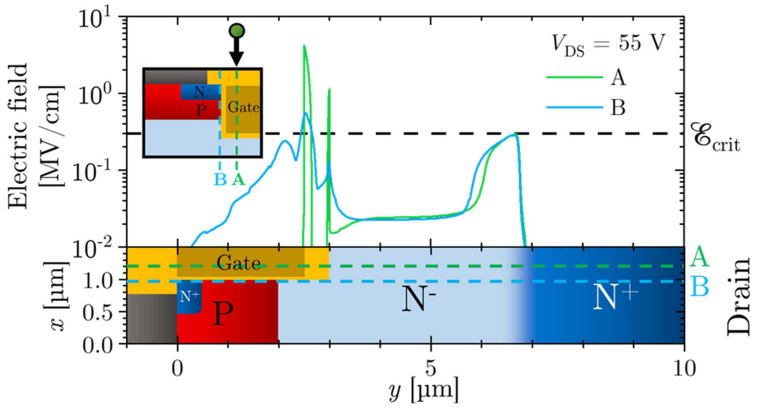

Figure 13. Spatial distributions of the peak electric field in a 70 V UMOSFET at $V_{DS} = 55$ V, induced by a ^{28}Si at 50 MeV striking the trench gate column. The field distributions are observed along both ion strike position (position A, dashed green line, $x = 1.20$ µm) and the vicinity of trench sidewalls in silicon (position B, dashed blue line, $x = 0.99$ µm). Simulated using ECORCE [27].

Although trenches gates enable superior electrical performance of Si UMOSFETs, such as their notably low specific on-resistance, they simultaneously introduce reliability challenges with respect to radiation effects. Under energetic ion exposure, e.g., in space environments, intense electric fields are generated near the trench gate corners, potentially compromising the physical integrity of both the semiconductor and insulating materials. The results presented in this study are consistent with recent findings on atmospheric neutron effects in similarly rated Si UMOS and DMOS devices, which revealed an enhanced vulnerability of Si UMOSFETs to SEBs induced by secondary particles from nuclear reactions involving quasi-atmospheric neutrons and device materials [5]. Similarly to radiation-hardened Si DMOSFETs [32], a common hardening trend in UMOSFETs has been the incorporation of a buffer layer to reduce field concentrations at the drift-substrate junction following a particle strike [5,33]. Based on the findings of our present study, alternative strategies to further reduce electric field intensities at trench gate corners, along with the optimization of buffer layer design, may significantly improve the SEB tolerance of next-generation power UMOSFETs.

Based on computational studies in DMOSFETs [32], it is likely that incorporating buffer layers with optimized doping profiles and thicknesses, along with source (emitter) doping optimization, could enhance SEB robustness in UMOSFETs. A recent study suggest that this approach may also mitigate neutron-induced SEBs in UMOSFETs [5]. However, a detailed evaluation of UMOSFET structural optimization requires dedicated TCAD simulations studies, which falls beyond the scope of our current work.

Finally, consistent with our results using energetic ions, recent studies with monoenergetic neutrons [34] and quasi-atmospheric neutrons [5] confirm that Si-based UMOSFETs are generally more susceptible to premature charge multiplication and destructive radiation effects compared to similarly-rated DMOSFETs. However, as mentioned in the introduction, experimental research on atmospheric neutron-induced SEB in SiC-based UMOS and DMOS power FETs demonstrated superior robustness in SiC UMOS architectures [10,11]. This discrepancy between our observed vulnerability in Si UMOSFETs and the reported robustness of SiC UMOSFETs strongly supports the conclusion that SEB mechanisms differ fundamentally between Si and SiC MOSFETs. In fact, unlike the well-established SEB mechanism in Si MOSFETs [19,20], recent work suggests that SEB onset in SiC power MOSFETs may instead be governed by critical energy stored in the depletion region [35].

5. Conclusions

The ion-induced SEE response of similarly rated Si-based UMOS and DMOS power FETs was experimentally investigated under both alpha particle and heavy ion irradiation. The main aspects of their charge collection mechanisms and susceptibility to ion-induced SEB were comparatively analyzed. By using alpha particles from a ^{241}Am radiation source, it was experimentally demonstrated that charge carrier multiplication is more pronounced in a UMOSFET than its DMOSFET counterpart during high-voltage operation. Contrary to earlier computational prediction and recent experiments involving SiC-based UMOS and DMOS transistors, heavy ion beam experiments with particle accelerators demonstrate that the Si-based UMOSFET generally initiates SEB at significantly lower thresholds and is substantially more vulnerable to heavy ion-induced SEB than its DMOSFET counterpart. These quantitative comparisons align with recent findings showing that similarly rated Si UMOSFETs are more vulnerable to premature multiplication effects induced by monoenergetic neutrons and SEBs induced by quasi-atmospheric neutrons. Since SEB in Si devices is strongly dependent on impact ionization and avalanche multiplication, the results confirm that carrier multiplication directly affects the radiation hardness of Si-based UMOSFETs in harsh environments. TCAD simulations attribute the increased SEB sensitivity of UMOSFETs to intense electric fields near the trench gate corners, which enhance the impact ionization process. Exploring new approaches to mitigate electric field concentrations at trench gate corners, combined with optimized buffer layer design, may substantially improve the SEB robustness of future Si-based UMOSFET devices. Our experimental data reveal a clear SEB vulnerability in Si UMOSFETs that contrasts with the documented SEB robustness of SiC UMOSFETs when both are compared to their DMOSFET counterparts. Consequently, this significant divergence provides strong evidence for fundamentally distinct SEB mechanisms between Si- and SiC-based power devices, as a recent study suggests.

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