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Analysis and Modeling of a 650 V GaN-based Half Bridge during Short Circuit operation

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Simone

Abstract

Following the vision of a green and sustainable future, the use of Wide Band Gap (WBG) semiconductors in Power Electronics is of paramount importance, since their physical properties enable the achievement of the highest performances in the energy conversion processes in terms of efficiency and power density. Silicon Carbide (SiC) power MOSFETs are now the leaders of the industrial, renewable and automotive markets thanks to their wide range of breakdown voltages (650-, 1200-, 1700- V), low on-resistance and fast switching times. At the same time, they offer excellent performances in terms of robustness and reliability, key features for all commercial applications. However, SiC MOSFETs seem to have reached their technological limit, while even better performances can be reached using Gallium Nitride High Electron Mobility Transistors (GaN HEMTs), which have attracted significant interest in the industrial and academic communities in recent years. Even if GaN transistors were born as normally-on devices, finding space in radio- and audio-frequency applications, the possibility to obtain power devices with very low on-resistance and extremely fast switching characteristics has prompted the development of normally-off GaN devices for power applications. However, the lateral structure limits the maximum breakdown voltage to 650 V, while the lower thermal conductivity forces the operating temperature to be lower than 150 °C. Furthermore, the reliability and the Short Circuit (SC) robustness of GaN HEMTs are lower in comparison to SiC and Si devices, strongly reducing their advantages and preventing their widespread use in commercial applications.

In this perspective, this thesis focuses on the SC operation of a 650 V GaN-based Half Bridge (HB), evaluating the influence of various operating parameters, including the DC-link voltage and the gate resistance. The SC characterizations presented in the literature focus on a single device, often operating in conditions far from the real application, e.g. with a large gate resistor. The study proposed in this thesis investigates the real case of the SC operation of a HB, determining the impact that another identical device can have on the SC and the interactions between the two GaN HEMTs. From a comparative analysis of experimental results in the literature and preliminary simulation results, significant differences are noticed, leading towards the development of a model for the drain and gate current of the GaN HEMT under study. After designing and realizing a prototype test board, an I – V characterization is performed for the drain and gate current, whose results are used to derive simple behavioral models for both drain and gate currents, achieving good accuracy. The behavioral model developed for the GaN HEMT, suitable for both

nominal operating conditions and SC operation, is integrated with the manufacturer's LTSpice model and used to accurately simulate the behavior of the devices during the SC, giving also the possibility to determine the impact of the gate leakage current on the self-regulation mechanism of the SC current. Experimental SC tests are led on the realized board, confirming the theoretical analysis and highlighting the effects of the DC-link voltage, the impact of using large gate resistance and the presence of mismatches in the circuit of the two transistors. Moreover, the SC power and energy are computed and a temperature estimation is provided for both devices to evaluate the different electro-thermal stress on the GaN HEMTs. The proposed model is validated by comparing the LTSpice simulations with the experimental results in all the tested conditions. Finally, the possibility to exploit the proposed gate leakage current model to estimate the junction temperature of the GaN HEMT is investigated and is verified evaluating the temperature reached by the devices during the SC event.

Abstract
(Italiano)

Seguendo la visione di un futuro verde e sostenibile, l'uso di semiconduttori di tipo Wide Band Gap (WBG) nell'elettronica di potenza è di fondamentale importanza, poiché le loro proprietà fisiche consentono di ottenere le massime prestazioni nella conversione di energia in termini di efficienza e densità di potenza. I MOSFET di potenza al carburo di silicio (SiC) sono oggi i leader dei mercati industriali, delle energie rinnovabili e dell'automotive grazie alla loro ampia gamma di tensioni di bloccaggio (650-, 1200-, 1700- V), alla bassa resistenza in *on* e ai rapidi tempi di commutazione. Allo stesso tempo, offrono prestazioni eccellenti in termini di robustezza e affidabilità, caratteristiche fondamentali per tutte le applicazioni commerciali. Tuttavia, i MOSFET in SiC sembrano aver raggiunto il loro limite tecnologico, mentre prestazioni ancora migliori possono essere ottenute con i transistor ad alta mobilità elettronica al nitruro di gallio (GaN HEMT), che negli ultimi anni hanno suscitato un notevole interesse nella comunità industriale e accademica. Anche se i transistor in GaN sono nati come dispositivi normalmente accesi, trovando spazio nelle applicazioni di radio- e audio-frequenza, la possibilità di ottenere dispositivi di potenza con una resistenza in *on* molto bassa e caratteristiche di commutazione estremamente veloci ha spinto lo sviluppo di dispositivi in GaN normalmente spenti per applicazioni di potenza. Tuttavia, la loro struttura laterale limita la tensione massima di bloccaggio a 650 V, mentre la minore conducibilità termica costringe una temperatura di esercizio inferiore a 150 °C. Inoltre, l'affidabilità e la resistenza al cortocircuito (SC) degli HEMT sono inferiori rispetto ai dispositivi in SiC e Si, riducendo fortemente i loro vantaggi e impedendone l'uso diffuso nelle applicazioni commerciali.

In quest'ottica, il presente lavoro di tesi si concentra sul funzionamento in cortocircuito di un Half Bridge (HB) con dispositivi in GaN da 650 V, valutando l'influenza di vari parametri operativi, tra cui la tensione del DC-link e la resistenza di gate. Le caratterizzazioni in cortocircuito presentate in letteratura si concentrano su un singolo dispositivo, spesso operante in condizioni lontane dall'applicazione reale, ad esempio con una grande resistenza di gate. Lo studio proposto in questa tesi indaga il caso reale del funzionamento in cortocircuito di un HB, determinando l'impatto che può avere un altro dispositivo identico e le interazioni tra i due HEMT. Da un'analisi comparativa dei risultati sperimentali presenti in letteratura e dei risultati preliminari delle simulazioni, si notano differenze significative che hanno condotto allo sviluppo di un modello per la corrente di drain e di gate dell'HEMT oggetto di studio. Dopo aver progettato e realizzato

un prototipo per i test, è stata eseguita una caratterizzazione I - V per la corrente di drain e di gate, i cui risultati sono stati utilizzati per ricavare semplici modelli comportamentali per entrambe le correnti di drain e di gate, ottenendo una buona accuratezza.

Il modello comportamentale sviluppato per l'HEMT in GaN, adatto sia alle condizioni operative nominali che al funzionamento in cortocircuito, viene integrato con il modello LTSpice del produttore e utilizzato per simulare accuratamente il comportamento dei dispositivi durante il cortocircuito, dando anche la possibilità di determinare l'impatto della corrente di leakage di gate sul meccanismo di autoregolazione della corrente di cortocircuito. I test sperimentali in cortocircuito sono condotti sulla scheda realizzata, confermando l'analisi teorica ed evidenziando gli effetti della tensione del bus DC, l'impatto dell'utilizzo di una grande resistenza di gate e la presenza di differenze nel circuito dei due transistor. Inoltre sono calcolate la potenza e l'energia in cortocircuito ed è fornita una stima della temperatura per entrambi i dispositivi per valutare il diverso stress elettrotermico sugli HEMT. Il modello proposto è validato confrontando le simulazioni LTSpice con i risultati sperimentali in tutte le condizioni di test. Infine, viene studiata la possibilità di sfruttare il modello proposto per la corrente di leakage di gate per stimare la temperatura di giunzione dell'HEMT e viene verificata stimando la temperatura raggiunta dai dispositivi durante il cortocircuito.

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1
Overview on GaN HEMTs

1.1 Introduction

Last generation Wide Band-Gap (WBG) power devices are finding increasing use in power electronics applications, replacing the well-established Silicon (Si) power MOSFETs and IGBTs, as they can achieve higher performances in terms of efficiency and power density. Silicon Carbide (SiC) and Gallium Nitride (GaN), thanks to their superior properties, are the most employed semiconductor materials for the realization of WBG power devices [1], [2].

SiC technology has already reached a high maturity level, enabling the possibility to operate in a wide range of power and voltage levels with high thermal stability, robustness and reliability. In fact, in the last years it has become the preferred solution for many industrial, automotive and grid-tied applications [3]-[5]. On the other hand, GaN-based transistors are in fast and promising development and are introduced as a very hard and mechanically stable semiconductor. With potential higher breakdown strength, faster switching speed, higher thermal conductivity and lower on-resistance, GaN High Electron Mobility Transistors (GaN HEMTs), significantly outperform Si-based devices and are a valuable alternative to SiC MOSFETs in lower voltage applications. GaN HEMTs enable the achievement of increasing efficiency and power density of power converters, though trying to maintain the same level of reliability reached with Si and SiC technologies [6]-[8].

Even if GaN HEMTs were initially adopted in Radio-Frequency applications, now they are also spreading in consumer electronics, data centers, audio amplification and low voltage industrial and automotive applications, such as motor drives, wireless power

transfer and on-board chargers [9]-[14], also because of the technology improvement in realizing normally-off GaN devices. In particular, GaN HEMTs are employed in many DC-DC converter topologies, both isolated, such as Flyback, DAB and resonant converters, and non-isolated as Buck, Boost and Buck-Boost [15]-[21].

Nevertheless, some factors still limit the spread of GaN HEMTs in all the fields of power electronics. They are mainly linked to the relatively low breakdown voltage and reliability and robustness issues. The first factor is dependent on the lateral structure of GaN devices, which limits the maximum breakdown voltage to about 650 V for HEMTs and 900 V for cascode devices and does not enable the avalanche capability [22], [23]. Some promising GaN transistors with a vertical structure have recently been developed in order to overcome this limitation, showing 1.2 kV breakdown voltage, avalanche capability and high robustness [24], [25], but they are still far from the commercial market and a widespread use.

The major causes of reliability issues in GaN HEMTs are related to charge trapping and hot electrons, that heavily degrade the device performances, both in its on- and off-state. The main processes related to charge trapping and hot electrons involve the dynamic on-resistance increase, the threshold voltage shift and the degradation of the gate [26]-[28]. The presence of charge traps derives from imperfections in the structure of the device, that can be induced by the realization process, and can be localized at different locations and energy levels [29]-[30]. Hot electrons can be generated by highly stressful operating conditions and the simultaneous presence of high voltage and current, as during the hard-switching event [26]-[28], [31], [32].

Moreover, another relevant issue of GaN HEMTs is linked to the Short Circuit (SC) robustness. Many studies and findings have been conducted in recent years on the SC behavior of GaN devices: from the capability, degradation and withstand time tests [33]-[36], to instability [37]-[39] and failure mechanisms analysis [40], [41]. Considering devices with 650 V breakdown voltage, GaN HEMTs show good SC ruggedness for voltages lower than 350 V, but at higher voltage they suffer of unrecoverable breakdown, showing lower SC capability in comparison with SiC and Si MOSFETs. The failure time in these conditions is less than 1 μs, making the design of a protection circuit against SC for GaN HEMTs a challenge. This is even more complicated because of the absence of a simple but reliable analytical model of the GaN HEMT that represents its behavior in SC conditions and that allows the designer to accurately predict the SC behavior without performing experimental tests and damaging the transistors, saving time and costs. Moreover, all the experimental SC tests presented in the literature are performed on a single device, sometimes connected in series to a higher current power device acting as a protection. However, in practical applications, the SC event can be triggered in Half Bridge-based topologies and involves two identical devices. The presence of two identical

GaN HEMTs during the SC event is not investigated in the literature, even if this can lead to relevant differences in the electro-thermal stress distribution between the two devices.

In this perspective, this thesis focuses on the Short Circuit behavior of normally-off GaN HEMTs for power converters applications. In particular, the SC operation of a Half Bridge is presented and analyzed through simulations and experimental tests. A PCB with two 650 V–60 A GaN HEMTs in Half Bridge configuration has been designed and realized to perform the I – V characterization and SC tests. A static I–V characterization of drain and gate currents has been led on the 650 V–60 A GaN HEMT at different operating conditions in order to derive a behavioral model for the drain and gate currents, suitable for the device simulation both during normal and SC operation of the device. The proposed model is used to simulate and predict the real SC behavior of the GaN devices, determining the main information about the SC event, such as the peak power dissipation, the involved energy and the junction temperature. Moreover, the model can be an useful instrument in designing a protection circuit against SC for GaN HEMTs. Experimental SC tests are performed at different bus voltages and with two values of gate resistance to validate the model and its applicability to other GaN HEMTs with different characteristics is evaluated.

1.2 Thesis outline

The outline of the thesis follows this structure:

- **Chapter 1** provides an introductive overview on the main features, the modeling approaches and the state-of-the-art of SC characterization of GaN HEMTs.
- **Chapter 2** introduces the analysis of the SC behavior of a GaN-based Half Bridge, highlighting the main phenomena involved during the SC and evaluating the effects of many circuit parameters on the SC behavior.
- **Chapter 3** describes the design process of the PCB used to perform all the experimental tests presented in the thesis.
- **Chapter 4** describes the procedure adopted to perform the experimental drain and gate I – V characterization and shows the obtained results on a 650 V – 60 A GaN HEMT. Based on these results, a behavioral model for the drain and gate currents of the GaN HEMT is proposed. Then, the accuracy of the model is evaluated.
- **Chapter 5** presents the implementation of the proposed model in SPICE, its comparison with the manufacturer model and its validation with experimental

results of non-destructive SC tests at different operating conditions. The model is then applied to a different GaN HEMT to evaluate its scalability and adaptability.

- **Chapter 6** summarizes the main results and contributions of the thesis, finally providing the conclusion and future outlooks.

1.3 Research contributions

Many research topics have been faced during the Ph.D. program, focusing on different fields of power electronics. In particular, I was devoted to the design, testing and optimization of power converters for railway applications and their integration with WBG power devices. These research activities were led in cooperation with two leading companies of the Italian railway field, such as Rete Ferroviaria Italiana (RFI s.p.a.) and Hitachi Rail. In the last part of my Ph.D. program I also focused on the robustness and the SC behavior of GaN HEMTs for their application in power converters.

The research contributions of my activity, published in international conference proceedings and scientific journals, are listed in the following.

Journal Papers

- S. A. Mortazavizadeh, S. Palazzo, A. Amendola, E. De Santis, D. Di Ruzza, G. Panariello, A. Sanseverino, F. Velardi and G. Busatto, "High Frequency, High Efficiency, and High Power Density GaN-Based LLC Resonant Converter: State-of-the-Art and Perspectives," Appl. Sci. 2021, 11, 11350. https://doi.org/10.3390/app112311350.
- C. Abbate, L. Colella, R. Di Folco, G. Busatto, E. Martano, S. Palazzo, A. Sanseverino and F. Velardi, "An Accurate Switching Current Measurement Based on Resistive Shunt Applied to Short Circuit GaN HEMT Characterization," Appl. Sci. 2021, 11, 9138. https://doi.org/10.3390/app11199138.

Conference Papers

- S. Palazzo, G. Busatto, E. De Santis, R. Giacomobono, D. Di Ruzza and G. Panariello, "A Hybrid Modulation Technique for Voltage Regulation in LLC Converters in the Presence of Transformer Parasitic Capacitance," 2022 IEEE

Energy Conversion Congress and Exposition (ECCE), 2022, 1-8, doi: 10.1109/ECCE50734.2022.9947909.

- G. Panariello, D. Di Ruzza, M. Canigliula, S. Palazzo, G. Busatto, E. De Santis, "Energy Efficient Architecture of Power Supply for Field Devices and Controllers of the RFI Computer-Based Interlocking," World Congress on Railway Research (WCRR), 2022, Birmingham, UK.
- D. Marciano, S. Palazzo, G. Busatto, A. Sanseverino and F. Velardi, "Role of Active Clamp Circuit in a DC/AC Isolated Converter based on the principle of Pulsating DC Link," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, 2704-2709, doi: 10.1109/ECCE47101.2021.9595012.
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- F. Calabrò, D. Bravo, C. Carissimo, E. Di Fazio, A. Di Pasquale, A.A.M.O. Eldray, C. Fabrizi, J.G.S. Gerges, S. Palazzo, J.F.F.T. Wassef, "Null rules for the detection of lower regularity of functions," Journal of Computational and Applied Mathematics, Volume 361, 2019, 547-553, doi: 10.1016/j.cam.2019.05.002.

In submission

- S. Palazzo, T. Pereira, Y. Pascal, G. Busatto and M. Liserre, "A Behavioral Model for Short Circuit Operation of a GaN-based Half Bridge," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), 2023, digest submitted.

1.4 GaN HEMTs in Power Electronics

The use of WBG devices in Power Electronics starts from the need to overcome the limitations of Silicon devices, which have now reached their technological limit. Instead, WBG materials like Silicon Carbide (SiC) and GaN can be used in realizing devices with superior breakdown voltage, switching efficiency, lower on-resistance and smaller size thanks to their physical properties, as can be seen comparing the key material properties of Table 1.1 [7].

Table 1.1 Key physical properties of Si, SiC and GaN.

Parameter	Si	SiC	GaN
Band Gap [eV]	1.12	3.26	3.39
Critical Field [MV/cm]	0.23	2.2	3.3
Electron Mobility [cm^2/V·s]	1400	950	1500
Permittivity	11.8	9.7	9
Thermal Conductivity [W/m·K]	$15 \cdot 10^{-3}$	$38 \cdot 10^{-3}$	$13 \cdot 10^{-3}$

The wider band gap energy of GaN results in a higher critical electric field and thus in a higher breakdown voltage, according to the approximated formula:

$$V_{BD} = \frac{1}{2} W_d E_c \tag{1.1}$$

where V_{BD} is the breakdown voltage, W_d is the drift region and E_c is the critical electric field. Hence, for the same breakdown voltage the drift region of a GaN device can be more than 10- and 1.5- times smaller than a Si or SiC one, respectively. This also leads to the reduction of the on-resistance $r_{DS,on}$, whose theoretical value for unit area can be expressed as:

$$r_{DS,on} = \frac{W_d}{q\mu_n N_D} \tag{1.2}$$

where q is the electron charge, μ_n is the electron mobility and N_D is the total number of electrons in the region.

A straightforward indication of the performances of the power devices can be obtained expressing the theoretical on-resistance in relation to the breakdown voltage, according to:

$$r_{DS,on} = \frac{4V_{BD}^2}{\varepsilon_0 \varepsilon_r E_c^3} \tag{1.3}$$

which is obtained combining (1.1) with the Poisson's equation $qN_D = \varepsilon_0 \varepsilon_r E_c / W_d$, where ε_0 is the vacuum dielectric constant. According to (1.3), it is possible to derive the ideal graph of Fig. 1.1 that compares the capability for Si-, SiC- and GaN-based power devices, showing how GaN HEMTs can theoretically achieve higher blocking voltages with a lower on-resistance.

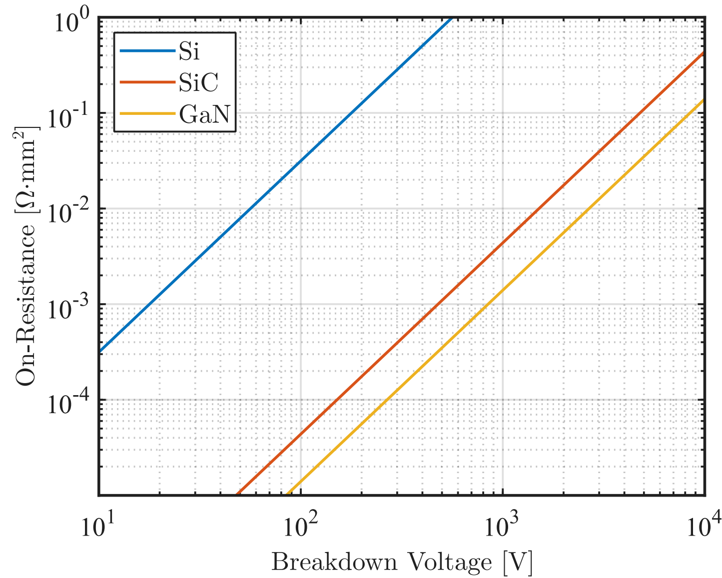
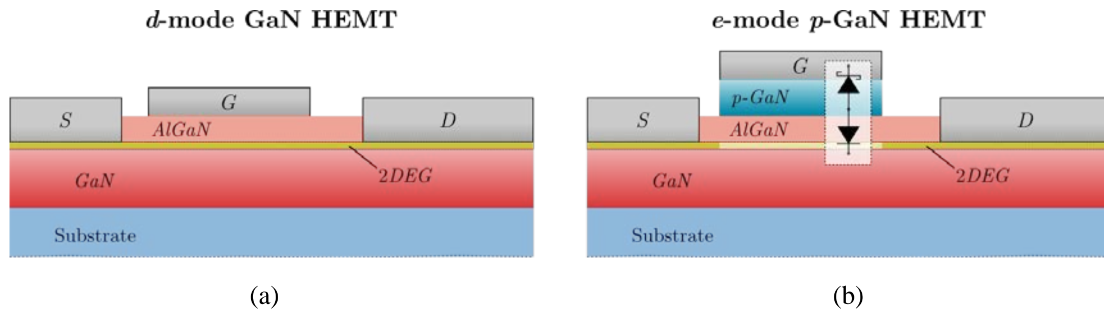


Fig. 1.1 Theoretical curves of specific on-resistance vs. blocking voltage for Si, SiC and GaN technology

1.4.1 Basic structures

One of the most important feature of the GaN HEMT derives from the chemical structure of GaN, called wurtzite, that is very chemically stable and mechanically robust, also confering to GaN some piezoelectric properties. When an AlGaN layer is made grown on the GaN crystal, a very high conductive region is formed at their interface, called two-dimensional electron gas (2DEG). The mechanisms leading to the formation of the 2DEG are mainly related to the spontaneous polarization, caused by the intrinsic asymmetry of the chemical bonds in the hexagonal wurtzite structure at the AlGaN-GaN interface, and to the piezoelectric polarization, that is caused by the mechanical compression of AlGaN on the GaN layer and generates an electric field. Therefore, a spontaneous layer with conductive electrons exists at the AlGaN-GaN interface and the confinement of the electrons in this very thin region increases their mobility up to 1500-2000 $cm^2/V \cdot s$.

The spontaneous formation of the 2DEG causes the GaN transistor to be intrinsically a *normally-on* device, with the possibility to interrupt the current flow between source and drain contacts applying a negative gate voltage respect source and drain, realizing a depletion-mode (d-mode) transistor, as shown in Fig. 1.2 (a). However, in power electronics applications, it is desirable to work with normally-off devices in order to avoid undesired Short Circuit at the start-up of converters, simplify the control logic and ensure safety. For this reason, many technological solutions have been used to make *normally-off* GaN transistors, with the basic concept to create a potential barrier at the AlGaN-GaN



(a) (b)

Fig. 1.2 Basic structures of the GaN HEMT: (a) depletion-mode GaN HEMT: the 2DEG is spontaneously formed at the AlGaN-GaN interface; (b) enhancement-mode p-GaN HEMT: the presence of a Schottky barrier inhibits the spontaneous formation of the conductive channel.

interface. This barrier can be lowered controlling the gate voltage to form the conductive channel between source and drain, to realize in such a way an enhancement-mode (e-mode) transistor. The most common solutions used to achieve this goal are [42]-[45]:

- recessed gate
- implanted gate
- p-doped GaN gate
- cascode configuration

Among these, the most common solution is the p-doped GaN gate, which consists in placing a positively charged GaN layer between the AlGaN and the gate metal contact. There are two types of gate contacts: ohmic and Schottky. The ohmic contact is typically used for low-power applications, where the gate voltage is small and the gate leakage current is not a significant issue, while Schottky contacts are typically used in high-power applications where a large gate voltage is required, providing better thermal stability but suffering of higher gate leakage current.

When the Schottky junction is formed underneath the gate, a potential barrier to the spontaneous formation of the 2DEG is created, realizing a normally-off device. The simplified structure of the Schottky-type p-GaN HEMT is shown in Fig. 1.2 (b). Because of the presence of the metal – p-GaN interface and the p-GaN – AlGaN – GaN interface, two back-to-back diodes are formed at the gate, as highlighted in Fig. 1.2 (b) [46].

1.4.2 Electrical characteristics

The e-mode p-GaN HEMT can be turned-on, as a MOSFET, with a positive Gate-to-Source voltage V_{GS} exceeding the threshold voltage $V_{GS,th}$, that is normally in the range 0.7 – 2 V. On the contrary, it can be fully turned-off with zero V_{GS}, giving also the

possibility to avoid providing another supply voltage level on the driver circuit, even if this exposes the GaN HEMT to be more sensitive to voltage spikes on the Gate, demanding a particular attention to the layout design. Driving the Gate with a negative voltage is still feasible, but it increases the reverse conduction losses. In fact, even if there is not a body diode like in MOSFETs, the reverse conduction is still possible in GaN HEMTs thanks to their symmetric structure. As the 2DEG channel can be formed when $V_{GS} > V_{GS,th}$, the same can happen when the Gate-to-Drain voltage V_{GD} exceeds its

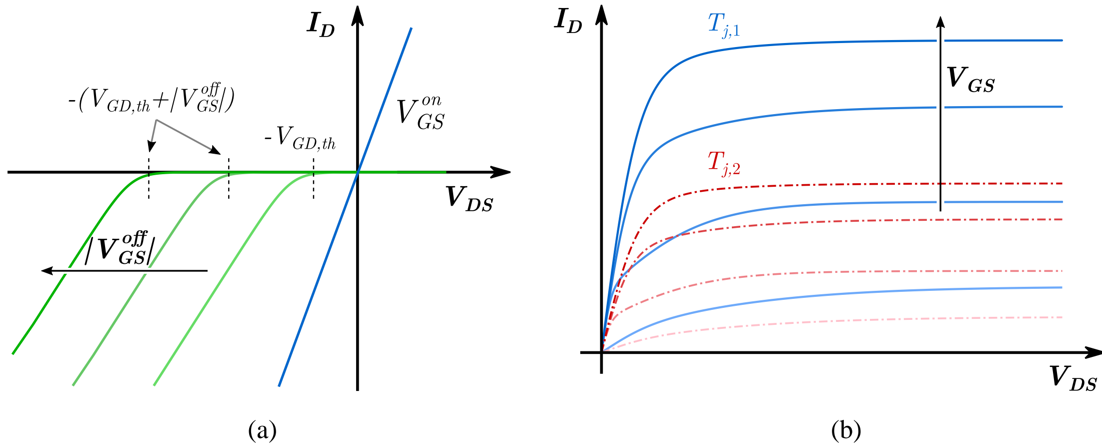


Fig. 1.3 Qualitative Reverse (a) and Forward (b) conduction characteristics of the e-mode GaN HEMT. The reverse conduction is characterized by a voltage drop at least equal to $V_{GD,th}$, to which the value of V_{GS} is added if a negative voltage is used to turn-off the device. In the Forward conduction, the increase of temperature from $T_{j,1}$ to $T_{j,2}$ causes the increase of the $r_{DS,on}$ and the reduction of the saturation current.

relative threshold $V_{GD,th}$. However, the reverse conduction is characterized by a higher voltage drop than the diode forward voltage of the MOSFET, in the range of 3 – 5 V. This voltage drop is given by the quantity $\left(V_{GD,th} - V_{GS}^{off}\right)$, which therefore increases if the HEMT is turned off with a negative $V_{GS} = V_{GS}^{off}$, causing excessive conduction losses.

However, since the reverse conduction behavior is not linked to the presence of a body diode, there is no reverse recovery and the related losses are then zero [7], [47]. The qualitative ideal reverse conduction characteristics for the GaN HEMT are shown in Fig. 1.3 (a).

Focusing on the output characteristics, during the forward conduction two regions can be observed:

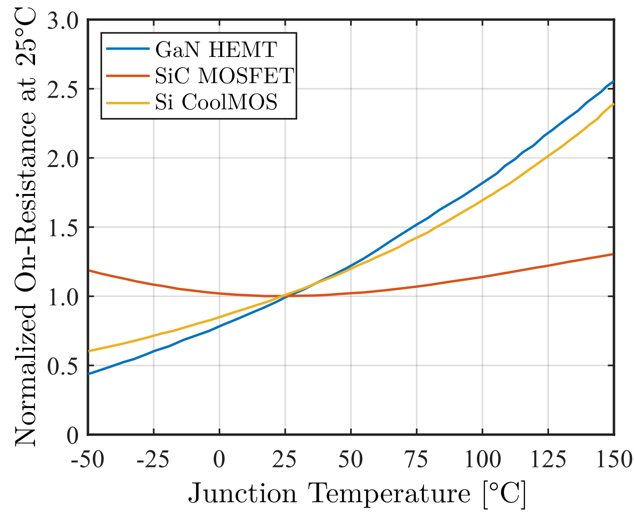


Fig. 1.4 Comparison of normalized $r_{DS,on}$ in function of the junction temperature for three different 650 V power devices: GaN HEMT GS66516T by GaN Systems, SiC MOSFET IMZA65R027M1H by Infineon and Si CoolMOS IPW65R019C7 by Infineon. The variation of $r_{DS,on}$ is larger for GaN and Si transistors than the SiC MOSFET.

1. A *linear region*, where the GaN HEMT behaves like a variable resistance, defined by the $r_{DS,on}$ that is dependent on the V_{GS}, the junction temperature T_j and the Drain current I_D.
2. A *saturation region*, where the GaN HEMT behaves like a controlled current source, dependent on V_{GS}, V_{DS} and T_j.

As T_j increases, the $r_{DS,on}$ also increases and the $I_D - V_{DS}$ curves are downshifted towards lower values of Drain current. The qualitative output curves of the GaN HEMT are depicted in Fig. 1.3 (b) at the varying of V_{GS} and for two junction temperatures, namely $T_{j,1}$ and $T_{j,2}$, with $T_{j,2} > T_{j,1}$.

In general, the temperature variation of the $r_{DS,on}$ is larger in GaN HEMTs than in SiC MOSFETs, due to the weaker thermal properties of GaN. For example, Fig. 1.4 compares the variation of $r_{DS,on}$ with junction temperature from the nominal value at 25 °C for three power devices of different technology but with the same rated voltage of 650 V and very similar current ratings: a 59 A SiC MOSFET [48], a 75 A Si CoolMOS [49] and a 60 A GaN HEMT [50]. It is evident from the figure how the on-resistance of the GaN HEMT and the CoolMOS undergoes a greater variation, up to 2.5 times the nominal value at 150 °C, while the $r_{DS,on}$ of the SiC MOSFET remains quite close to its rated value and is about 40% greater at 150 °C. This issue is mainly related to the weaker thermal properties

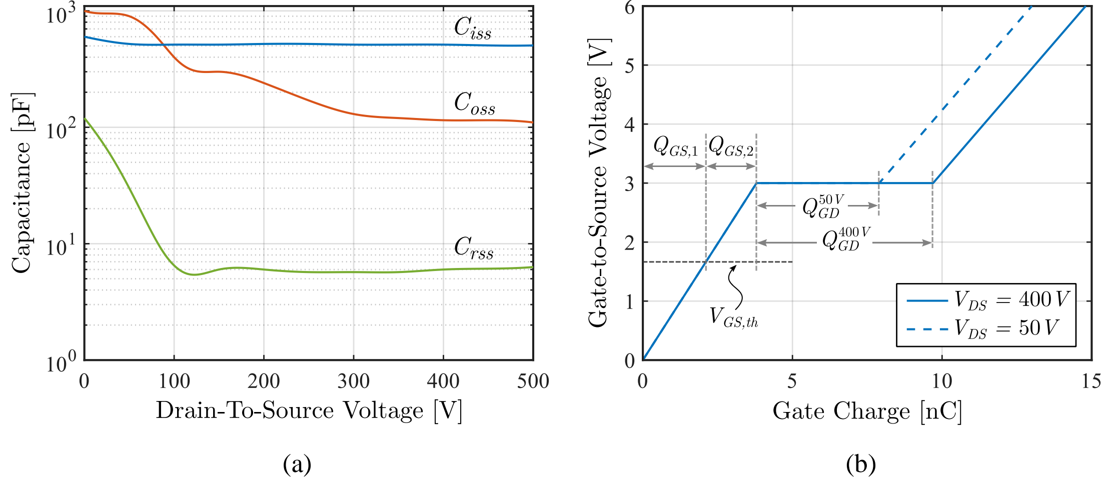
of GaN with respect SiC and prevents the use of GaN HEMTs in applications requiring high temperature operations, since the main advantages of GaN technology would be lost. So, especially for GaN HEMTs, it is crucial to adequately dissipate the heat generated during the operation in switching converters to keep T_j as low as possible in order to preserve the performances of the device.

1.4.3 Capacitance and charge

One of the greatest advantages of the GaN HEMT consists in the very low value of its capacitances, determining excellent switching performances of the device. Last generation MOSFETs are optimized to reach switching frequencies up to few hundreds of kHz [51] thanks to the reduction of the semiconductor area and, as a consequence, of the parasitic capacitances at the expense of a higher on-resistance, since the first are inversely proportional and the second are directly proportional to the semiconductor area. GaN HEMTs can operate up to the MHz range maintaining a low on-resistance thanks to their superior physical properties. The value of the capacitances strongly depends on the area between the source, drain and gate contacts and since for GaN HEMTs this is much smaller than for MOSFETs, lower values are obtained.

The capacitance determines the amount of charge needed to change the voltage between two terminals of the device, so lower capacitance leads to lower charge and a faster transition from one voltage level to another during the switching cycle. As in the MOSFET, three capacitances can be defined: the gate-to-source capacitance C_{GS}, the gate-to-drain capacitance C_{GD} and the drain-to-source capacitance C_{DS}. Looking into the gate with drain and source contacts shorted, the input capacitance is defined as $C_{iss} = C_{GS} + C_{GD}$ and in the same way, when gate and source are shorted, the output capacitance can be defined as $C_{oss} = C_{DS} + C_{GD}$. C_{GD} is commonly called transfer or Miller capacitance and indicated as C_{rss}. While C_{iss} is weakly dependent on the V_{DS}, C_{oss} and C_{rss} are a non-linear function of V_{DS} and can notably vary with it, as can be seen from Fig. 1.5 (a) that shows the input, output and reverse capacitances of the 650 V GaN HEMT GS66516T by GaN Systems [50].

The fast turn-on and turn-off switching transients of the GaN HEMT are achievable thanks to the very low amount of charge required by the input capacitance to switch the voltage across it. The dependence of the gate charge Q_G with the gate voltage V_{GS} is non-linear and its relationship for the 650 V GaN HEMT GS66516T is depicted in Fig. 1.5 (b). The total gate charge needed to drive the HEMT can be divided into different contributions, as highlighted in Fig. 1.5 (b), in which:



(a) (b)

Fig. 1.5 Drain-to-source voltage dependence of C_{iss}, C_{oss} and C_{rss} (a) and gate charge characteristic (b) of 650 V GaN HEMT GS66516T by GaN Systems.

- Q_{GS} is the charge required to increase the voltage from zero to the plateau and can be defined as $Q_{GS} = Q_{GS,1} + Q_{GS,2}$, where $Q_{GS,1}$ and $Q_{GS,2}$ represent the charge required to increase V_{GS} up to the threshold voltage and from the threshold voltage to the plateau level, respectively.
- Q_{GD}, also called Miller charge, is the charge required to commutate the HEMT's drain voltage and to enter the linear region of the $I_D - V_{DS}$ characteristic. Q_{GD} varies with the V_{DS} and its value can be obtained as

$$Q_{GD}(V_{DS}) = \int_0^{V_{DS}} C_{rss}(v)\, dv \tag{1.4}$$

where V_{DS} is the voltage to be commutated.

- After providing the amount of charge $Q_{GS} + Q_{GD}$, a further increase is required to reach the desired gate voltage: as it can be seen from Fig. 1.5 (b), if $V_{GS} = 5$ V is the desired voltage, the total charge that must be provided is about 13 nC for $V_{DS} = 400$ V.

GaN HEMTs enable very high frequency operations, so the voltage and current waveforms can be characterized by high *dv/dt* and *di/dt* during the switching cycle. When using Half Bridge-based topologies the high *dv/dt* at the switching node may cause the false turn-on of the off-state device, since during the voltage transition the current can flow in its C_{GS}, that is connected to the drain through the Miller capacitance C_{GD}. In many

cases this fact causes shoot-through, noise and additional power dissipation and eventually it can lead to the Short Circuit of the Half Bridge [52], [53]. One of the key parameters that should be considered to prevent this undesired issue is the Miller ratio, defined as the ratio $Q_{GD}/Q_{GS,1}$. The safe operation of the GaN HEMT is ensured and the false turn-on can be avoided if the Miller ratio is less than unity in all the operating conditions [7].

The output capacitance C_{oss} plays an important role in determining the switching behavior of the HEMT, since it is involved in the energy exchange with the other passive components of the circuit. To avoid hard-switching losses, Zero Voltage Switching (ZVS) is commonly used in power converters, exploiting the presence of an inductive current to discharge the output capacitances of the GaN HEMTs during the deadtime before turning them on. The ZVS behavior of the power device is strongly influenced by C_{oss}, since the necessary condition to achieve ZVS is expressed by [54]:

$$\frac{1}{2}LI^2 \geq Q_{oss}(V_{DC}) \cdot V_{DC} \tag{1.5}$$

where L is the inductor providing the current I in the bridge, V_{DC} is the bus voltage and Q_{oss} is the charge stored in C_{oss}, that depends on V_{DC}. As previously mentioned, C_{oss} is a non-linear function of V_{DS}, but it is possible to define a charge-equivalent linear capacitance $C_{oss,Q}$ that provides the same value of Q_{oss} for each V_{DS} as:

$$C_{oss,Q} = \frac{\int_0^{V_{DS}} C_{oss}(v)dv}{V_{DS}} = \frac{Q_{oss}(V_{DS})}{V_{DS}} \tag{1.6}$$

Combining (1.5) and (1.6), with $V_{DS} = V_{DC}$, the ZVS condition can be expressed as:

$$\frac{1}{2}LI^2 \geq C_{oss,Q}(V_{DC}) \cdot V_{DC}^2 \tag{1.7}$$

If the condition found in (1.7) is not fulfilled, incomplete soft-switching occurs on the device that is turning on causing high power dissipation, since its C_{oss} is not fully discharged.

1.4.4 Figure of Merit

It is convenient to use a unique parameter to evaluate and compare the performances of power transistors to take the best choice for an application. The Figure of Merit (FOM) permits to compare the key features of transistors of different technologies according to the minimum hard-switching losses achievable for each technology. Many ways to define

the FOM have been proposed in the literature [55]-[59], starting from the computation of the minimum possible power dissipation during the switching cycle.

The power dissipated in a switch can be divided into two components: the conduction losses and the switching losses. The first represents the power dissipated on the on-resistance during the conduction interval of the switch and is equal to $r_{DS,on}I^2$. The second term is dependent on the switching frequency, the voltage and current to be commutated, the output capacitance, the reverse recovery and the reverse conduction. It becomes quite difficult to consider all these parameters when computing the total power loss and the FOM, but it is necessary to perform a coherent evaluation on the performances of the power device.

One of the most complete FOM formulation, named Hard-Switching-FOM (HSFOM), is proposed in [59] and is defined as:

$$HSFOM = \frac{1}{\sqrt{r_{DS,on}Q_{oss}} + k\tau_{rr}\sqrt{f_{sw}V_{sw}}} \tag{1.8}$$

in which f_{sw} is the switching frequency, V_{sw} is the voltage that must be commutated, τ_{rr} is the reverse-recovery time and k is a parameter dependent on the topology of the converter considered for the FOM computation. The HSFOM takes into account all the power loss contributions described above, but it requires a great effort for its computation and moreover is topology-dependent.

GaN HEMTs do not have the body diode, so the reverse-recovery time and the related losses are zero. This leads to the simplification of (1.8) when computing the FOM for GaN devices, that becomes:

$$HSFOM = \frac{1}{\sqrt{r_{DS,on}Q_{oss}}}. \tag{1.9}$$

In this case, a useful FOM definition can be found in [55], where the key parameters used to determine the performances of the device are $r_{DS,on}$ and $C_{oss,Q}$, that only depend on the device properties and, for this reason, this FOM is also named Device-FOM (DFOM). It is defined as:

$$DFOM = \frac{1}{\sqrt{r_{DS,on}C_{oss,Q}}}. \tag{1.10}$$

Moreover, the DFOM is independent from the semiconductor area A_{semi}, since $r_{DS,on}$ is proportional to $1/\mathrm{A_{semi}}$ and $C_{oss,Q}$ is proportional to A_{semi}.

A comparative analysis of $r_{DS,on}$ and $C_{oss,Q}$ has been performed in this section considering three power devices families of different technologies with 650 V breakdown voltage: GaN HEMTs by GaN Systems, SiC MOSFETs and Si CoolMOS transistors by Infineon. Six devices for each family have been considered and the $r_{DS,on} - C_{oss,Q}$ values have been extracted from the datasheets at $V_{DS} = 400$ V and two junction temperatures, 25 °C and 150 °C, and they are plotted in Fig. 1.6. The circles and the squares represent the single power devices at 25 °C and 150 °C, respectively, while the lines show the linear regression of the computed values and are used to compare the performances of the different technologies, since they are directly related to the DFOM, representing the points at which the product $r_{DS,on}C_{oss,Q}$ is constant. Lower lines in the graph indicate better performances of the device, so it is evident how WBG devices outperform Si MOSFETs and, in particular, GaN HEMTs show the best FOM at 25 °C.

However, at $T_j = 150$ °C GaN HEMTs experience a greater increase of $r_{DS,on}$ than SiC MOSFETs, which therefore still represent the most suited technology for high-temperature operations. However, even if the DFOM provides fast and meaningful results in first analysis, for a correct and complete comparison with GaN HEMTs, the contribution of the reverse-recovery time and the switching frequency should be considered in the computation of the FOM for SiC MOSFETs and (1.8) should be used.

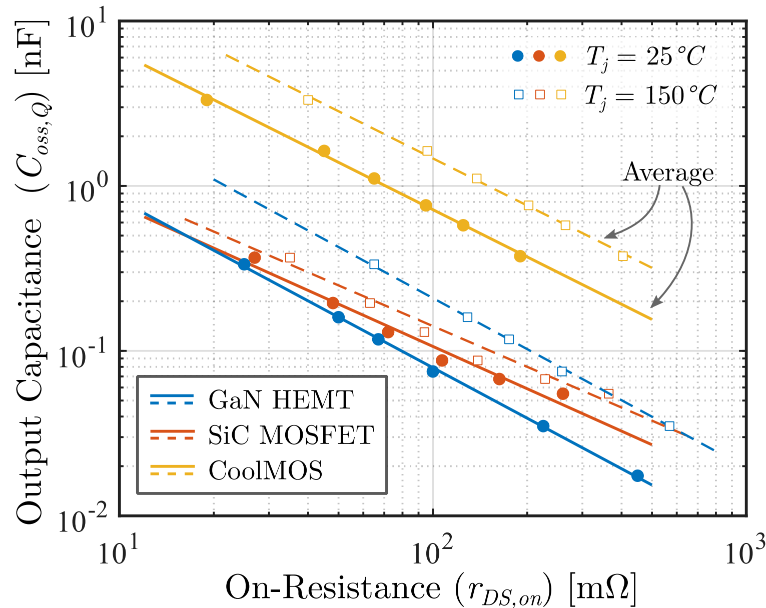


Fig. 1.6 Figure of Merit for different technologies of 650 V power devices: GaN HEMT by GaN Systems, SiC MOSFET and Si CoolMOS by Infineon. WBG technology greatly outperforms Si-based technology. GaN HEMTs show the best FOM at $T_j = 25$ °C but their performances deteriorate at $T_j = 150$ °C, where SiC MOSFET still represent the best solution.

1.4.5 Modeling of GaN HEMTs

The modeling of power devices is often a complex process and requires a great effort to achieve a highly accurate and time-saving solution. At the same time it is necessary to have a reliable model of the real power device, since it could be used to perform simulations and power losses analysis, and also to provide an useful instrument to understand and improve the technology of power devices. Depending on the final goal and the application field, numerous modeling approaches have been proposed [60], listed here in order of increasing accuracy and complexity:

- behavioral models
- semi-physical models
- physics-based models
- semi-numerical models
- numerical models.

Behavioral models are computed starting from the experimental tests on the device and deriving a function that describes its behavior through the fitting of many parameters, that have no direct physical meaning. These model, though the simplest ones in terms of time and computational complexity, are the less accurate since neglect many real aspects of the device that can take place during its operation. Moreover, they are quite dependent on the condition at which are computed, so a change in the operating condition may cause loss of accuracy.

Semi-physical models take some advantages from both behavioral and physics-based models. The equations describing the behavior of the device are derived from physics and adapted through the fitting of some parameters. These model are normally used in simulation environments such as SPICE and are mainly intended to application-level simulations, e.g. to analyze power converter topologies or evaluate power losses and efficiency with an acceptable level of accuracy.

Physics-based models are based on the physical phenomena involved in the semiconductor device and are derived solving the related physical equations. This requires the knowledge of semiconductor physics, as well as a big effort in writing and solving the analytical equations, and therefore they are intended for device-level simulations.

Semi-numerical and numerical models are based on the knowledge of semiconductor physics, device geometry and material properties. The physical equations are then solved through numerical methods like Finite Element Analysis. These numerical models are used by software such as Sentaurus, TCAD and SILVACO and are the most complex and

accurate, providing an important tool to analyze power semiconductor and improve their technology.

The models of GaN HEMTs presented in the literature are for the majority behavioral and physical ones and many of them were developed for the d-mode GaN HEMTs and then adjusted for e-mode HEMTs [61]-[66]. Recently, two physics-based models became industry-standard for the compact modeling of radio-frequency and high voltage GaN HEMTs: the Massachusetts Institute of Technology (MIT) virtual source GaN HEMT model (MVSG) [67] and the advanced SPICE model (ASM) [68], [69]. In this last one, the classic SPICE semi-physical approach is replaced by an accurate numerical model, which includes also nonlinear phenomena, such as the charge trapping. The charge trapping mechanism attracted a lot of interest from the modeling perspective, since it strongly impacts the dynamic response and the performances of GaN HEMTs. Therefore, many physical approaches have also been introduced in the literature to model the charge trapping [64], [69]-[72].

With the increasing development of Artificial Intelligence (AI), some behavioral models based on Artificial Neural Networks (ANN) have also been proposed in the last years, showing good adaptability to GaN HEMTs of different manufacturers [73], [74].

The GaN HEMTs' manufacturers usually provide a SPICE model of their devices, as is the case of Infineon, EPC and GaN Systems [75], [76]. These models are based on the experimental characterization of the transistors led by the manufacturers and are intended for the simulation of the GaN HEMTs in power converters, guaranteeing good accuracy and low computation time. In general, they consist of an electro-thermal network that includes both the main electrical and thermal relations of the device, as shown in Fig. 1.7. The model contains the parasitic resistances and inductances at gate (G), drain (D) and source (S) contacts, while the capacitances C_{GS}, C_{GD} and C_{DS} are modeled as variable charge sources dependent on the voltages V_{GS}, V_{GD} and V_{DS}. The drain current I_D is represented by a controlled current source, dependent on V_{GS}, V_{DS} and T_j and it is used to compute the instantaneous power dissipation $P_D = V_{DS}I_D$, that is the input for the thermal network along with the ambient temperature T_{amb}. The thermal network is generally modeled according to the Cauer thermal model, consisting of different cascaded RC cells, corresponding to an equivalent representation of the measured thermal resistances and capacitances between junction and case.

Depending on the desired level of accuracy, various simplifications can be made in the model, such as neglecting the thermal model or the presence of parasitic inductances. However, since the performance of the GaN HEMT is highly dependent on the temperature, neglecting the thermal model would lead to unrealistic results or incorrect analysis.

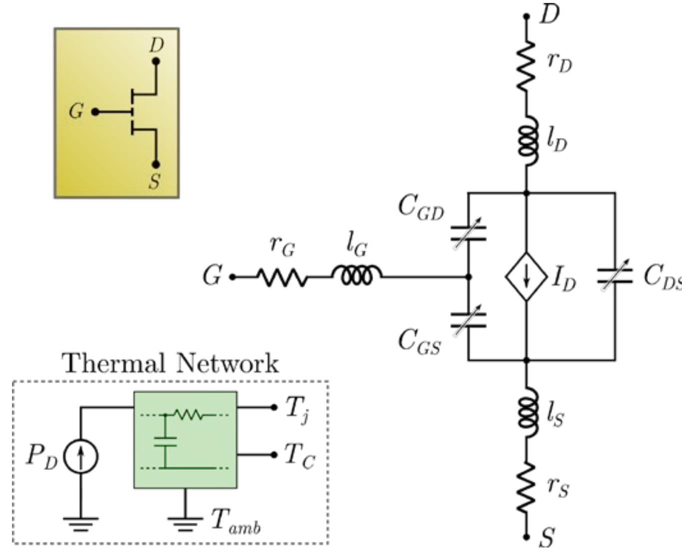


Fig. 1.7 General equivalent model for SPICE provided by GaN HEMTs' manufacturers.

As an example, the SPICE model of the 650 V – 60 A GaN HEMT by GaN Systems, available in [50], provides two levels of accuracy. The complete model, including the thermal network, will be briefly presented here, as it will be the starting point of the discussion led in Chapter 4.

All the parameters used in the model are listed in Table 1.2. The drain current of the device for $V_{DS} > 0$ and $V_{DS} < 0$ is expressed by equations (1.11) and (1.12), respectively:

$$I_D = c\left[a_1 - a_2\left(T_j - T_0\right)\right] \cdot ln\left(1 + e^{k(V_{GS}-V_{th})}\right) \cdot \frac{V_{DS}}{1 + f(V_{GS}) \cdot V_{DS}} \tag{1.11}$$

$$I_D = -c\left[a_1 - a_2\left(T_j - T_0\right)\right] \cdot ln\left(1 + e^{k(V_{GD}-V_{th})}\right) \cdot \frac{V_{SD}}{1 + f(V_{GD}) \cdot V_{SD}} \tag{1.12}$$

where the functions $f(V_{GS})$ and $\mathrm{f}(V_{GD})$ are of the form $f(v) = x_0 + x_1(v + x_2)$. The temperature dependence of the on-resistance is modeled by two variable resistors placed in series to the I_D current source, one on the drain side and another on the source side. The equations for the model of these two variable resistances are:

$$r_D = I_D \cdot sh_d \cdot m_{res} \cdot \left(1 - r_{Tc} \cdot \left(T_j - T_0\right)\right) + gan_{res}\left(\frac{T_j + 273}{T_0 + 273}\right)^{g_{Tc}} \tag{1.13}$$

$$r_S = I_D \cdot sh_s \cdot m_{res} \cdot \left(1 - r_{Tc} \cdot (T_j - T_0)\right) + gan_{res} \left(\frac{T_j + 273}{T_0 + 273}\right)^{g_{Tc}} \tag{1.14}$$

The capacitances among G, S and D are modeled as a variable charge source in parallel to a constant capacitance. The basic form of the equations used for C_{DS} and C_{GD} is:

$$Q(v) = \sum_{j=1}^{4} \alpha_{1j} \cdot ln\left(1 + e^{\alpha_{2j}(v+\alpha_{3j})}\right) \tag{1.15}$$

while the model of C_{GS} is expressed by:

$$\begin{aligned} Q(V_{GS}, V_{DS}) = \Bigg(\sum_{j=1}^{4} \beta_{1j} \cdot \left(1 - \frac{1}{1 + e^{\beta_{2j}(-V_{DS}+\beta_{3j})}}\right) + \\ + \sum_{j=1}^{4} \gamma_{1j} \cdot \left(\frac{1}{1 + e^{\gamma_{2j}(-V_{DS}+\gamma_{3j})}} - 1\right) \Bigg) \cdot V_{GS} \end{aligned} \tag{1.16}$$

which has to incorporate the dependence with both V_{DS} and V_{GS}. The constant parameters α_{ij}, β_{ij} and γ_{ij} used in (1.15) and (1.16), with i = 1, …, 3 and j = 1, …, 4, can be found in [50] and are not reported here for brevity.

Finally, the equivalent thermal model is represented through four RC cells according to the Cauer model, as shown in Fig. 1.8, where the case-to-ambient thermal resistance R_{C-amb} is also considered. The parameters $C_{\theta i}$ and $R_{\theta i}$ are the thermal capacitance and resistance of each cell and they are listed in Table 1.3, along with their time constants.

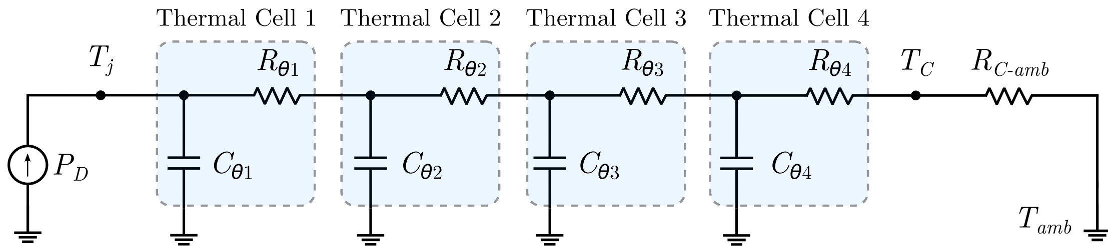


Fig. 1.8 Thermal model for the GaN HEMT GS66516T by Gan Systems.

Table 1.2 Parameters for drain current and on-resistance SPICE models of the GS66516T.

Symbol	***Value***	***Unit***			
T_0	25	°C			
Drain Current Model					
Symbol	***Value***	***Unit***	***Symbol***	***Value***	***Unit***
c	0.105	A/V	V_{th}	1.61	V
a_1	174.1	-	x_0	1.1	-
a_2	0.798	$°C^{-1}$	x_1	1.1	V^{-2}
k	26.0	V^{-1}	x_2	1.0	V
On-Resistance Model					
Symbol	***Value***	***Unit***	***Symbol***	***Value***	***Unit***
sh_d	0.943	A^{-1}	sh_s	0.052	A^{-1}
m_{res}	0.002	Ω	r_{Tc}	–0.004	$°C^{-1}$
gan_{res}	0.022	Ω	g_{Tc}	2.85	-

Table 1.3 Parameters for the thermal model of GS66516T.

Thermal Model					
Thermal Capacitance [Ws/°C]		***Thermal Resistance*** [°C/W]		***Time Constant*** [s]	
Symbol	***Value***	***Symbol***	***Value***	***Symbol***	***Value***
$C_{\theta 1}$	$1.4 \cdot 10^{-4}$	$R_{\theta 1}$	0.01	τ_1	$1.40 \cdot 10^{-6}$
$C_{\theta 2}$	$1.23 \cdot 10^{-3}$	$R_{\theta 2}$	0.14	τ_2	$172 \cdot 10^{-6}$
$C_{\theta 3}$	$10.8 \cdot 10^{-3}$	$R_{\theta 3}$	0.14	τ_3	$1.5 \cdot 10^{-3}$
$C_{\theta 4}$	$3.3 \cdot 10^{-3}$	$R_{\theta 4}$	0.01	τ_4	$33 \cdot 10^{-6}$

1.4.6 Reliability aspects

The extreme potential and the limitations of GaN technology have been investigated in detail during the last years in different application fields, from radio-frequency to power electronics. Despite excellent features reported for GaN HEMTs, some issues still undermine their performances and reliability, such as dispersion, trapping and parasitic effects, as well as long-term stability [28], [77], [78].

Charge trapping can occur due to a variety of factors, including defects in the device structure, surface states, and interface traps. The presence of defects in the structure of the device causes deep levels that can be dynamically filled by holes and electrons depending on the device operating conditions, affecting the local potential and leading to possible instability. Moreover, the energy levels of the defects as well as their physical location

can lead to different issues, such as the variation of the DC operating point in power amplification, the drain current collapse and threshold voltage and on-resistance shifts [28], [77]-[79].

The current collapse consists in the drain current reduction and in a decrease in device performance. The main cause of current collapse is the trapping of electrons in surface states or defects in the AlGaN/GaN heterojunction, leading to the reduction in the effective channel conductivity. Different mechanisms for current collapse have been proposed, including trap-assisted tunneling and impact ionization, and several solutions have been introduced to mitigate this phenomenon, such as passivation techniques and gate-recessed structures [80].

Dynamic on-resistance is another critical aspect in GaN HEMTs, that causes an increase of the on-resistance during switching operation. High values of $r_{DS,on}$ can lead to increased power dissipation and decreased efficiency. One of the main causes of dynamic-$r_{DS,on}$ is related to hot electrons, consisting in high-energy electrons that gain kinetic energy from the applied electric field. They are generated under high-voltage and high-frequency operation and cause degradation of the device, not only affecting the on-resistance, but also causing increased gate leakage and the threshold voltage shift. Several studies have proposed various mitigation techniques for hot electron degradation, such as using thicker barrier layers, improving the gate insulation, and reducing the electric field. In addition, the on-resistance increase is also temperature-dependent, further limiting the operation of GaN HEMTs at high voltages and temperatures, even if optimization on the structure and, in particular on the buffer layer, can suppress this effect [31], [81], [82].

Temperature is another relevant parameter that is responsible for degradation of GaN HEMTs, especially for high-power applications, where they can operate at high junction temperature for long time. The high temperature reverse bias (HTRB) stress is commonly used to evaluate the reliability of GaN HEMTs for high voltage operations. This condition can lead to permanent degradation of the on-state current and the transconductance and can also cause the threshold voltage shift and the gate leakage current increase [83], [84]. In addition to this permanent degradation, some positive effects have been reported like the decrease of gate leakage current and a decrease of current collapse during pulsed measurement during the HTRB test. The impact of temperature cycling on the reliability of GaN HEMTs was studied in [85], finding that thermal stress caused by repeated temperature changes led to device degradation and failure. The use of GaN HEMTs under extreme temperatures operation has been proved in [86], where a HEMT device with InAlN/GaN lattice matched configuration was fabricated allowing 1-MHz large-signal operation at 1000 °C in vacuum for 25 hours, without evidencing major degradation of the heterostructure.

The external influence of the environment on GaN HEMTs was also studied and particular attention was brought to radiation hardness to evaluate the use of GaN HEMTs in aerospace and military applications [87], [88]. Like all semiconductor devices, GaN HEMTs can be susceptible to damage from ionizing radiation. One of the main effects of radiation on GaN HEMTs is the creation of charge carriers, which can cause changes in device properties and potentially lead to device failure. In addition, radiation can also cause defects in the device structure, which can also impact device performance. Several studies have investigated the radiation hardness of GaN HEMTs, with varying results depending on the type and dosage of the used radiation. The charge carrier density has been identified to be relatively insensitive to gamma rays, that in low doses seem to bring even improvements in device performances, even if high doses of gamma rays can result in severe degradation [89]. Moreover, the impact of heavy-ion irradiation on GaN HEMTs exhibited significant degradation in performance at high radiation doses, but also showed their recovery capability after a long restoring period [90], [91].

1.5 Short Circuit robustness of GaN HEMTs

One of the key aspects in power electronics is the robustness of power devices. In fact, the ability to bear high electro-thermal stress without experiencing catastrophic failures is a crucial point in power converters that must operate without interruption and with high levels of safety and reliability. With the increasing development of power electronics in the perspective of a more sustainable future and energy management, the need of highly reliable conversion systems spread to all the application fields, such as automotive, industry, military, data centers, servers, communication systems and renewables. In this context, the employment of robust and reliable power devices is mandatory [92]-[94].

In particular, the capability to handle Short Circuit (SC) conditions is a core aspect of the robustness of power device. The majority of power converters for the latter application fields is based on Half Bridge (HB) and Full Bridge (FB) configurations, such as 1-phase and 3-phase inverters, resonant DC/DC power converters, DAB and DAB-based topologies and so on. In all the converters based on HB or FB topology there is the risk to cause faults due to the SC of a bridge-leg, leading to the breakdown of the power devices and damages to the whole system. The SC fault can be caused by the power devices degradation, such as thermal runaway, gate rupture or aging, but also by auxiliary circuit malfunctions and poor layout design, that could make the devices susceptible of noise and false turn on.

Some solutions must be led in the design process to prevent and mitigate the SC failure in power converters, possibly without interrupting their operation. This is commonly achieved using fault-detection methods and realizing a protection against the fault event.

The fault-detection is dependent on the converter topology, as different solutions can be provided for inverters and multi-modular DC/DC converters [94]-[96]. The protection, instead, is often realized adding a protection circuit in the gate driver circuit of the power devices, using redundant devices or using auxiliary switches to change the configuration of the bridge and ensure the safe operation of the converter, even if with reduced performances. The hardware redundancy can be performed in different ways: on switch-level, using series or parallel redundant power devices; on leg-level, using redundant bridge legs in the converter; on module-level, in the case of modular converters; on system-level, using redundant series/parallel converters [94], [95].

In order to evaluate the impact of SC on the operation of the device and to design a protection circuit, SC capability tests are performed on the power devices to characterize the electro-thermal stress and the possible boundary conditions that prevent the devices from the catastrophic failure.

As Si MOSFETs and IGBTs have been the leading power devices in medium and high power applications for long years, the research widely focused on their SC robustness, contributing to the improvement of Si-based semiconductor technology, that has reached the highest levels of reliability. On that basis, the recent development of WBG semiconductors as valuable substitutes of Si devices to reach higher performances, efficiency and power density led to an extensive study of the SC behavior on SiC and GaN devices as well [33]-[41], [98]-[105].

Starting from the extensive literature on SC behavior of IGBTs, three types of SC events can be distinguished for a power device [97]:

- Short Circuit type I (SC-I) is the direct turn-on of the device while its V_{DS} is high. In this condition, V_{GS} is initially low with V_{DS} high, like in the normal off-state condition. While V_{DS} is still high, a positive V_{GS} is applied, turning on the device, that operates in its saturation region, causing a high peak drain current. This type of SC is also called Hard Switching Fault (HSF).
- Short Circuit type II (SC-II) is the occurrence of the SC during the on-state of the device. In this case, before the SC event the device is conducting the load current and its V_{DS} assumes the on-state value, close to zero. When the SC occurs, V_{DS} becomes equal to the DC-link voltage and the current suddenly increases with a *di/dt* defined by the DC-link voltage and the parasitic inductance in the circuit. This type of SC is also defined as Fault Under Load

(FUL) and it can be more dangerous for the device, as higher current peak and power dissipation are involved.

- Short Circuit type III (SC-III) occurs when the SC happens on the load path during the switching of the leg, involving the anti-parallel diodes of the devices that are turning on. This condition is quite similar to SC-II, involving a high current peak, but before the SC event the current flows in the diode and the reverse recovery contributes to the increased current peak. For GaN HEMTs, where no body diode and the related reverse recovery is present in the structure, this condition can be assumed to be close to SC-II event.

Many different studies on the Short Circuit (SC) robustness of GaN HEMTs have been performed in recent years. As the most suitable for high power and voltage applications, GaN HEMTs with a breakdown voltage higher than 600 V have been commonly tested. All the experimental SC tests are led focusing on the HSF, where a single device under test (DUT) is characterized in terms of withstand time, energy, time to failure, degradation, instability and failure mechanisms [33]-[41], [105]. In many cases, a device with higher current rating is placed in series to the DUT to protect the circuit in case of failure of the DUT, which could lead to damage to other components on the board.

The robustness of a 650 V – 60 A GaN HEMT under various SC conditions is studied in [34]. In particular, the effects of the DC-link voltage V_{dc}, gate-to-source voltage V_{GS}, temperature and type of SC event are discussed. Two types of SC tests are investigated: a single event SC, with a fixed 10 μs pulse-width, and repetitive SC events, with SC pulse-width increased with 200 ns steps up to the failure of the DUT.

The single event SC tests provides information about the capability of the device. In this type of tests, when $V_{GS} = 6$ V, the recommended driving condition for this device, the DUT showed a good capability for V_{dc} lower than 350 V, surviving all the SC events, both at 25 °C and 125 °C. However, for $V_{dc} \geq 350$ V the DUT fails in less than 700 ns, highlighting a critical aspect of the device. The destruction of the device is attributed to the extreme rise of temperature in a small region of the device, that leads to the melting of the contacts, caused by the high current density. Gate-drain insulation also failed, as V_{GS} overcame its maximum voltage limit. The failure of the device can be avoided for V_{dc} up to 450 V if a reduced gate driving voltage is used, as demonstrated in the work.

The main features of the SC behavior of the DUT are also discussed. In particular, the strong negative temperature feedback of device conductivity, caused by the reduction of the carrier mobility and the channel temperature increase, acts as a self-regulation for the drain current. At the beginning of the SC event, the peak drain current is dependent on V_{GS} and it reaches about 240 A at 6 V. During the SC, the drain current experiences a dramatic reduction, that depends on the dissipated power and, so, on the applied V_{dc}. At

50 V, the final value of the current is about 120 A, while at 300 V it decays to 40 A. The increment of the test temperature is beneficial for the reduction of the current, that is even lower at the end of the SC, because T_j is higher.

Another mechanism found to be relevant for the SC event consists in the gate leakage current increase. In nominal conditions ($V_{GS} = 6$ V, $T_j = 25$ °C), its value is 300 μA, but during the SC event it is increased up to 30 mA, due to the increase of T_j. This phenomenon results in the reduction of V_{GS} applied to the DUT, since a larger voltage drop occurs on the external gate resistor. This fact is considered to be a further beneficial mechanism that helps in reducing the drain current during the SC event.

Then, the authors compute the energy involved during the non-destructive SC tests and define the critical energy that caused the failure of the device. For V_{dc} between 300 V and 400 V the SC energy is between 150 mJ and 220 mJ.

The repetitive SC tests are used to evaluate the degradation of the DUT and the maximum subsequent SC cycles that it can survive. Two scenarios have been investigated: first, repetitive SC event with increasing SC pulse-width at fixed $V_{dc} = 300$ V; second, repetitive tests with fixed SC pulse-width and fixed low voltage $V_{dc} = 20$ V. Both the scenarios led to degradation of the device, observable in the I – V curves, the drain leakage current, the gate leakage current and the threshold voltage. In the first case, the DUT fails after seven pulses and show the reduction of the gate leakage currents and of the threshold voltage, and a slight reduction of drain leakage current for $V_{DS} > 300$ V. In the second condition, the DUT can survive more than 100 SC pulses, but it shows a severe degradation of I – V curves, along with the reduction of drain leakage current and the increase of the threshold voltage.

Some critical aspects of the 650 V – 60 A GaN HEMT are pointed out in this work, as the reduced SC capability for high V_{dc} values that are commonly adopted for the DC-link when using 650 V-devices and the reduced capability to survive repetitive SC tests. The first aspect is critical in comparison to Si and SiC technologies, that show a higher SC robustness, with a withstand time greater than 10 μs at $V_{dc} = 400$ V, while it is less than 700 ns for the DUT. However this issue is not related to the specific tested DUT, as also other families of GaN devices with the same voltage ratings show weak SC robustness at high voltages. For instance, the SC withstand times of different 600- and 650-V power devices are compared in Fig. 1.9. Si and SiC MOSFETs have the highest SC capability, while all devices based on GaN technology show clear worse performances at high voltages in terms of SC robustness. This fact is related to the deep difference in the physical structure of GaN-based transistors, that are lateral devices, and is a limiting factor for the spread of GaN HEMTs in all power electronics applications.

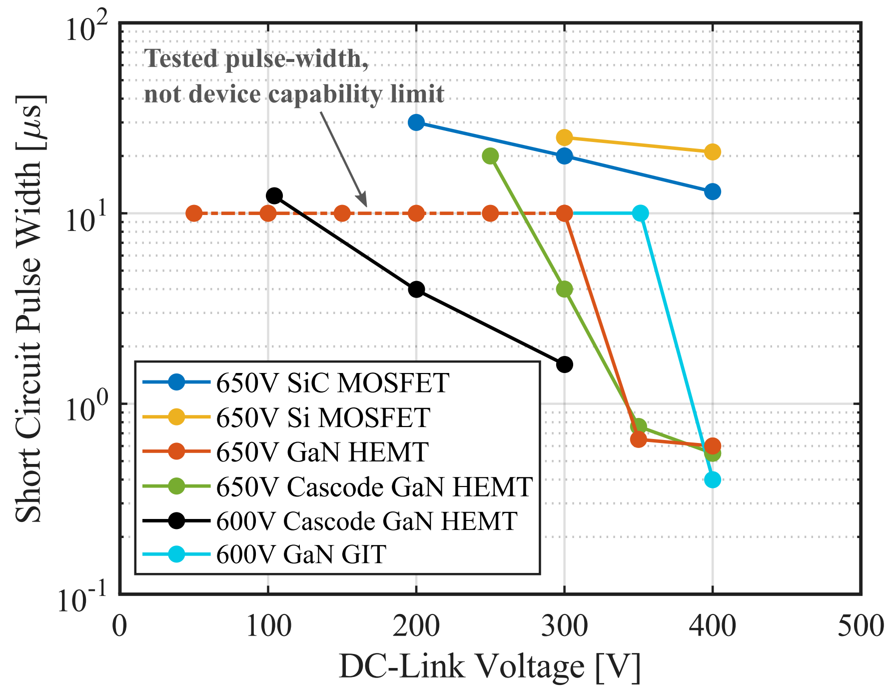


Fig. 1.9 Short Circuit withstand time of different 600/650 V power transistors [34].

The SC capability of others GaN HEMTs are evaluated in the literature. In [33], the DUT is a 650 V – 15 A device, tested both for single and repetitive SC events with an IGBT as a protection on the DC-link. In the test conditions V_{dc} = 400 V, V_{GS} = 6 V the device shows a long SC withstand time, more than 600 μs, at the opposite of the 60 A device. The same explanations are given about the drain current self-regulation mechanism and the long withstand time is attributed to the dramatic drop of the current, that in turns slows down the rise of T_j. For repetitive SC tests, however, the DUT exhibits a withstand time lower than 1 μs in the same conditions and fails at the second pulse.

To evaluate the sensitivity of the DUT to the operating conditions, V_{GS}, V_{dc} and the SC pulse-width t_{SC} were varied. The reduction of t_{SC} from 1 μs to 45 ns leads to a higher withstand time in repetitive tests and the device fails at the 13th SC event. However, the reduction of V_{dc} and V_{GS} has a greater impact on SC behavior than t_{SC}. In fact, with V_{dc} = 200 V no failure of the DUT happens after 4000 cycles with t_{SC} = 1 μs, while the reduction of V_{GS} from 6 V to 3 V implies no failure up to 2000 cycles.

The impact of dynamic V_{GS} on the SC behavior is also evaluated by turning on the DUT before applying the whole V_{dc} across it. The results showed a clear dependence on the time duration between the turn-on of the DUT and the SC event, with a reduction of the peak drain current with the increase of this duration.

Simulation analysis is also provided to investigate the failure mechanism of the DUT, showing the temperature distribution along the device during the SC and highlighting the extreme temperature increase in the gate-drain region. The analysis of the failure spot on a decapsulated failed device is performed through a focus ion beam cutting, showing that the high rise of temperature can lead to the formation of cracks at the interface between the GaN buffer layer and the transition layers, that can be even propagated to the other parts of the device.

Further insights on the failure mechanisms of 650 V GaN HEMTs under SC conditions are provided in [39]-[41], where two types of failures are identified. The first happens for $V_{DS} < 350$ V and with long time to failure, involving a huge amount of energy and high T_j increase. The second failure happens at higher V_{DS} and occurs in less than 1 μs, involving much lower energy.

Destructive SC tests were performed on many 7.5 A GaN HEMTs at 4.5-, 5.0- and 6.0 V gate voltage and 250- and 300 V drain voltage, evaluating the time to failure and the mean power dissipation for each one. To evaluate the impact of T_j on the SC failure, the temperatures of the DUTs immediately before the failure have been estimated using the real thermal impedance of the device for single pulse operation. The computed average temperature for each DUT is 520 °C, which has been used to fit the experimental results of time to failure versus average power dissipation, showing excellent agreement and thus indicating a thermal destruction of the tested DUTs. Moreover, the fitting of the data computing the average SC energy does not accurately represent the failure trend, indicating that the failure temperature is not only dependent on the energy dissipated, but also on the thermal impedance of the device, which varies with the SC duration.

For higher drain voltages, the failure is quite different and involves less energy. In [40] this kind of failure is extensively discussed by performing SC tests with increasing V_{DS} from 320 V to 500 V for different V_{GS} and for a fixed 5 μs SC time. The experimental results on different tested devices show a time to failure always less than 1 μs for each V_{GS}. The post-failure analysis on the DUTs also identifies the region where the failure occurs, corresponding in all the cases to the gate edge on the drain side. The cause of the failure is identified as the extreme high power density reached in this specific device area. This is confirmed by finite element simulations, in which the same experimental conditions are reproduced and a high power density, along with temperature increase, is obtained in the aforementioned region.

The simulation results computed different values for T_j, in the range 885 K – 1026 K, depending on the applied V_{DS}. The unexpected wide T_j variability in simulation is due to the lack of asymmetries in the device structure, that exist and are intrinsic in the real device and lead to current focalization and the reduction of the active area of the device, which

is more prominent at high V_{DS}. The reduction of device active area and the current crowding are taken into account in the simulations correcting the value of V_{GS} with a factor obtained by the experimental results, that showed the reduction of the drain current with increasing V_{DS}. Hence, for this DUT the estimated temperature reached before the failure is about 1100 K (827 °C).

Another widely investigated aspect of SC behavior of GaN HEMTs is the occurrence of oscillations, as it happens in IGBTs, that can produce high EMI in the circuit and increase the chance of failure of the devices. They are experimentally observed in [39], where high frequency oscillations (75 MHz) appear on the DUT's waveforms. Oscillations can appear when the input impedance of the device exhibits a negative real part and its impedance is equal to the output impedance of the driver. The small signal parameters of the GaN HEMTs play a relevant role in determining this behavior.

A comprehensive analysis of SC oscillations in p-GaN HEMTs is provided in [37], where the impact of many circuit and device parameters is studied and an analytical model to explain the occurrence of instabilities is proposed. The results of experimental SC tests on a 650 V – 26 A GaN HEMT show that oscillations can be triggered when a stray inductance is present in the common-source path, with a gate resistance equal to 1 Ω. The entity of the oscillations becomes higher when V_{dc} is increased, while they fully disappear when using a larger gate resistor.

The results of SPICE simulations are used to clarify the positive feedback mechanism leading to self-sustained oscillations on GaN HEMTs. In particular, the occurrence of oscillations is explained by the resonance of the RLC tank that is formed in the circuit because of the stray inductances, capacitances and resistances. In particular, the voltage across the common source inductance acts as an AC voltage source, introducing oscillations on the gate of the DUT, which in turns reflects the oscillations on the drain current. The drain current, flowing in the common-source inductance, closes the positive feedback loop. This behavior is correctly described by deriving an equivalent small-signal model for the DUT, linearized around its working point in SC conditions, which defines the relationship between the gate-source voltage and the input driving voltage.

The impact of all the circuit components is analyzed thanks to this model and, in particular, the effect of increased V_{DS} is shown to bring the device to instability. In addition, a parametric simulation of the damping ratio variation with other circuit parameters is performed, highlighting the boundaries to ensure safe operation with absence of instabilities. Besides reducing the stray inductance on the common-source, which remains the primary cause of SC oscillations, other beneficial solutions in eliminating the oscillations consist in the increase of gate-drain capacitance, that however

affects the switching losses during the normal operation, and the use of a large gate resistance, which nevertheless slows down the switching speed of the device.

From the analyzed results, it can be verified that a 10 Ω resistor, commonly used with GaN HEMTs, is useful to suppress oscillations if the common-source inductance is lower than 1 nH. Anyway, the occurrence of oscillations is strictly linked to the device small-signal model, so different devices can show different behavior and boundary conditions for the instability.

A comparison on the SC behavior of different GaN transistors is provided in [35], where 600 V cascode devices, 600 V p-GaN HEMTs and 650 V metal-insulator-semiconductor HEMTs (MISHEMTs) are evaluated in both non-destructive and destructive SC tests. The cascode devices show the worst SC capability, failing in about 5 μs at V_{dc} lower than 200 V, while the p-GaN HEMT shows the best capability, even if it fails in 400 ns at $V_{dc} = 400$ V. The MISHEMT also experiences a fast failure in about 600 ns at $V_{dc} = 350$ V.

Some insights about the significant differences among different technologies of GaN devices are provided by the authors, that also perform TCAD simulations to describe the main phenomena involved during the SC event. Cascode devices are subjected to a lower decrease of the drain current during the SC with respect p-GaN HEMTs, due to the lower temperature reached in the channel. In this way, the reduction of carrier mobility, which acts as a negative feedback for the reduction of the SC current in p-GaN HEMTs, does not help in reducing the SC stress. In fact, both the peak and the final values of the drain current increase with the applied V_{DS}, leading to the destruction of the cascode device at 200 V. On the contrary, p-GaN HEMTs and MISHEMTs reach high temperatures of the channel, up to 1000 K, experiencing a current drop of about 70% during the SC event and therefore are able to survive at higher V_{DS}.

In all the cases the failure of the GaN devices happens because of thermal destruction and for high V_{DS} it is attributed to the current crowding, as also shown in [40]. Moreover, the increase of temperature along the device structure leads to the increase of the temperature of the gate region, that reach about 600 K for the p-GaN HEMT under test. This fact is responsible of the reduction of the threshold voltage and a consequent increase of the gate leakage current [106], that however is not indicated to have a relevant impact on the drain current reduction, in opposition to other works [34], [36]. Further insights on the drain and gate current behavior of a p-GaN HEMT during the SC are provided in [106], where the temperature dependence of the carrier mobility in the 2DEG is evaluated in detail. P-GaN HEMTs in general show a high gate leakage current dependence with the temperature because of the Schottky junction at the gate and this fact could be exploited for the detection of the SC event.

In resuming the state-of-the-art on SC behavior of GaN HEMTs and focusing on p-doped gate transistors, some key points can be identified:

- The SC capability of medium voltage (600/650 V) GaN HEMTs is lower than Si and SiC MOSFETs and almost no GaN devices survive a 400 V SC with the recommended driving conditions, limiting their applicability in applications requiring high SC ruggedness.
- The main phenomena involved in the SC are temperature-related and consist in drain current reduction and gate leakage current increase.
- The failure mechanisms are related to the high temperature increase in the structure of the device, leading to the destruction of the device in a long time for low V_{DS} and very quickly at high V_{DS}, because of the current crowding.
- The time to failure at high V_{DS} is less than 700 ns and therefore a very fast SC protection needs to be adopted to save the device.
- All the experimental characterizations are focused on the SC type I and are performed on a single DUT.
- Very large values of turn-on gate resistance are often used to perform the SC tests, both to slow down the switching transients and to prevent instabilities. In fact, in [33] the authors use a 38 Ω gate resistor, while a 50 Ω resistor is used in [35] and [106]. In [36] 46-, 100-, 460-Ω values are used. In [34] the value is not provided, but it can be obtained from the experimental data of the gate current and voltage and it is about 60 Ω.
- The impact of the gate leakage current on the SC behavior is not fully clarified. Moreover, it could have a deeper influence when using a large gate resistance, causing a deeper gate voltage reduction during the SC event.
- Accurate analysis is achieved through numerical simulation softwares, but less attention is given to application-oriented simulative tools, like LTSpice, PSpice or Simulink, even because the absence of a simple and accurate model that fully describe the SC behavior of GaN HEMTs.

2
Short Circuit analysis of a GaN-based Half Bridge

As introduced in Chapter 1, the Short Circuit (SC) characterization of GaN HEMTs is often carried out focusing on the single device, performing a SC directly on the DC-link capacitors or with another protection device with much higher current rating. However, the actual test condition does not reflect the real case in practical applications, where the problem of the SC event can occur in converters based on Half Bridge (HB) and Full Bridge (FB) configurations. In fact, the SC can occur because of the unexpected turn-on of one GaN HEMT that may be caused by a driver circuit malfunction, auxiliary power supply failure or false turn-on due to the Miller effect [52], [53].

Even the presence of the protection device placed in series to the GaN HEMT under test is far from the real SC event, because it always works in its linear region and never undergoes an electro-thermal stress. On the contrary, in the practical case the power devices of the bridge are equal and therefore the SC involves two identical devices, whose behavior should be analyzed.

Hence, analyzing the SC operation when two identical GaN devices are used, as in the case of a HB, is substantial to determine the effects of the SC on them and understand their behavior and their electro-thermal stress as well. This chapter deals with this topic, providing a theoretical analysis of the SC event on a GaN-based HB and evaluating some factors that can affect the SC behavior of the two devices.

2.1 Short Circuit operation of the Half Bridge

In order to analyze the SC operation of a GaN-based Half Bridge, the basic circuit scheme of Fig. 2.1 (a) can be considered, where V_s represent a real DC voltage source with its impedance Z_s, C_{DC} is the main DC-link capacitance, C_{dc} is the decoupling capacitance, L_{stray} represents the stray inductance between the main DC-link and C_{dc} and Q_1, Q_2 are two identical GaN HEMTs. In first approximation, all the power loop inductance is considered lumped in L_p.

To create the SC on the HB, the gates of Q_1 and Q_2 are driven by the logic signals shown in Fig. 2.1 (b). According to these driving signals, the operation of the HB can be divided into four phases (*I*, *II*, *III*, *IV*), where the third one is the SC phase and its duration is defined as SC pulse-width T_{SC}.

The configurations of the HB during the four different phases are shown in Fig. 2.2 neglecting the voltage source and considering a fixed V_{dc} value on the capacitor C_{dc}. The operating points on the drain I – V characteristics of the two GaN HEMTs are also highlighted for each phase in Fig. 2.3.

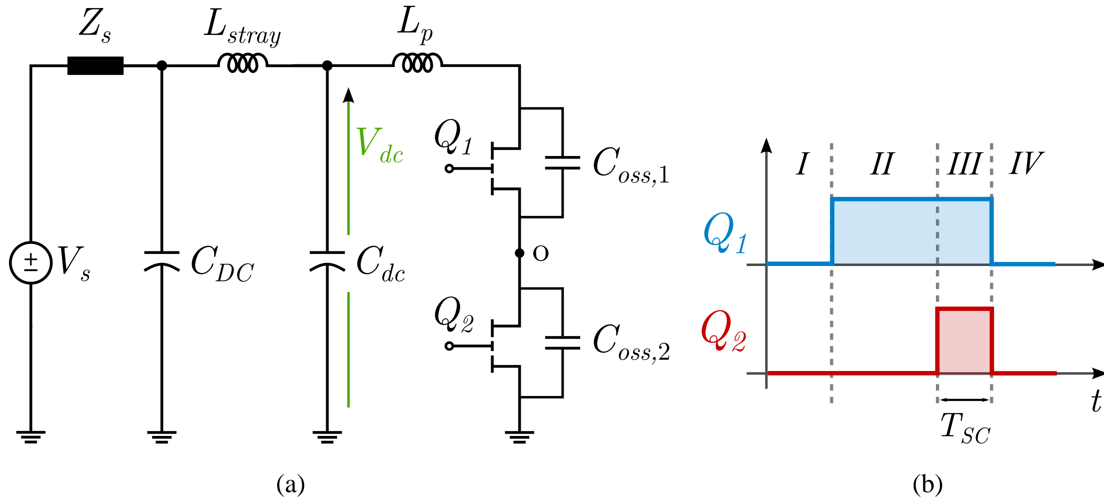


Fig. 2.1 Basic circuit scheme of the Half Bridge with GaN HEMTs (a) and driving signals (b) for the study of the SC behavior.

The operations can be described as follows:

I. During phase *I* the GaN HEMTs are in off-state and are blocking the DC-link voltage V_{dc} across them. The node O is floating and, ideally, each device blocks half V_{dc} assuming the same leakage characteristic, so their output capacitances $C_{oss,1}$, $C_{oss,2}$ are charged, as shown in Fig. 2.2 (a).

II. In phase *II* the high side device Q_1 is turned-on and its drain-to-source voltage $V_{DS,1}$ goes to zero, applying the whole DC-link voltage V_{dc} to the low side device Q_2 (Fig. 2.2 (b)). At the steady state, no current flows in the bridge.

III. In phase *III* Q_2 is also turned on while Q_1 is on and the HB operates in SC conditions for the time period T_{SC}. The SC current I_{SC} is determined by the operating point on the output characteristic of device Q_2, visible in Fig. 2.3. Q_2 works in the saturation region and behaves like a controlled current source while it is still blocking almost all the DC-link voltage V_{dc}. Ideally, considering the same gate voltages and junction temperatures and neglecting any other effect, at the beginning of the SC Q_1 and Q_2 work on the same output characteristic and the operating point of Q_1 is determined by the value of the drain current set by Q_2 according to the Kirchhoff's circuit equations:

$$\begin{cases} I_{D,1} = I_{D,2} = I_{SC} \\ V_{dc} = V_{DS,1} + V_{DS,2} + L_p \dfrac{dI_{SC}}{dt} \end{cases} \tag{2.1}$$

The presence of the parasitic inductance L_p causes a transient reduction of $V_{DS,2}$ and as a consequence, $V_{DS,1}$ can experience an increase. The operating point of Q_1, assuming that its gate voltage is always higher and its temperature is always lower than the ones of Q_2, is located in the linear region of its output characteristic, as it will be further explained later. Therefore it behaves like a current-controlled resistance defined by its $r_{DS,on}$, as graphically shown in Fig. 2.3.

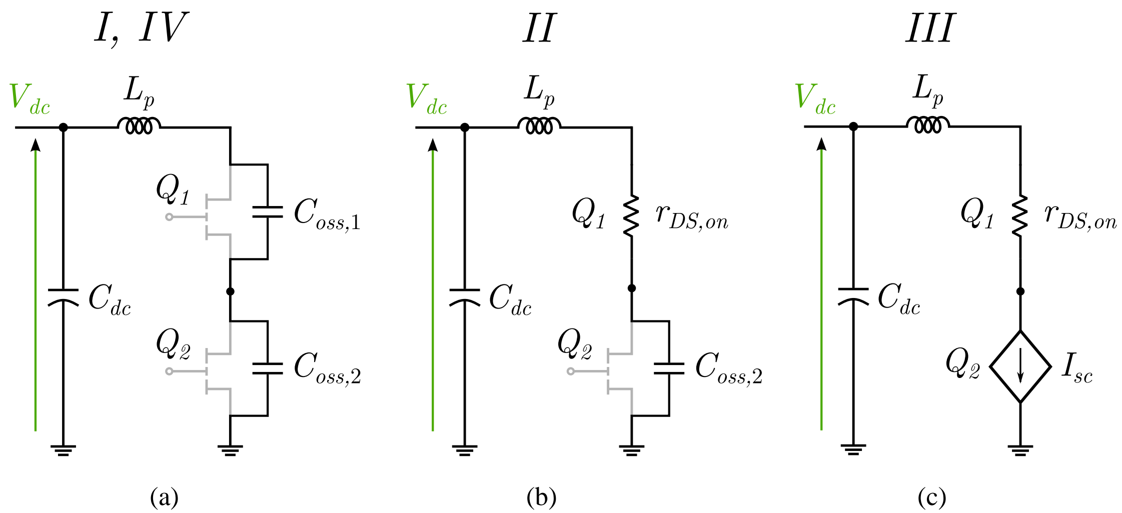


Fig. 2.2 Circuit configurations during the different phases of the SC operation, defined according to the driving signals of Fig. 2.1: (a) phases I and IV, (b) phase II, (c) phase III.

During this phase the power dissipation of device Q_1 is $P_{d,1} = r_{DS,on}I_{SC}^2$ and, since $r_{DS,on}$ is low, it is not critical for the device. On the contrary, device Q_2 is in the saturation region and its power dissipation can be approximated as $P_{d,2} \approx V_{dc}I_{SC}$. The high instantaneous power dissipation on device Q_2 causes a sudden increase of its junction temperature $T_{j,2}$ and the downshifting of the I – V characteristic towards lower values of current. On the contrary, as the SC current decreases, the operating point of Q_1 moves on the same initial characteristic towards lower values of $r_{DS,on}$, causing the reduction of $V_{DS,1}$ and the increase of $V_{DS,2}$. This is qualitatively represented in the output characteristic of Fig. 2.3 in phase *III*, where $T_{j,1} < T_{j,2} < T_{j,3} < T_{j,4}$.

IV. In phase *IV* the two devices are turned-off and they block again the DC-link voltage V_{dc} (Fig. 2.2 (a)). However, because at the end of phase *III* they were subjected to different voltages, their output capacitances assume different values because of the $C_{oss} - V_{DS}$ characteristic. This implies that $C_{oss,1}$ assumes a higher value than $C_{oss,2}$, as Q_1 was blocking the lowest voltage. So Q_2, because of the lowest output capacitance, will block a higher percentage of the DC-link voltage, as shown in Fig. 2.3 (phase *IV*).

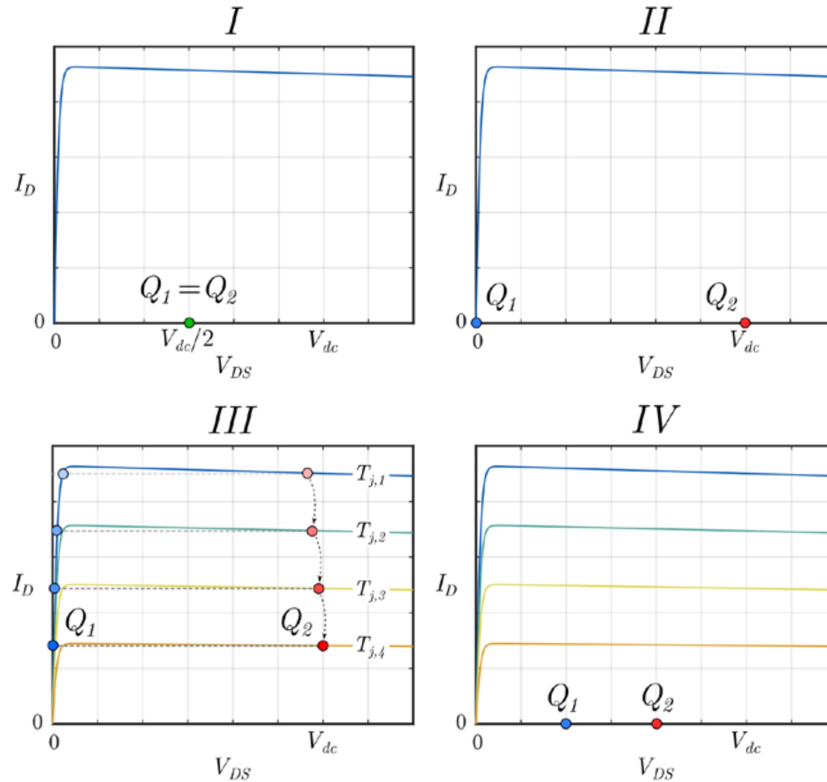


Fig. 2.3 Operating points of the two GaN HEMTs on the Drain I – V characteristic for the different phases during the SC operation. Blue dots refer to device Q_1, while red ones to device Q_2.

Hence, during the SC event the behavior of the two devices is not the same and the electro-thermal stresses are also different. In this condition, Q_2 can be considered the device which leads the SC current, since it works in the saturation region, and Q_1 "follows" the current by varying its V_{DS} drop acting as a variable resistor. For the latter discussion, the equivalent scheme of the HB during the SC event can be defined as the one shown in Fig. 2.2 (c), with a controlled current source and the on-resistance of the other device.

In first analysis, all the SC stress is borne by the device that turns-on after its blocking phase: in fact, the same reasoning could be conducted swapping the driving signals of the two devices, turning-on Q_2 first and Q_1 afterwards. In this case, the roles of the switches would be inverted and Q_1 would operate in the saturation region and bear all the SC stress.

However, for the real case a further discussion on the possible behavior of the two GaN HEMTs is needed to understand if it is possible that the two devices exchange their operating points depending on some circuit and test conditions. In practice, for the latter analysis, if device Q_2 turns-on after the blocking phase, the SC stress should be borne especially by Q_2 and not Q_1. The question is if it is possible, under some conditions, that device Q_1 becomes the most stressed device even if Q_2 turns on after the blocking phase. To answer this question many simulations have been performed and the results will be discussed in the next section.

2.2 Simulation analysis

A simulation study has been led to verify the theoretical analysis performed in section 2.1 using LTSpice, which has the possibility to incorporate the manufacturer model of the GaN HEMTs. The level-3 model of the 650 V – 60 A GaN HEMT has been used to perform the simulation analysis. It incorporates the parasitic inductances of the real device and its thermal model and it has been already presented in section 1.4.5. The circuit scheme used for the simulation study is shown in Fig. 2.4, where also the distributed parasitic inductances at drain, source and gate contacts that can exist in the real circuit have been placed. R_{g1} and R_{g2} are the gate resistors, while V_{G1} and V_{G2} are the gate driving signals for Q_1 and Q_2, respectively. R_p represents the parasitic resistance of the power loop. The values of the parameters used in the simulation are listed in Table 2.1.

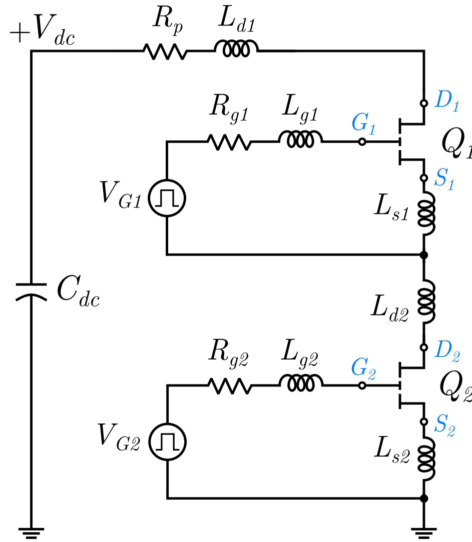


Fig. 2.4 Circuit implemented in the LTSpice simulation for the SC analysis.

Different parametric simulations have been performed to evaluate the effects of such parameters on the SC of the GaN-based HB and they will be discussed separately in the following. The driving signals used in all the simulations are those of Fig. 2.1 (b) and the SC pulse-width has been fixed to $T_{SC} = 5$ µs.

Table 2.1 Parameters used in the LTSpice simulations.

LTSpice Simulation Parameters		
Symbol	***Value***	***Unit***
Q_1, Q_2	GS66516T	-
C_{dc}	80	µF
V_{G1}, V_{G2}	4, 5, 6	V
R_{g1}, R_{g2}	10, 100	Ω
L_{g1}, L_{g2}	1.0	nH
L_{d1}	3.0	nH
L_{d2}	2.0	nH
L_{s1}, L_{s2}	0.5	nH
R_p	10	mΩ

2.2.1 Effect of DC-link voltage

The impact of the DC-link voltage on the SC behavior is evaluated by varying V_{dc} from 50 V to 450 V in 50 V steps. The gate driving voltages V_{G1} and V_{G2} are fixed to 5 V and the gate resistances R_{g1} and R_{g2} are set to 10 Ω. The results of the simulation are shown in Fig. 2.5, Fig. 2.6 and Fig. 2.7, where the plotted waveforms are the SC current, the gate-

to-source voltage, the gate current, the drain-to-source voltage and the junction temperature of each device.

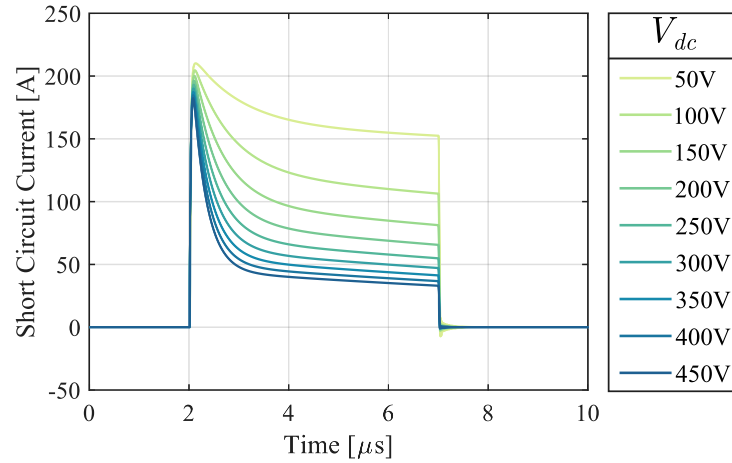


Fig. 2.5 Simulated Short Circuit current for a V_{dc} variation from 50 V to 450 V

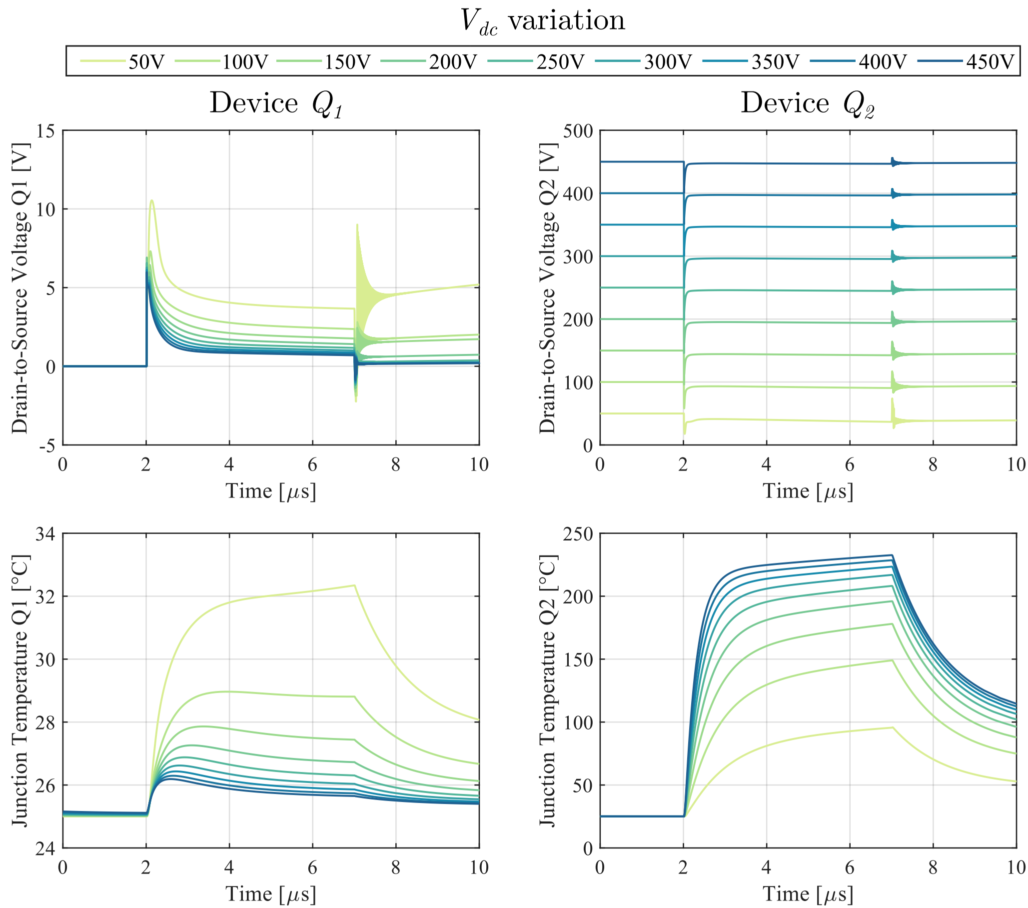


Fig. 2.6 Simulated V_{DS} and T_j of each GaN device for a V_{dc} variation from 50 V to 450 V.

At the beginning of the SC event at $t = 2$ μs, the SC current rapidly increases in about 150 ns and shows a peak value of about 210 A that depends on V_{GS} and the initial T_j. The peak value reduces as V_{DS} increases, as also shown in the simulation, because of a higher and faster increment of T_j, caused by a higher power dissipation. The high *di/dt* is responsible for a transient reduction in device Q_2 drain-to-source voltage, due to the presence of parasitic inductances in the power loop, while V_{DS} of device Q_1 undergoes an increase of few volts starting from 0 V.

Because of the high instantaneous power dissipation of Q_2, its junction temperature increases. The increment of T_j is proportional to the input V_{dc} and it reaches more than 200 °C for V_{dc} higher than 200 V. On the contrary, device Q_1, being subjected to lower V_{DS}, suffers from a lower increase of T_j, that is maximum at low V_{dc}. As V_{dc} increases, the operating point of Q_1 goes deeper in its linear region and its V_{DS} decreases. Therefore, the power dissipation of Q_1 is linked to the on-resistance and is much smaller than in device Q_2, leading to much lower temperature.

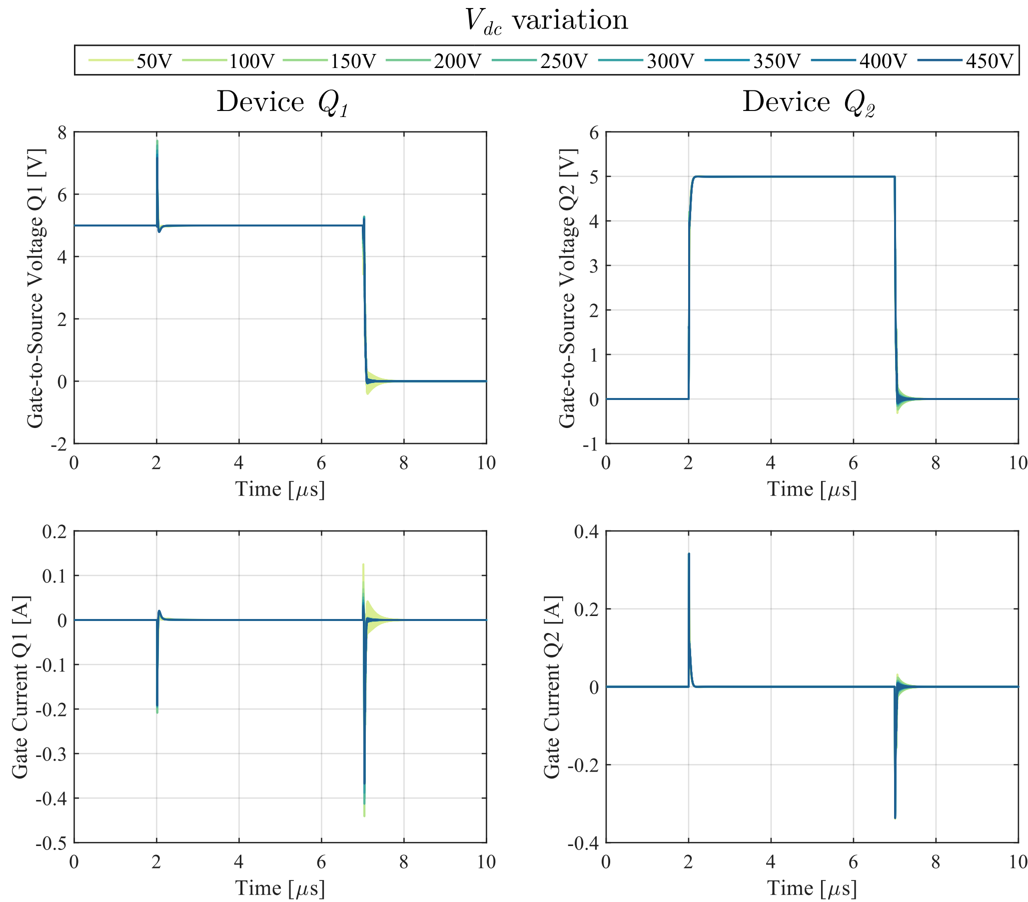


Fig. 2.7 Simulated V_{GS} and I_G of each GaN device for a V_{dc} variation from 50 V to 450 V.

After the initial phase, I_{SC} experiences a significant drop to lower values of current because of the massive increase of Q_2 junction temperature. At the end of the SC, the current is respectively 30% and 80% lower than its peak value at $V_{dc} = 50$ V and $V_{dc} = 400$ V. Moreover, the major drop of the current happens in less than 2 μs since the beginning of the SC for $V_{dc} = 400$ V.

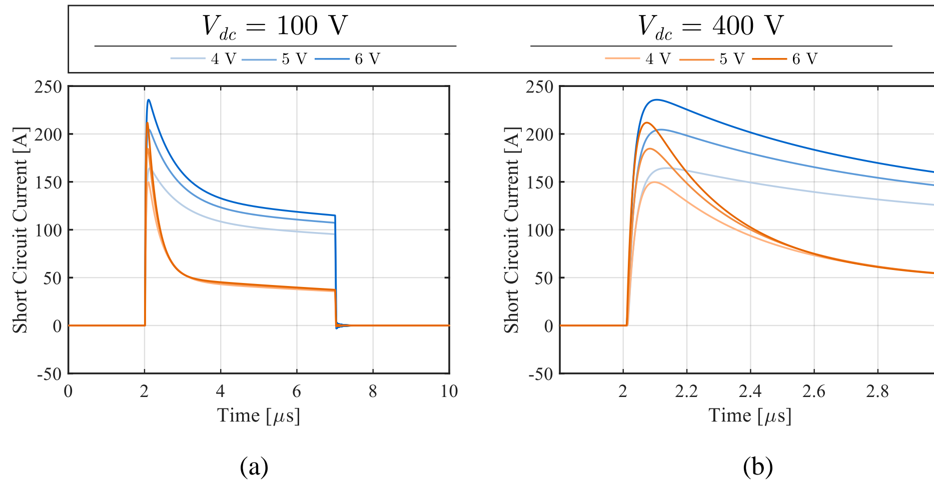
Considering the gate, Fig. 2.7 shows the gate voltage and current (V_{GS} and I_G) of the two devices. The turn-on transition of Q_1 is not shown since it has poor information, considering that no current flows in the GaN devices and all V_{dc} is applied to Q_2. When Q_2 turns on, the high *di/dt* of the SC current is responsible for the transient voltage and current variation on the gate of Q_1. After that, no noticeable changes in the gate waveforms are visible until the devices are turned off. However, it is known that the junction temperature has a crucial impact on gate current, so a considerable increment of I_G in device Q_2 would be expected as V_{dc}, and so T_j, increases. This relationship, which is experimentally confirmed in many works [107]-[111], is not represented in the manufacturer model of the GaN HEMT, but it needs to be evaluated because it directly affects the SC behavior of the device. In fact, as introduced in chapter 1, in many works the self-regulation mechanism of the SC current is attributed to the simultaneous effect of junction temperature and gate current increase.

2.2.2 Effect of gate voltage

The SC current is set by the device that operates in the saturation region and therefore it is strongly dependent on V_{GS} and T_j. To evaluate the impact of V_{GS} on the SC of the HB, a simulation is performed with different gate driver voltages for both the GaN HEMTs: 4 V, 5 V and 6 V. To take into account also the effect of the DC-link voltage, two values of V_{dc} are used, namely 100 V and 400 V. All the other parameters are set according to Table 2.1. The results of the simulation are shown in Fig. 2.8, Fig. 2.9 and Fig. 2.10.

Looking at Fig. 2.8, it is clear how the value of V_{GS} defines the peak SC current, that is 160 A and 240 A at $V_{GS} = 4$ V and $V_{GS} = 6$ V, respectively, when V_{dc} is equal to 100 V. As V_{dc} increases, the peak SC current is limited by the concurrent increment of T_j of device Q_2, that increases faster because of the higher power dissipation. It is interesting to note that for $V_{dc} = 400$ V, after the initial peak, the SC current reduces to the same values, indicating that the impact of T_j is preponderant than V_{GS} when high temperatures are reached during the SC.

The other waveforms are not significantly interested by the change of the driving voltage. The gate current is not reported in the plots as it does not effectively represent the



(a) (b)

Fig. 2.8 Simulated Short Circuit current for V_{GS} equal to 4 V, 5 V and 6 V and V_{dc} equal to 100 V and 400 V (a) and detail of the beginning of the SC event (b).

real gate current of the GaN HEMTs during the SC, for the reason explained in the above section.

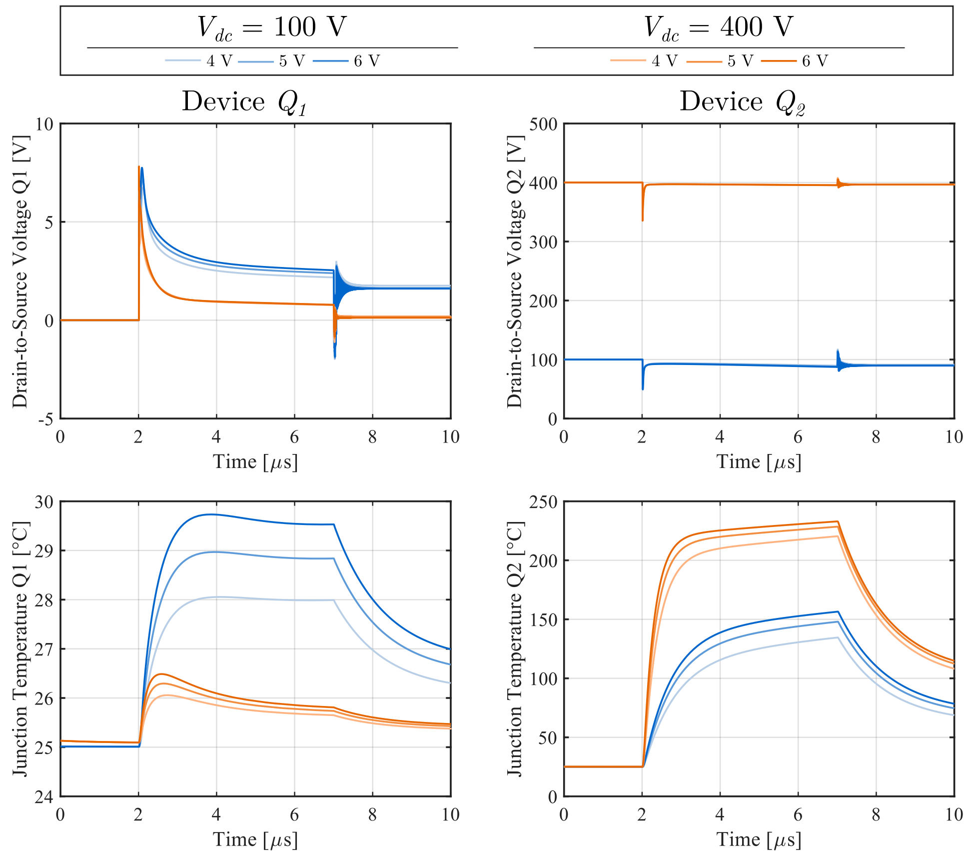


Fig. 2.9 Simulated V_{DS} and T_j of each GaN device for V_{GS} equal to 4 V, 5 V and 6 V and V_{dc} equal to 100 V and 400 V.

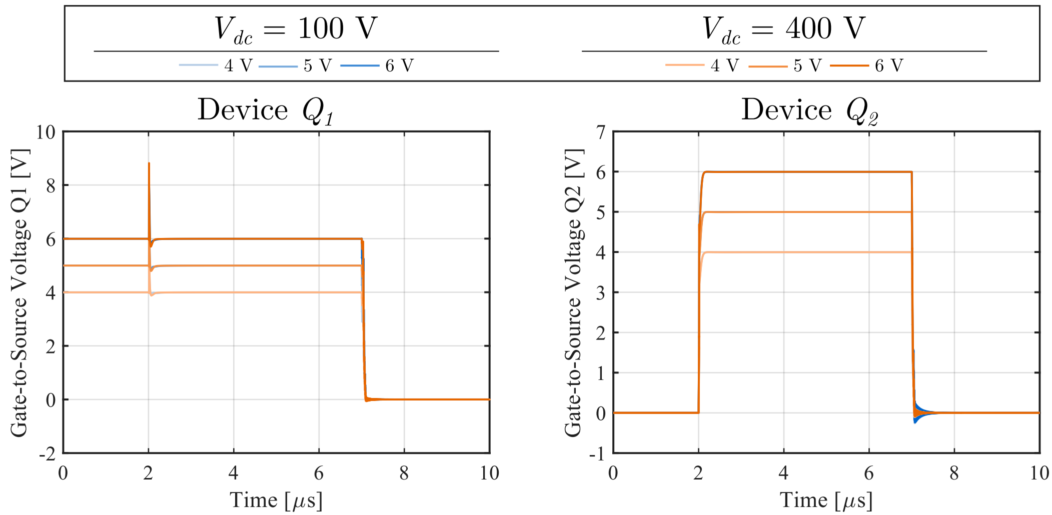


Fig. 2.10 Simulated V_{GS} of each GaN device for V_{GS} equal to 4 V, 5 V and 6 V and V_{dc} equal to 100 V and 400 V.

2.2.3 Effect of gate resistance

The influence of the gate resistance R_g on the SC behavior of the GaN-based HB is investigated in this paragraph. Two values of R_{g1} and R_{g2} have been used, 10 Ω and 100 Ω. V_{dc} was also varied from 100 V to 400 V in 100 V steps to better evaluate the impact of gate resistance on the SC waveforms and clearly visualize the results. The waveforms of the two GaN HEMTs are plotted in Fig. 2.11, Fig. 2.12 and Fig. 2.13, where

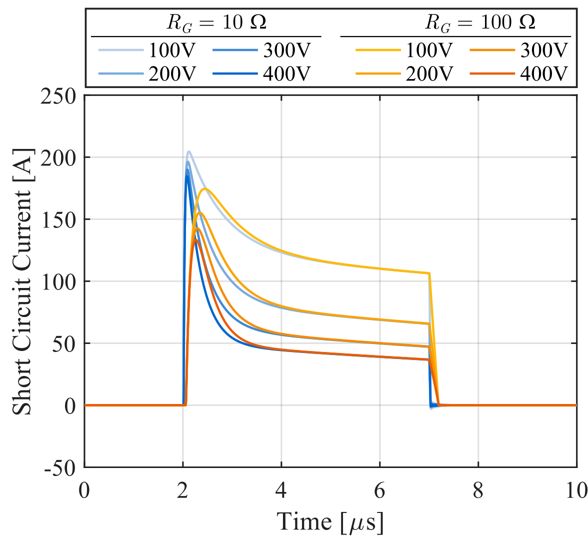


Fig. 2.11 Simulated Short Circuit current for $R_g = 10\ \Omega$ and $R_g = 100\ \Omega$, with a V_{dc} variation from 100 V to 400 V.

the blue and orange lines correspond to the conditions $R_g = 10\,\Omega$ and $R_g = 100\,\Omega$, respectively. The gate current of the two devices is not reported since it does not represent their real behavior, because of the manufacturer model.

The main consequence of increasing the gate resistance is slowing down the turn-on and turn-off transients, as can be seen from the gate voltage in Fig. 2.13. This, of course, reduces the *di/dt* of the SC current and minimizes the effects of parasitic inductances on the power loop, damping the oscillation on the drain voltages. Another effect consists in the reduction of the peak SC current, visible in Fig. 2.11. Considering the condition $V_{dc} =$ 100 V, the peak current is about 200 A for $R_g = 10\,\Omega$ and it reduces of the 15% to 170 A for $R_g = 100\,\Omega$, while when $V_{dc} = 400$ V, it goes from 180 A to 130 A.

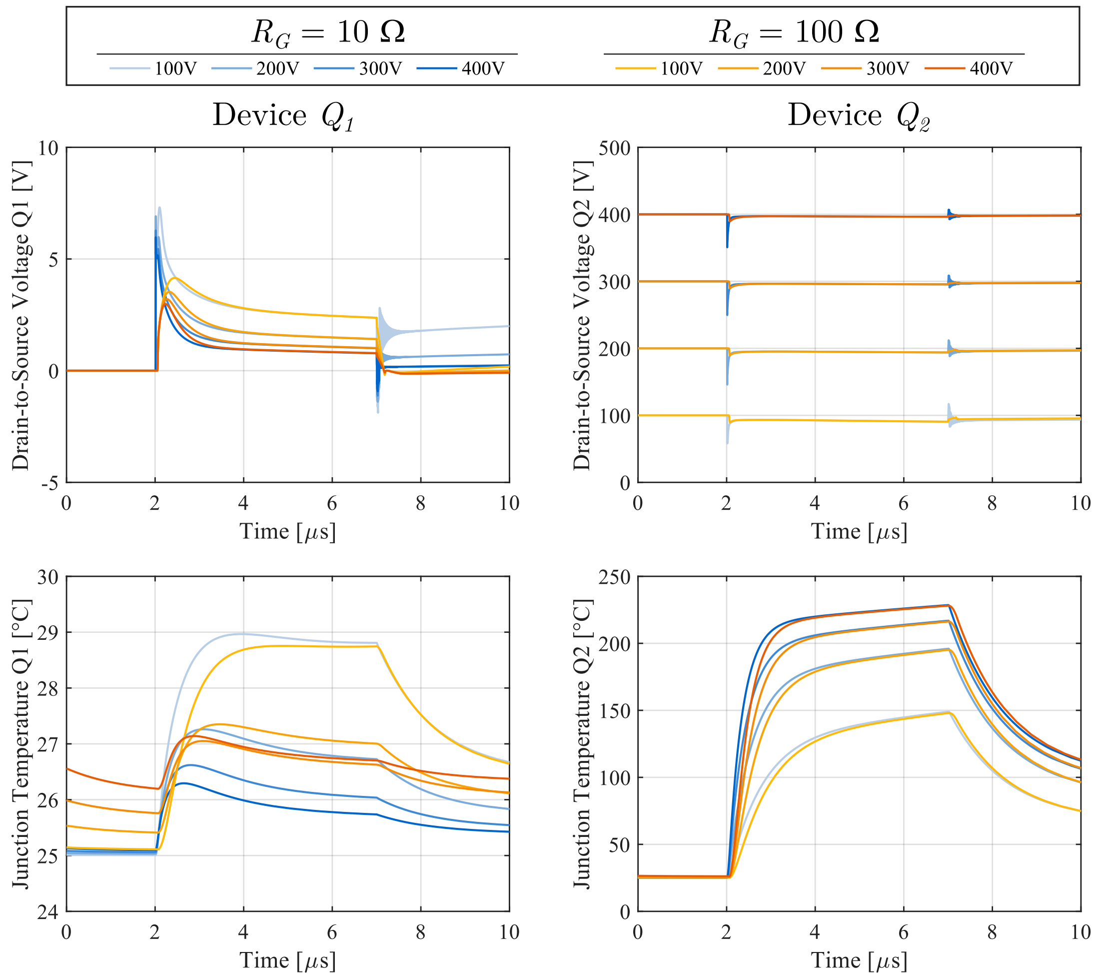


Fig. 2.12 Simulated V_{DS} and T_j of each GaN device for $R_g = 10\,\Omega$ and $R_g = 100\,\Omega$, with a V_{dc} variation from 100 V to 400 V.

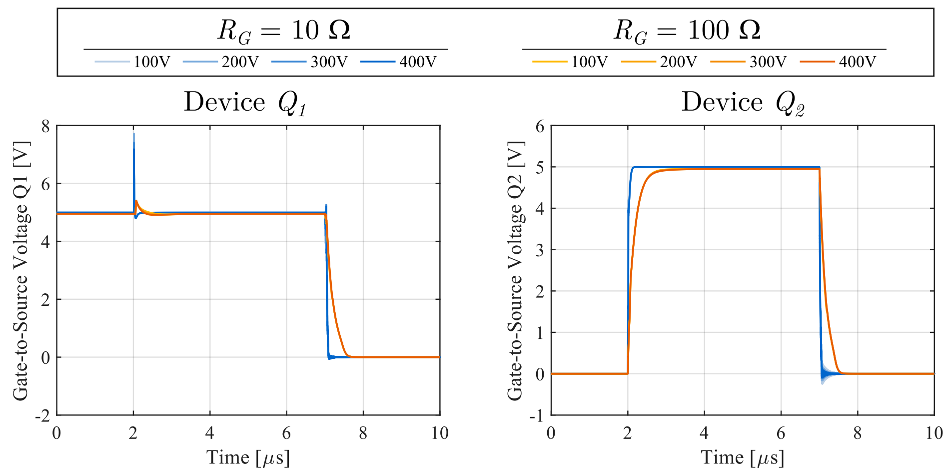


Fig. 2.13 Simulated V_{GS} of each GaN device for $R_g = 10\ \Omega$ and $R_g = 100\ \Omega$, with a V_{dc} variation from 100 V to 400 V.

This can be explained considering Fig. 2.14, where a detail of the SC current and the junction temperature of device Q_2 is shown at the beginning of the SC event. Focusing on the condition $V_{dc} = 400$ V, when using a 10 Ω resistance the current reaches its peak in few nanoseconds at $t = 2.08$ µs, while T_j starts to increase with the time constant related to the thermal impedance of the GaN HEMT and its value is 50 °C when I_{SC} reaches the peak. With the 100 Ω resistance I_{SC} takes more time to reach its peak, that occurs at $t = 2.26$ µs. During this period T_j starts to increase and reaches 80 °C when I_{SC} is the maximum. With higher R_g the *di/dt* of the SC current is slowed down, but during its growth there is already a considerable power dissipation that makes T_j increase. So, the self-heating impacts the drain current more quickly and its maximum value is lower.

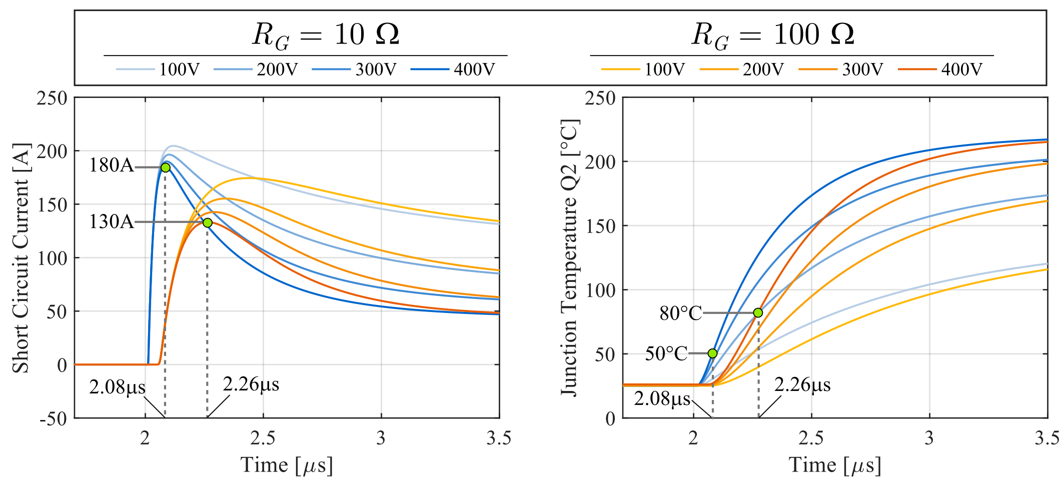


Fig. 2.14 Detail of SC current and T_j of device Q_2 for $R_g = 10\ \Omega$ and $R_g = 100\ \Omega$, with a V_{dc} variation from 100 V to 400 V.

Finally, after the initial phase the SC current tends to the same value both with 10 Ω and 100 Ω gate resistance, because also T_j reaches the same value, as visible in Fig. 2.11 and Fig. 2.12.

The use of a large gate resistance seems to be beneficial for the SC, but it has little practical use in normal operating conditions because it degrades the switching performances of the device. Anyway, a large gate resistor could be used in a protection circuit to smooth the turn-off of the devices after a SC event and to prevent oscillations on the gate and the drain.

2.2.4 Effect of parasitic inductances

Among the parasitic inductances that can appear in the circuit because of the layout of the board, the common-source inductance has been identified as the most impacting on the power devices. In the presence of a large common-source inductance, instability and oscillations can appear during the SC event leading to the destruction of the devices, as well described in [37], [38].

Instead, the stray inductance on the drain of the power devices can cause a deeper voltage dip at the beginning of the SC and the arise of ringing at the turn-off, with consequent overvoltage on the drain and undamped oscillations. However, apart from that, the stray inductance on the drain side does not significantly affect the SC behavior of the two GaN HEMTs, as can be seen from Fig. 2.15, that compares the SC current and the drain-source voltages of the two devices in the condition $V_{dc} = 300$ V, $R_g = 10\,\Omega$, respectively with 3 nH (blue lines) and 10 nH (orange lines) of stray inductance on the drain of each device. The leg stray inductance in a well-designed PCB is commonly in the order of 2 – 3 nH, so the presence of a 10 nH stray inductance, though possible, is a very deteriorating case.

The SC current doesn't show any noticeable difference in the two cases, while it is clear the effect on the drain-source voltages. In fact, $V_{DS,2}$ has a deeper voltage dip at the beginning of the SC, going from 257 V to 150 V with 3 nH and 10 nH, respectively, while both $V_{DS,1}$ and $V_{DS,2}$ experience low-damped oscillations at the turn-off. The overvoltage on Q_2 moves from 306 V to about 340 V with 3 nH and 10 nH, respectively.

Another simulation analysis has been performed to study the impact of common-source inductance on the SC behavior of the GaN-HB, in the same previous conditions, i.e. $V_{dc} = 300$ V and $R_g = 10\,\Omega$, with $L_{d1} = L_{d2} = 3$ nH. The common-source inductance, assuming symmetrical layout and identical devices, was set to 0.5 nH, 1 nH and 2 nH for each HEMT, with $L_{cs} = L_{s1} = L_{s2}$.

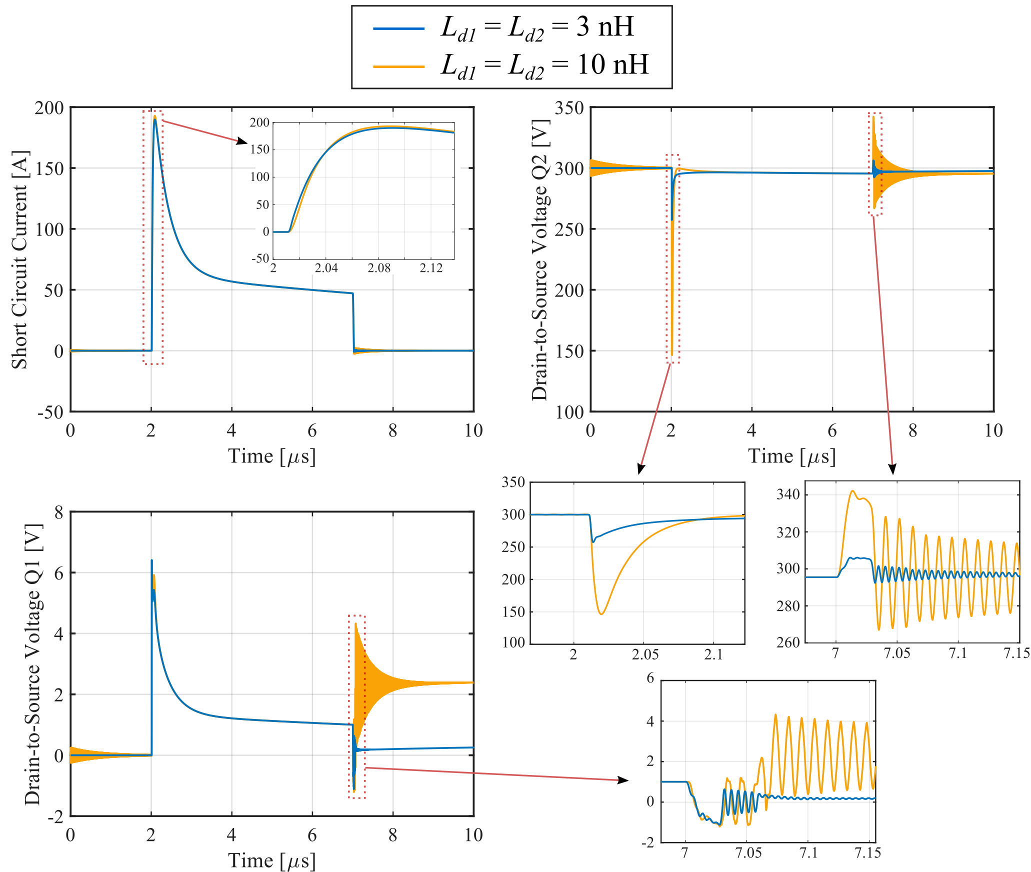


Fig. 2.15 SC current and drain-source voltages of devices Q_1 and Q_2 with related zooms for two values of stray inductance on the drains, namely 3 nH and 10 nH, in the conditions $V_{dc} = 300$ V, $R_g = 10\ \Omega$.

The waveforms obtained from the simulation are shown in Fig. 2.16, Fig. 2.17 and Fig. 2.18. As a major effect, the increase of L_{cs} reduces the *di/dt* of the SC current and also its peak value from 180 A to 170 A with 0.5 nH and 1.0 nH respectively, because of the T_j increase during the growth of the current. For $L_{cs} = 2$ nH, oscillations are triggered, involving gate and drain currents and voltages of the two devices. A detail of the SC current is shown in Fig. 2.16 (b) to highlight the oscillations that appear for $L_{cs} = 2$ nH, which have a frequency f_0 of about 200 MHz. Then, at about 4 µs, the oscillations disappear. The presence of oscillations during the SC event on a p-GaN HEMT can be explained considering the positive feedback mechanism played by L_{cs}. However, it is worth noting that the oscillations in this condition look different from the ones showed in [37] and that they were already triggered before the SC event, that begins at 2 µs. This means that the presence of large L_{cs}, independently from the SC condition, forming an RLC resonant tank in the gate loop can be responsible for the occurrence of instability in the circuit.

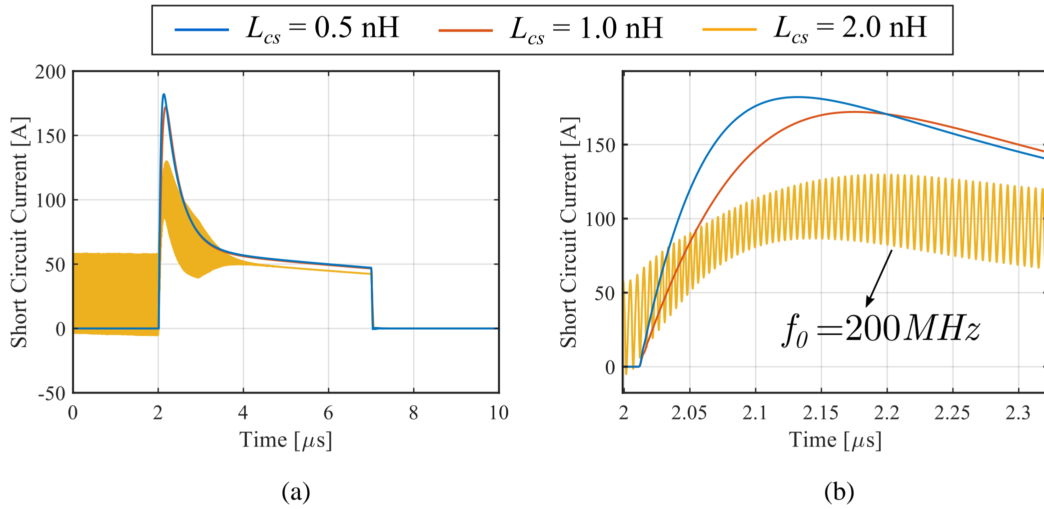


Fig. 2.16 Simulated Short Circuit current for three different values of L_{cs}, namely 0.5 nH, 1.0 nH and 2.0 nH, in the conditions V_{dc} = 300 V, R_g = 10 Ω, (a) full evolution of the current, (b) detail of the SC current at the beginning of the SC.

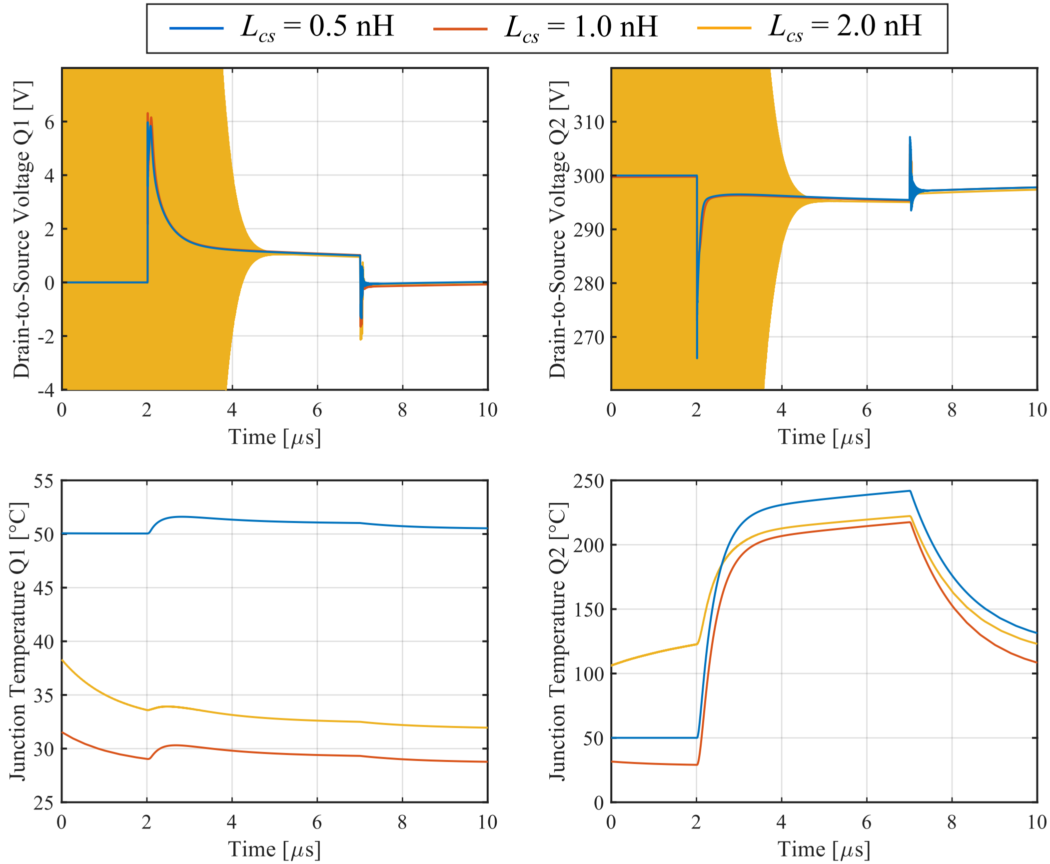
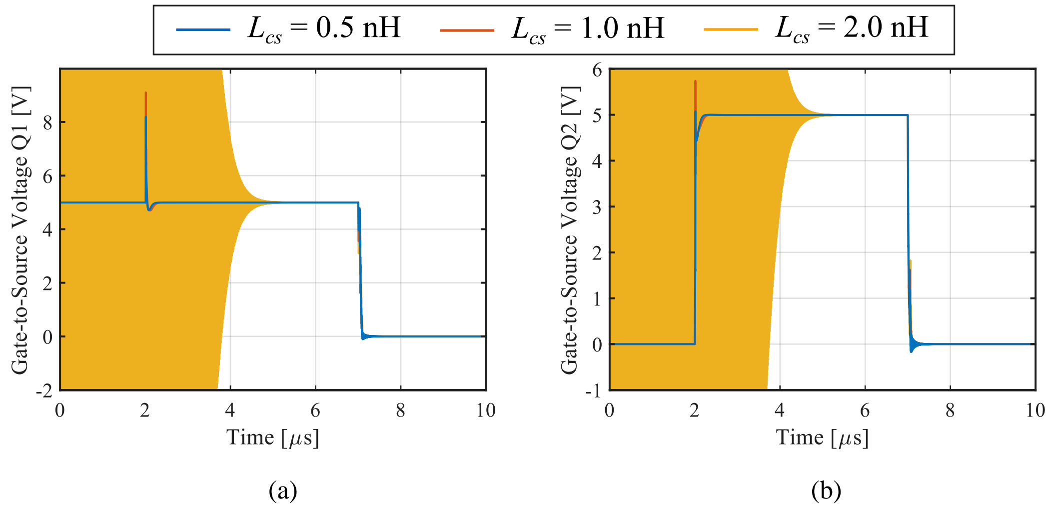


Fig. 2.17 Simulated V_{DS} and T_j of each GaN device for three different values of L_{cs}, namely 0.5 nH, 1.0 nH and 2.0 nH, in the conditions V_{dc} = 300 V, R_g = 10 Ω.



(a) (b)

Fig. 2.18 Simulated V_{GS} of the two GaN HEMTs for three different values of L_{cs}, namely 0.5 nH, 1.0 nH and 2.0 nH, in the conditions $V_{dc} = 300$ V, $R_g = 10$ Ω.

The presence of oscillations also before the SC event cause a higher power dissipation of both GaN HEMTs, increasing their junction temperatures, as shown in Fig. 2.17.

As the oscillations are caused by the RLC resonant tank in the gate loop, they can be effectively damped increasing slightly the gate resistor. As an evidence, the SC current is plotted in Fig. 2.19 (a) in a longer time scale, in the conditions $V_{dc} = 300$ V, $L_{cs} = 2$ nH and for two values of R_g, namely 10 Ω and 20 Ω. When using a 20 Ω gate resistance the oscillations are completely damped. Eliminating the oscillations also reduces the power dissipation of the device before the SC, as confirmed by the junction temperature of Q_2, plotted in Fig. 2.19 (b), that stays constant to 25 °C until the SC occurs.

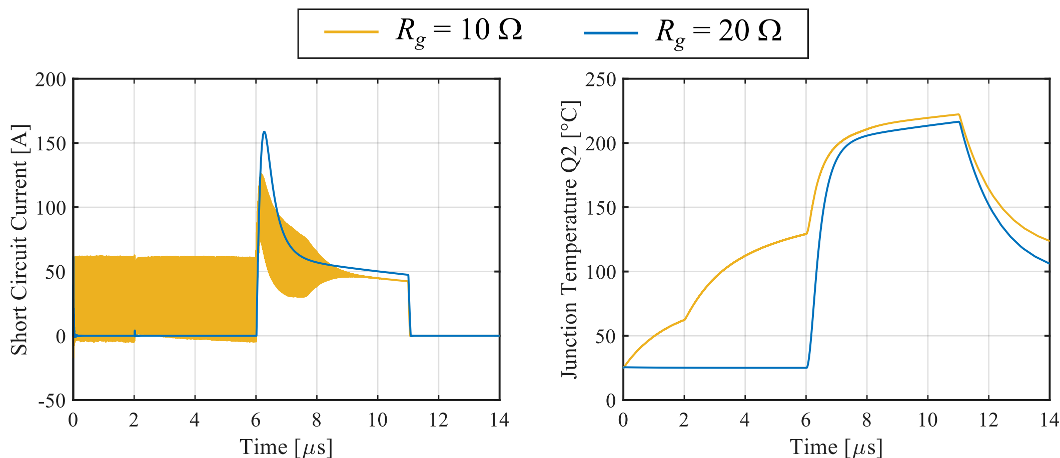


Fig. 2.19 SC current (a) and junction temperature (b) of device Q_2 for $R_g = 10$ Ω and $R_g = 20$ Ω in the conditions $V_{dc} = 300$ V, $L_{cs} = 2$ nH. The oscillations are effectively damped with larger R_g.

2.2.5 Effect of mismatch

It is possible that two identical devices show some differences in their behavior, both because of minimal differences or defects in the internal structure and differences in the layout of the board where they are used. Neglecting the first aspect, differences in the circuit connections of the two devices can lead to the arise of different parasitic effects in the circuit. For example, different lengths of the gate loop result in a mismatch between the parasitic inductance on the path for the two devices. The same happens if the tracks that connect the power loop have different lengths, distributing different amount of parasitic inductance along the path.

A simulation analysis has been performed to evaluate the impact of such mismatch on the SC behavior of the two GaN HEMTs in the HB. The parasitic inductances on the gate and power path of the two HEMTs were varied. After analyzing the simulation results, no unexpected behaviors have been observed varying the parasitic inductances L_g, on the gate, and L_d, on the drain. However, significant changes in the behavior of the two devices have been noticed when the mismatch involves the common-source inductance.

To show the effects of common-source inductance mismatch, the simulation was carried out according to the circuit of Fig. 2.4, where L_{d1} and L_{d2} were set to 3 nH and L_{g1} and L_{g2} to 1 nH. The common-source inductance L_{s2} on the low side device was set to 0.4 nH, while L_{s1} on the high side device was set to 1.0 nH. The simulation results are shown in Fig. 2.20, Fig. 2.21 and Fig. 2.22, in the conditions $V_{G1} = V_{G2} = 5$ V, $R_{g1} = R_{g2} = 10\ \Omega$ and for a V_{dc} variation from 100 V to 400 V in 100 V steps.

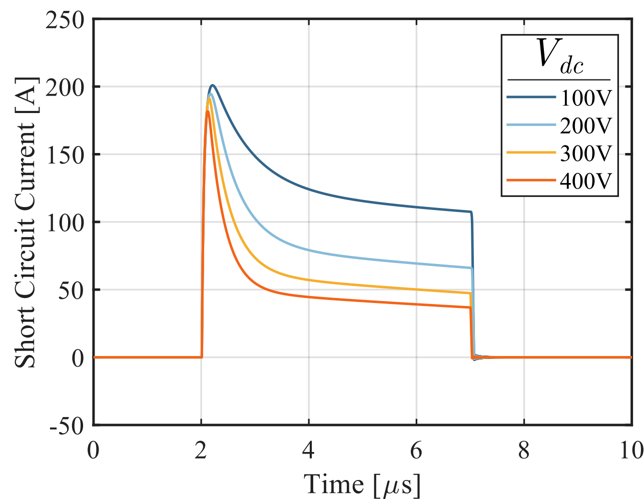


Fig. 2.20 Simulated Short Circuit current in the presence of mismatch in common-source inductances of the two GaN HEMTs, with $L_{s1} = 1.0$ nH, $L_{s2} = 0.4$ nH and a V_{dc} variation from 100 V to 400 V.

The SC current, visible in Fig. 2.20, does not show changes in comparison to the perfect symmetrical circuit in the same other simulation conditions (cfr. Fig. 2.5). Its peak is about 200 A at $V_{dc} = 100$ V and then it slightly decreases to 180 A at $V_{dc} = 400$ V, because of self-heating.

However, the V_{DS} of the two GaN HEMTs undergo completely different behavior in comparison to the ideal symmetrical case, as clearly visible in Fig. 2.21, where V_{DS} and T_j of the two devices are shown. For lower V_{dc} (100 V and 200 V), even if device Q_2 turns on after its blocking phase and should be subjected to almost all V_{dc}, working in its saturation region, its V_{DS} actually goes to zero when the SC starts at 2 µs. On the contrary, V_{DS} of device Q_1 increases at about the DC-link voltage. In this case device Q_1 is working in its saturation region and determines the SC current. Therefore it is also subjected to a high power dissipation, resulting in the increase of its T_j, that reaches about 200 °C at $V_{dc} = 200$ V.

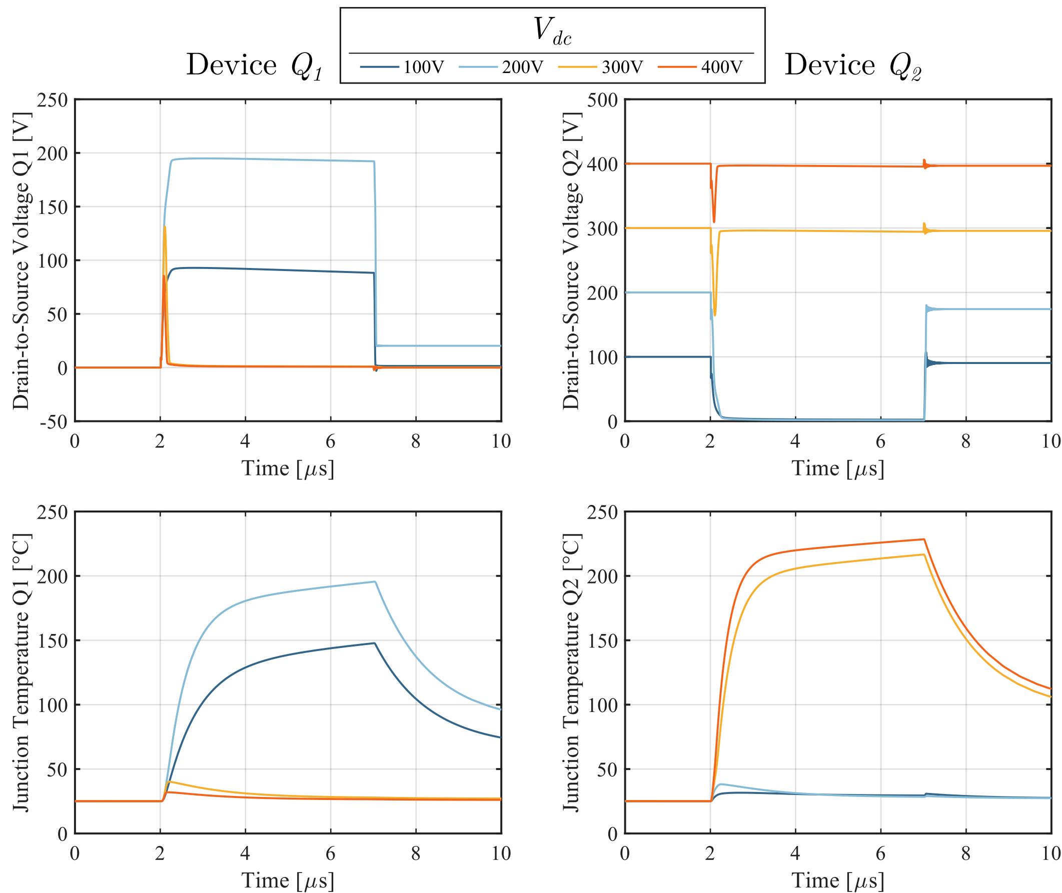
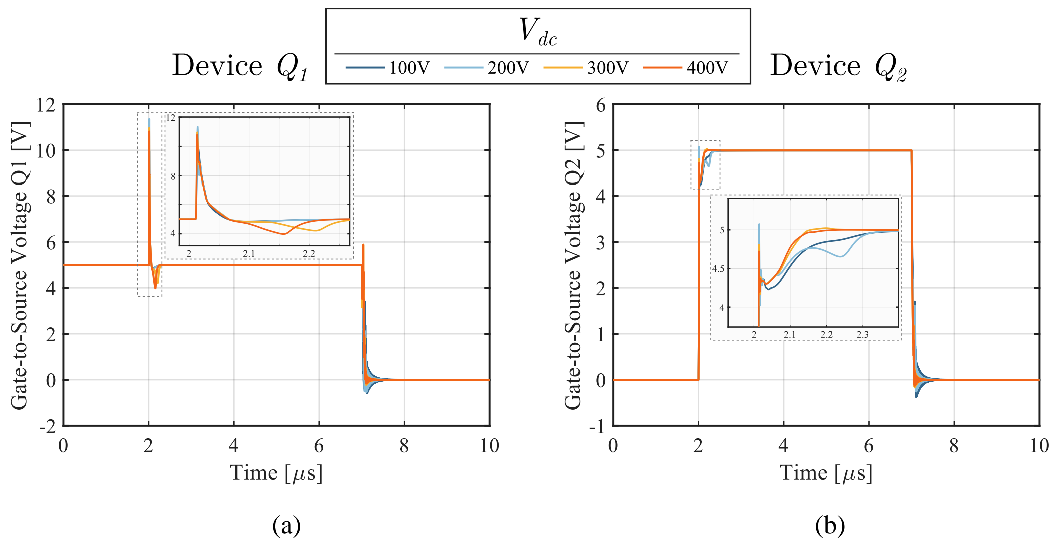


Fig. 2.21 Simulated V_{DS} and T_j of each GaN device in the presence of mismatch in common-source inductances of the two GaN HEMTs, with $L_{s1} = 1.0$ nH, $L_{s2} = 0.4$ nH and a V_{dc} variation from 100 V to 400 V.

At higher V_{dc} (300 V and 400 V in the simulation), the behavior of the two devices is reestablished as in the ideal case without mismatch. Device Q_2 suffers from the highest power dissipation and experiences a huge temperature increase, higher than 200 °C. For the sake of completeness, V_{GS} of the GaN devices are also reported in Fig. 2.22, where a detail of the waveforms at the beginning of the SC is also highlighted. In comparison to the ideal case, V_{GS} of device Q_1 has a peak higher than 10 V and a consequent voltage drop when the SC current starts to increase, because of the large inductance in the gate loop and the high *di/dt*. Also V_{GS} of device Q_2 is affected by the presence of a common-source inductance in the gate loop and shows a voltage drop that is lower than in V_{GS} of device Q_1.



(a) (b)

Fig. 2.22 Simulated V_{GS} of the two GaN HEMTs in the presence of mismatch in common-source inductances of the two GaN HEMTs, with $L_{s1} = 1.0$ nH, $L_{s2} = 0.4$ nH and a V_{dc} variation from 100 V to 400 V.

To highlight the operation of the two GaN HEMTs in this condition during the SC, the I – V locus of the drain current and voltages has been traced. It has been derived from the simulated waveforms I_{SC}, $V_{DS,1}$ and $V_{DS,2}$ in the time domain and computed for the time instants included in $t_0 = 2$ µs and $t_f = t_0 + T_{SC} = 7$ µs. The I – V loci at the different simulated V_{dc} are plotted in Fig. 2.23, where the initial and final time instants are also highlighted.

At the start of the SC event, because of the high *di/dt*, the drain-source voltage of Q_1 exhibits an important transient increase due to the large parasitic inductance on the source L_{s1}. At the same time, the opposite happens to device Q_2 and its V_{DS}, at the beginning equal to V_{dc}, has a consistent voltage drop. This can be seen both from Fig. 2.21 and the I – V loci in Fig. 2.23. When $V_{DS,1}$, that starts from 0 V, becomes higher than $V_{DS,2}$, that

starts from V_{dc}, the behaviors of the two GaN HEMTs are swapped and $V_{DS,1}$ tends to V_{dc} while $V_{DS,2}$ goes to its on-state voltage. This happens when V_{dc} is lower than 300 V in the simulated test conditions. In this case, the power dissipation of Q_1 is higher than in Q_2, since it is subjected to high V_{DS}. When V_{dc} is higher than 300 V $V_{DS,1}$ and $V_{DS,2}$, even showing a transient increase and decrease respectively, do not overlap anymore and $V_{DS,1}$ tends to its on-state voltage drop, while $V_{DS,2}$ tends to V_{dc}.

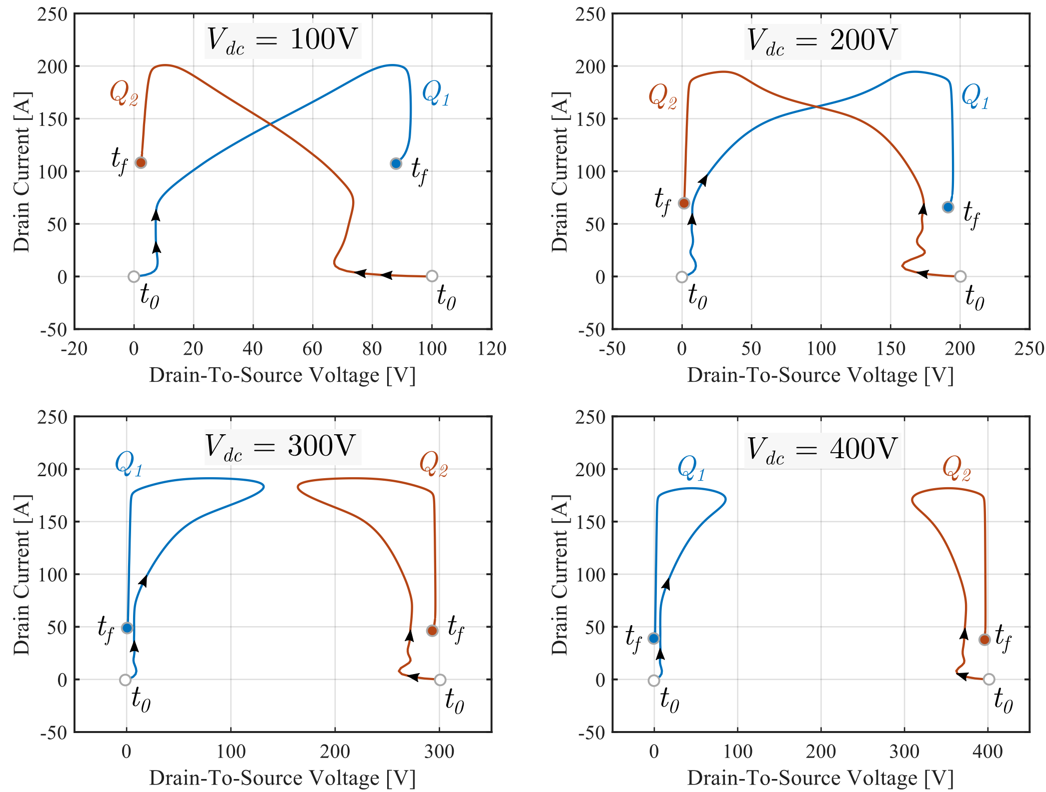


Fig. 2.23 I – V loci of the two GaN HEMTs during the SC in the presence of mismatch in common-source inductances, with $L_{s1} = 1.0$ nH, $L_{s2} = 0.4$ nH.

The behavior of the two GaN HEMTs in this condition can be explained considering their output characteristics and the gate voltage and temperature waveforms of Fig. 2.21 and Fig. 2.22. After the transient turn-on phase of device Q_2, the steady-state equilibrium point is determined by the intersection of the output characteristics of the transistors. The difference in the stray inductances on the source path is responsible of the reduction of $V_{GS,2}$ with respect $V_{GS,1}$ for $V_{dc} < 300$ V, as highlighted in Fig. 2.22. This leads Q_1 to block a higher percentage of V_{dc} and its higher V_{DS} also causes the increase of its junction temperature $T_{j,1}$, that becomes higher than $T_{j,2}$ of Q_2, as shown in Fig. 2.21. Since $T_{j,1} > T_{j,2}$, the output characteristic of Q_1 intersects the one of Q_2 in the linear region of this latter

one, leading Q_1 to operate in the saturation region and Q_2 to work in the linear region at the steady state. For $V_{dc} \geq 300$ V the opposite situation is established, as Q_1 shows a larger gate voltage drop at the beginning of the SC and, even if it goes in the saturation region during the transient, device Q_2 undergoes a higher temperature increase and in the steady state it works in the saturation region, while Q_1 works in the linear region.

2.3 Discussion

The simulation analysis performed in this chapter identifies that the SC behavior of a GaN-based HB is mostly determined by the GaN HEMT that turns on after its blocking phase, which behaves as a controlled current source, determining the SC current. It is also subjected to the highest thermal and electrical stress, since it works in the saturation region. In the case study of a 650 V – 60 A GaN-based HB, the maximum current peak is about 240 A and the junction temperature of the most stressed device can reach more than 240 °C for a 5 μs SC pulse-width in the worst conditions, according to the thermal model of the manufacturer.

The SC is influenced by numerous operating conditions and parameters. In particular, the DC-link voltage has a major impact on the power dissipation and the temperature increase of the devices.

The gate-source voltage controls the maximum drain current of the GaN HEMT and therefore, the peak SC current is strongly dependent on its value, while during the SC event, the increase of the junction temperature determines the reduction of the current.

The use of a large gate resistance is beneficial to slow down the *di/dt* and limit the effects of parasitic inductances in the circuit. Among the parasitic inductances, the common-source one plays a crucial role in determining eventual instabilities. Moreover, a mismatch in the board layout that involves the source connection between power and signal loop of the two GaN HEMTs can cause a higher power dissipation on the device with larger common-source inductance, swapping the behavior of the two GaN HEMTs under specific DC-link voltages and circuit parameters.

The gate leakage current increase during the SC due to the temperature increase is not considered in the simulation model of the 650 V – 60 A GaN HEMT, even if its role during the SC is widely confirmed in the literature. Therefore, the impact of the gate-source voltage reduction during the SC is also not incorporated in the simulation model, affecting the accuracy and reliability of the simulations.

3
Design and realization of a 650 V GaN-based Half Bridge

In this chapter the printed circuit board (PCB) realized for the experimental testing of 650 V – 60 A GaN HEMTs will be presented and the main steps of the design process will be discussed. The different sections of the circuit will be also described, focusing in particular on the power section, the driver circuit and the auxiliary power supply. Finally, a brief description of the FPGA implementation to generate the driving signals used for the experimental tests will be provided.

3.1 Circuit scheme

To achieve the goal of analyzing the SC behavior of a GaN-based Half Bridge (HB), a hardware prototype has been designed and realized on a PCB. The basic scheme of a HB with two identical GaN devices is shown in Fig. 3.1.

As in any converters, three main sections can be identified. They are described in the following.

- The power section consists of the DC-link bus capacitor C_{bus}, the high-side (HS) device Q_1 and the low-side (LS) device Q_2. The input DC voltage source, not shown in Fig. 3.1, provides the voltage V_{DC} at the DC-link referred to the power ground PGND. The devices Q_1 and Q_2 form the HB and the common point V_{AN} is the output connection, which can be eventually connected to a load.

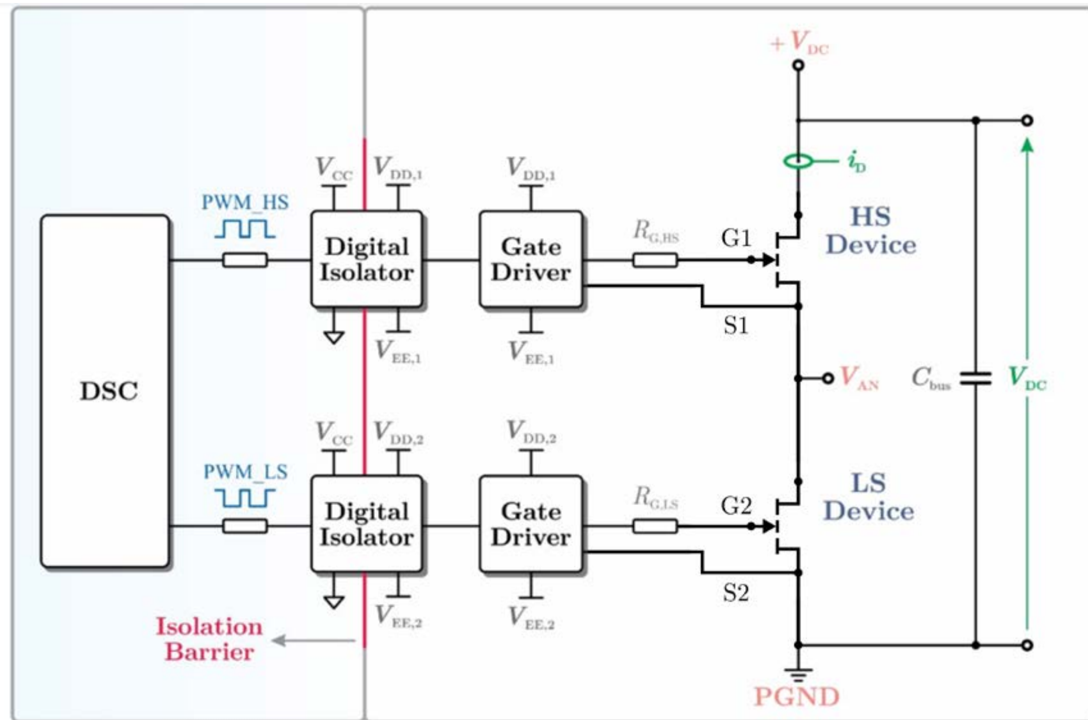


Fig. 3.1 Circuit schematic of the GaN-based Half Bridge.

- The signal section consists of a gate driver and a digital isolator for each device and by a digital signal controller, that generates the driving signals according to the desired logic. The gate driver provides the required current and voltage to switch on and off the power device and is connected to the gate through the gate resistor R_G. The digital isolator creates an isolation barrier between the low voltage and the high voltage sections, also providing a level shift of the input logic signals.
- The last section is made of the auxiliary power supply, consisting in different voltage regulators that provide the various voltage levels required by the digital isolators and the gate drivers from a common input low voltage. Although the circuit related to the auxiliary power supply is not shown in Fig. 3.1, the different voltage levels can be identified: V_{cc} is the input voltage, from which the voltage levels for the high-side device, V_{DD1} and V_{EE1}, and for the low-side device, V_{DD2} and V_{EE2}, are derived.

3.2 Design of the test board

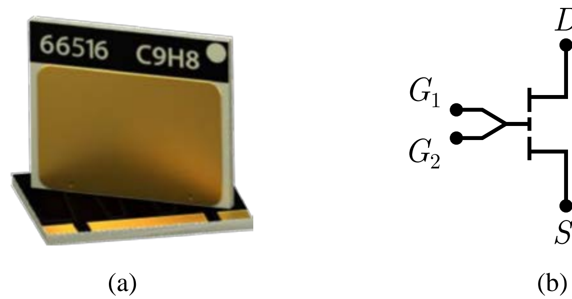
In this section the design steps carried out to realize the circuit are described, focusing on the design choices held in the different stages of the GaN-based HB defined above.

3.2.1 Power stage

The GaN devices chosen for the analysis of the SC behavior of the HB are two 650 V – 60 A e-mode GaN HEMTs GS66516T produced by GaN Systems. This choice derives from the flexibility that a device of such ratings can find in many power electronics converters. In fact the 650 V breakdown voltage enables the use of these GaN HEMTs in all applications that exploit a 300 V or 400 V DC bus, such as single-phase inverters in photovoltaics and motor drives, and DC/DC converters for on-board chargers in electric vehicles and data centers [20], [21]. Moreover, the high drain current rating of 60 A makes this GaN HEMT a suitable alternative to SiC MOSFETs for medium and low power applications. A 650 V cascode GaN device could represent a valid alternative to the selected e-mode GaN HEMT, especially due to its advantage in terms of driving. In fact, the presence of a low voltage Si MOSFET allows the use of a higher gate voltage that would facilitate the design of the driving circuit and would allow the use of common low-cost drivers. Moreover, the higher threshold voltage of cascode devices makes them less sensitive to noise and false turn-on. However, the presence of a low-voltage Si MOSFET in the cascode configuration causes an increase in the total $r_{DS,on}$ and the presence of a reverse recovery charge Q_{rr}, affecting the switching behavior of the device. Moreover, the SC robustness of 650 V cascode devices has been proven to be lower than e-mode GaN HEMTs [34], [35]. These latter considerations brought to the choice of the 650 V – 60 A GaN HEMT as the objective of the SC analysis of the GaN-based HB.

The package and the circuit symbol of the 650 V – 60 A GaN HEMT used in the test board are shown in Fig. 3.2. The device has four pins, with dual gate pads to achieve an optimal board layout, and a top-side thermal pad that is internally connected to the source and the substrate. The package material is high temperature epoxy-based PCB material. Some of the most meaningful characteristics of the device are summarized in Table 3.1, though the full datasheet is available in [50].

From the characteristics of the device, it is worth noting a wide range of variation for the threshold voltage $V_{GS,th}$, the on-resistance $r_{DS,on}$ and the drain leakage current I_{DSS} at the nominal conditions $T_j = 25$ °C and $V_{GS} = 6$ V. In addition, all these parameters, as well as the gate current I_{GS}, are strongly sensitive to temperature and undergo an important variation during the SC event, as it causes an extreme increase of the junction temperature that can reach far higher values than 150 °C.



(a) (b)

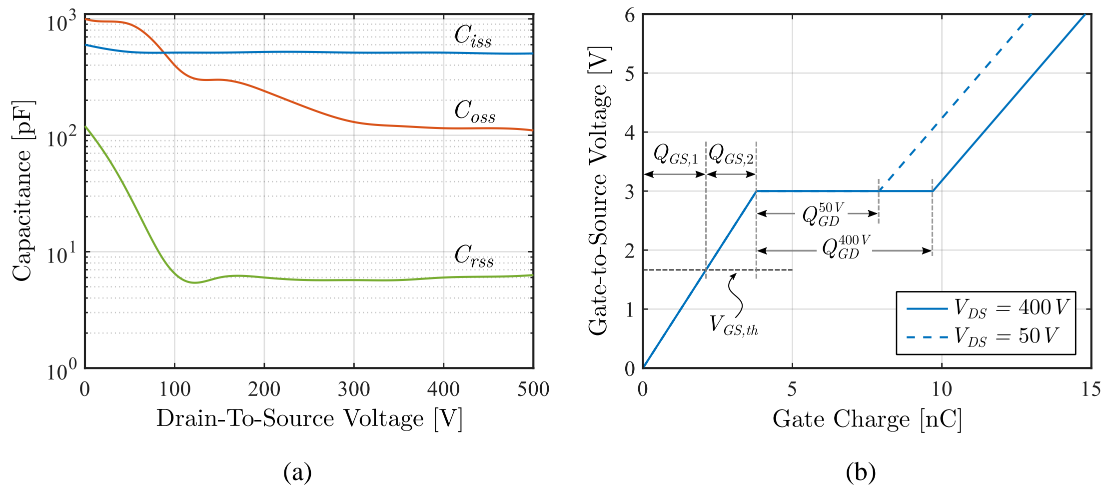
Fig. 3.2 Picture of the 650 V – 60 A GaN HEMT (a) and circuit symbol (b).

Table 3.1 Some of the main characteristics of GS66516T ($T_j = 25$ °C and $V_{GS} = 6$ V, unless specified).

Characteristics of GS66516T		
Symbol	***Value***	***Unit***
$V_{DS,max}$	650	V
$I_{D,max}$	60	A
V_{GS}	-10 ÷ 7	V
$V_{GS,th}$	1.1 ÷ 2.6	V
$r_{DS,on\ @25°C}$	25	mΩ
$r_{DS,on\ @150°C}$	65	mΩ
I_{GS}	320	μA
$I_{DSS\ @V_{GS}=6V}$	4 ÷ 100	μA
T_j	-55 ÷ 150	°C

The temperature dependence of the on-resistance is well addressed on the manufacturer datasheet, but very poor information are provided about the temperature dependence of the other parameters, that however need to be considered especially during the SC operation.

The characteristics of the capacitances and the related charges have been described in Chapter 1 and the $C - V_{DS}$ and $Q_G - V_{GS}$ graphs of the GS66516T, taken from the datasheet, are reported here in Fig. 3.3 for completeness. The very low Q_G and capacitance values allow the device to operate at a very high switching frequency of more than 10 MHz. For example, during a hard switching cycle in the conditions $V_{DS} = 400$ V, $V_{GS} = 0 – 6$ V and $I_D = 20$ A the device exhibits extremely fast rise and fall times of 12 ns and 22 ns, respectively, and very low turn-on and turn-off delays of 4 ns and 15 ns, respectively. This also leads to low switching energy losses, that are about 134 μJ at the turn-on and 17 μJ at the turn-off.



(a) (b)

Fig. 3.3 Drain-to-Source voltage dependence of C_{iss}, C_{oss} and C_{rss} (a) and Gate charge characteristic (b) of GS66516T.

The Safe Operating Area (SOA) of the GS66516T, taken from the datasheet, is shown in Fig. 3.4, where three different boundary regions are highlighted, defining the maximum time for which the device is expected to operate without self-damages, considering the maximum power dissipation capability and the voltage and current limits. The most stressing condition for high V_{DS} with $I_D = 120$ A is bearable for 200 ns. During the SC the drain current will exceed its maximum value and therefore the device will operate far beyond the SOA.

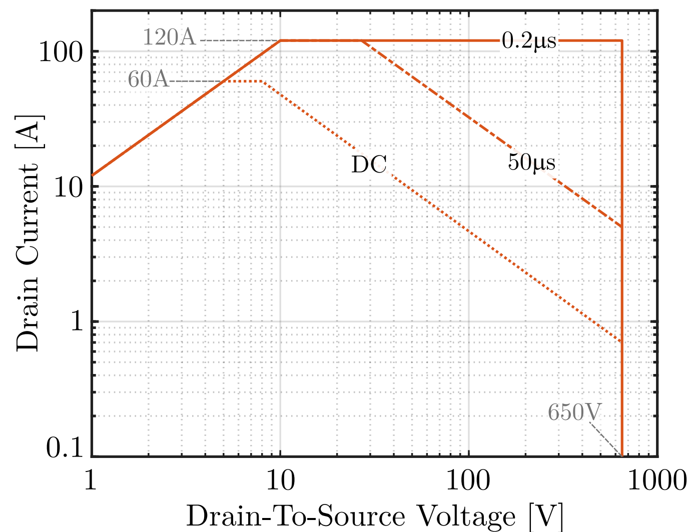


Fig. 3.4 Safe Operating Area (SOA) of GS66516T at $T_j = 25$ °C.

3.2.2 Bus capacitors

The operation of the HB in SC conditions is characterized by a high current flowing in the power devices. During the SC, the decoupling capacitors have to sustain the transient SC current without experiencing an excessive voltage drop, in order to maintain fixed the voltage on the HB. In the case of SC on a single 650 V – 60 A GaN HEMT, the highest peak and mean values of the current occur at low temperatures, maximum V_{GS} and low V_{DS} in the saturation region. According to the test results showed in [34], the worst tested condition is at $V_{GS} = 6$ V, $V_{DC} = 50$ V and $T_j = 25$ °C, where the SC current I_{SC} shows a peak value of about 230 A and after that decreases to about 120 A during a 10 μs SC pulse-width, because of the increase of temperature.

In the case study of the SC on a HB the current is expected to have the same behavior, at least in first analysis, so the above values are taken as the worst case to choice the capacitor value. Assuming that the SC event starts at the time instant $t = 0$ with initial capacitor voltage $v_C(0) = V_{C0}$, at the end of the SC pulse-width T_{SC}, v_C will be:

$$v_C(T_{SC}) = V_{C0} - \frac{1}{C}\int_0^{T_{SC}} I_{SC}(t)\, dt \tag{3.1}$$

where the time dependence of I_{SC} is related to the evolution of junction temperature over time. The values of $I_{SC}(t)$ have been extracted from [34] and used to compute the mean SC current $\bar{I}_{SC}$, that is equal to about 140 A in the worst case. So (3.1) can be written as

$$v_C(T_{SC}) = V_{C0} - \frac{1}{C}\bar{I}_{SC}T_{SC} \tag{3.2}$$

Defining the maximum admissible voltage drop $\Delta V_{C,max} = V_{C0} - v_C(T_{SC})$, the required capacitance value can be found as

$$C \geq \frac{\bar{I}_{SC}T_{SC}}{\Delta V_{C,max}} \tag{3.3}$$

In the design process, the capacitance has been chosen considering a maximum voltage drop $\Delta V_{C,max} = 15$ V for a SC pulse-width $T_{SC} = 5$ μs, obtaining $C \geq 80$ μF.

Ceramic capacitors of different capacitance values and 450 V voltage rating from TDK have been used as decoupling capacitors, while the main DC-link is composed by 14 x 22 μF/450 V aluminum electrolytic capacitors from Vishay.

3.2.3 Drivers and digital isolators

GaN HEMTs can switch faster than SiC and Si MOSFETs, so particular attention should be paid in designing the driver circuitry because of the high *dv/dt* and *di/dt*. In fact, the fast switching transitions of voltage and current can result in noise coupling on the gate drive loop, leading to the presence of spikes on the gate that can overcome its maximum ratings or occur in false turn-on. Although this issue exists for all GaN devices, it is even more critical for 650 V HEMTs in HB topologies, because high *dv/dt* occur in the switching cycle.

The first priority is to control the noise coupling from the power loop to the gate drive loop. This can be achieved by a careful layout design and the reduction of gate impedance. Moreover, the noise coupling can be mitigated in a different way for turn-on and turn-off.

During the turn-off it is crucial to control the Miller effect because of the high *dv/dt*, that can cause false turn-on of the off-state device. This problem can be addressed using two different resistors for turn-on and turn-off, with $R_{G,off} < R_{G,on}$, a strong pull-down of the gate and adding a clamping or TVS diode [112]. The use of negative V_{GS} for turn-off is also useful to prevent false turn-on, but it affects the reverse conduction losses, as described in (1.4.2), so it requires a trade-off between the control of Miller effect and the power loss.

The presence of stray inductance on the gate loop can cause oscillations and over/undershoot on the gate, because of the coupling with C_{iss}. In particular, the presence of a common source inductance creates a *di/dt*-sensitive feedback path between the power and the gate loops. In this case, the preferred solution is improving the layout, reducing the distance between the driver and the gate, using kelvin source connection and creating low inductance PCB tracks.

For a HB topology, there are two possibilities to design the driver circuit. The first is using a driver with dual outputs for both high-side and low-side which is internally isolated and the second is using full isolated single gate drivers, one for each device. In both cases, an isolated power supply providing the required voltage levels has to be provided. Another chance is to supply the high-side with a bootstrap circuit to provide the level-shift starting from a unique power supply with common ground.

The solution used in the 650 V GaN-based HB employs a single driver, digital isolator and isolated power supply for each HEMT, since this configuration achieves the best performances and ensures safe operations [112].

The driver used in the board is the LM5114A from Texas Instruments [113], whose block diagram is reported in Fig. 3.5. It has independent source and sink outputs with high current capability to easily control turn-on and turn-off switching times using two split

gate resistors. It is characterized by very fast switching speed and low propagation delay (12 ns). Moreover it provides inverting and non-inverting inputs that are TTL/CMOS logic compatible and covers a wide range of voltage levels (4 V – 14 V) with undervoltage lockout function. The driver used in the test board has a WSON package with an exposed pad to facilitate thermal dissipation. A summary of the driver's key-features is reported in Table 3.2, while a complete description is provided in [113].

Table 3.2 Key features of the LM5114A ($V_{DD} = 4.5$ V, $C_L = 1000$ pF, unless specified).

Characteristics of the LM5114A			
Symbol		***Value***	***Unit***
V_{DD}	Supply voltage	4.0 – 14.0	V
V_{IH}	Logic 1 input voltage	$0.67 \cdot V_{DD}$	V
V_{IL}	Logic 0 input voltage	$0.33 \cdot V_{DD}$	V
t_R	Rise time	8	ns
t_F	Fall time	3.2	ns
t_{D-on}	Turn-on delay	12	ns
t_{D-off}	Turn-off delay	12	ns
$T_{j,max}$	Maximum temperature	150	°C

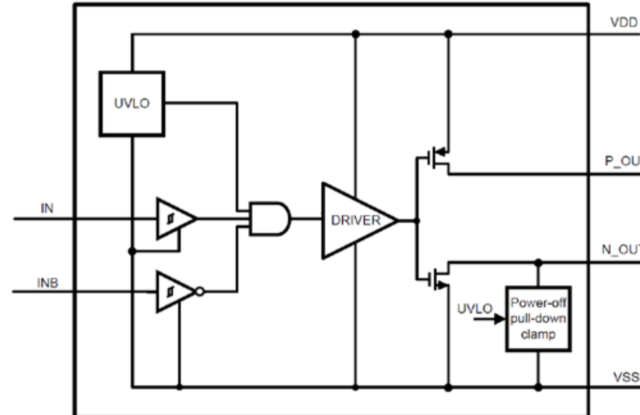


Fig. 3.5 Block diagram of the LM5114 driver by Texas Instruments.

The digital isolator used to provide the input signals to the driver is the ISO7720F by Texas Instruments [114], which has a robust capacitive isolation barrier up to 5 kV, a high common mode transient immunity up to 100 kV/µs and a maximum data rate of 100 Mbps. Moreover it has a supply range from 2.25 V to 5.5 V and a low propagation delay of 11 ns (typical). It also ensures safe operation in case of power supply or input

signal loss by forcing the output to the low state. The main characteristics of the digital isolator are listed in Table 3.3 and a full description is available in [114].

Table 3.3 Key features of the ISO7720F ($V_{CC} = 5$ V unless specified).

Characteristics of the ISO7720F			
Symbol		***Value***	***Unit***
V_{CC1}, V_{CC2}	Supply voltage	2.25 – 5.5	V
DR	Data rate	0 – 100	Mbps
C_{IO}	Barrier capacitance	0.5	pF
V_{ISO}	Isolation voltage	5000	V
$CMTI$	CM transient immunity	85 – 100	kV/μs
t_{PD}	Propagation delay	6 – 16	ns
t_r, t_f	Rise and fall times	1.8 – 3.9	ns
$T_{j,max}$	Maximum temperature	150	°C

The schematic of the digital isolator and driver circuit is shown in Fig. 3.6. The same circuit is used for both the high-side and low-side devices. The OUTA of the digital isolator is used as enable signal for the driver, while the logic signal is connected to INB of the digital isolator and then the related OUTB is connected to the non-inverting input of the driver. A clamping diode DGS1A and a pull-down resistor are connected between gate and source of the GaN device and also the insert of a small capacitance has been planned, though not placed on the board. A BNC connector has been placed to sense the gate-to-source voltage.

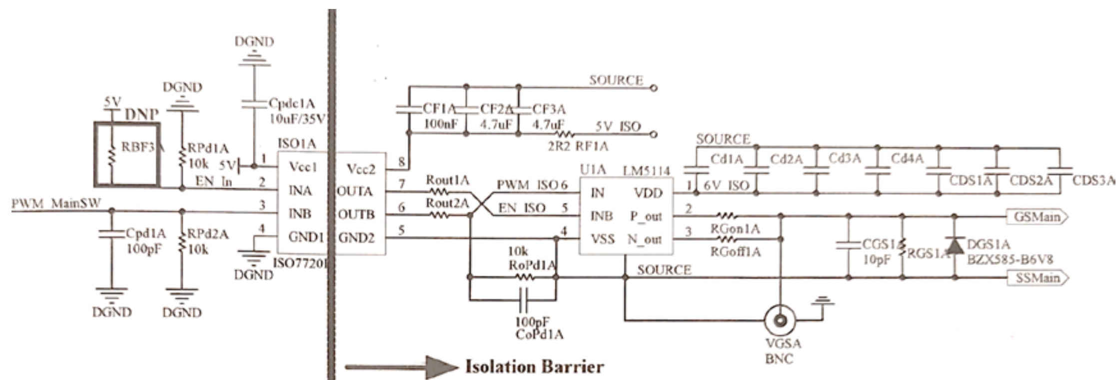


Fig. 3.6 Schematic of the driver and digital isolator circuit of the designed test board.

The logic signal in input to the digital isolator is provided by an FPGA board and sent to the PCB through fiber optics HFBR-x521Z with 5 MBd signal rate.

3.2.4 Auxiliary power supply

The isolated power supply provided to the driver circuit is derived through different stages of regulators. The input power supply is 5 V and can be provided by a voltage source such as a benchtop power supply. It feeds all the fiber optics receiver circuit, the primary side of the digital isolators and an isolated DC/DC converter with 9 V output voltage. From this isolated 9 V voltage, other two linear regulators are used to provide the 5 V power supply for the secondary side of the digital isolator, and the voltage level for the driver defining the positive value of V_{GS}. The 0 V level is used to turn-off the gate of the two HEMTs, avoiding the employment of a further regulator to provide another voltage level.

The schematic of the power supply circuit is shown in Fig. 3.7. The PDS2-S5-S9-M from CUI Inc [115] has been chosen to provide the 9 V_ISO output. It is a 2 W isolated DC/DC converter with SMT package and short circuit protection. In addition, it requires the output capacitors and the EMI filter at the input, as placed in the schematic. Then the isolated voltage levels for the digital isolator and the driver are provided by the linear regulators LP2985 from Texas Instruments [116]. This family of voltage regulators offers a wide range of output voltages from 2.5 V to 16 V with small package size, overcurrent protection and low output impedance. Moreover it performs the output voltage regulation with very high precision (1% tolerance) and for this reason it has been chosen to provide the positive voltage level of V_{GS}.

A 5.0 V regulator from this family is used to supply the secondary side of the digital isolators, while regulators with different output voltages have been selected for the driver, since different V_{GS} values are used to characterize the SC behavior of the HB. The 3.0-, 4.0, 5.0- and 6.1- V regulators have been selected for this purpose.

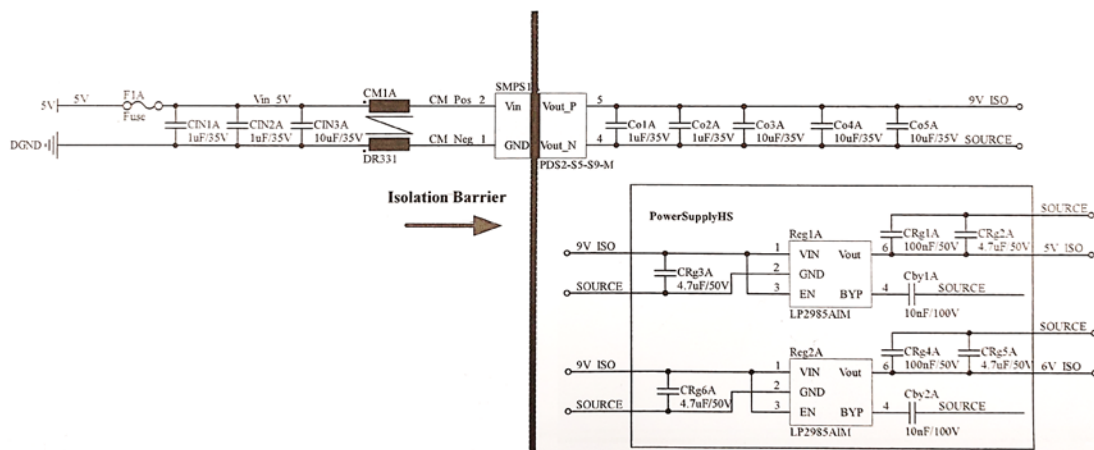


Fig. 3.7 Schematic of the power supply circuit of the designed test board. The high-side and low-side power supply circuits are identical.

3.2.5 Control board

The control signals for the HB are generated through the Cyclone II FPGA board, that is interfaced with the board through the fiber optics. The logic signals S_1 and S_2 to perform a controlled SC on the HB are depicted in Fig. 3.8, where the characteristic time intervals for the test are highlighted. The time duration T_1 corresponds to the condition where a device is turned on and the other one is off and blocks the DC-link voltage. This time interval has been set constant to 5 μs. The second time interval T_2 represents the SC pulse-width, while T_3 is a delay added between the turn-off of the two devices and it has been fixed to 200 ns.

Since the FPGA control board is equipped with many switches with programmable functions, different values of the SC pulse-width T_2 have been assigned to them to speed up the test procedure. In addition, an enable pin has been set to inhibit the generation of the signals when it is low and a start key has been programmed to give the start-up to the SC test.

A microcontroller-based circuit could be used to generate the logic driving signals of the GaN HEMTs, even if this solution would require a high-performance microcontroller to accurately manage very short pulses and would still limit the resolution of the system to a few microseconds. In order to ensure a deterministic and accurate determination of the timing of the two devices and have a finer resolution, the FPGA-based approach was preferred. This choice enabled the generation of the driving signals with a 4 ns precision by using a 250 MHz clock provided by the FPGA board.

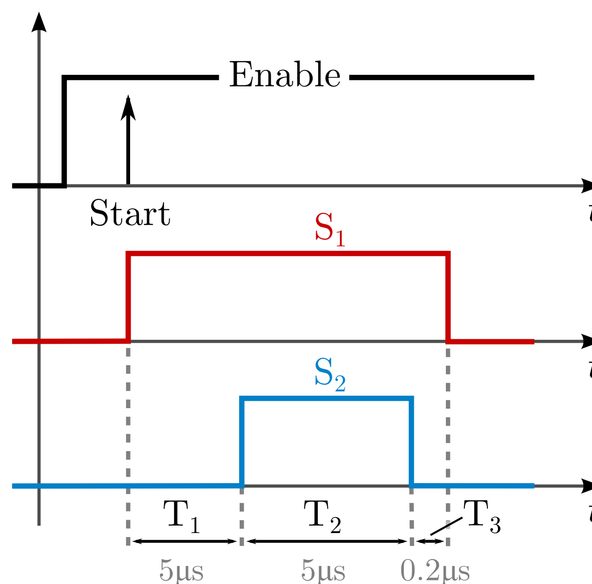


Fig. 3.8 Characteristic control signals for the SC test with related timings.

3.2.6 Realized prototype

During the realization of the GaN-based HB the following guidelines have been considered:

- Ensure insulation levels through appropriate spacing of contacts and components at different potentials.
- Minimize the value of the stray inductance along the board through the distribution of the various capacitors in the circuit and exploiting the busbar technique.

The PCB has been made in 4 layers and Fig. 3.9 and Fig. 3.10 shows the 3-D rendering of the top and bottom sides, respectively. The main sections described in the previous paragraphs are highlighted. Distributed capacitors have been placed in the whole board to reduce the parasitic inductance both on the signal and the power paths. Finally, Fig. 3.11 shows a picture of the realized 160 mm x 140 mm prototype.

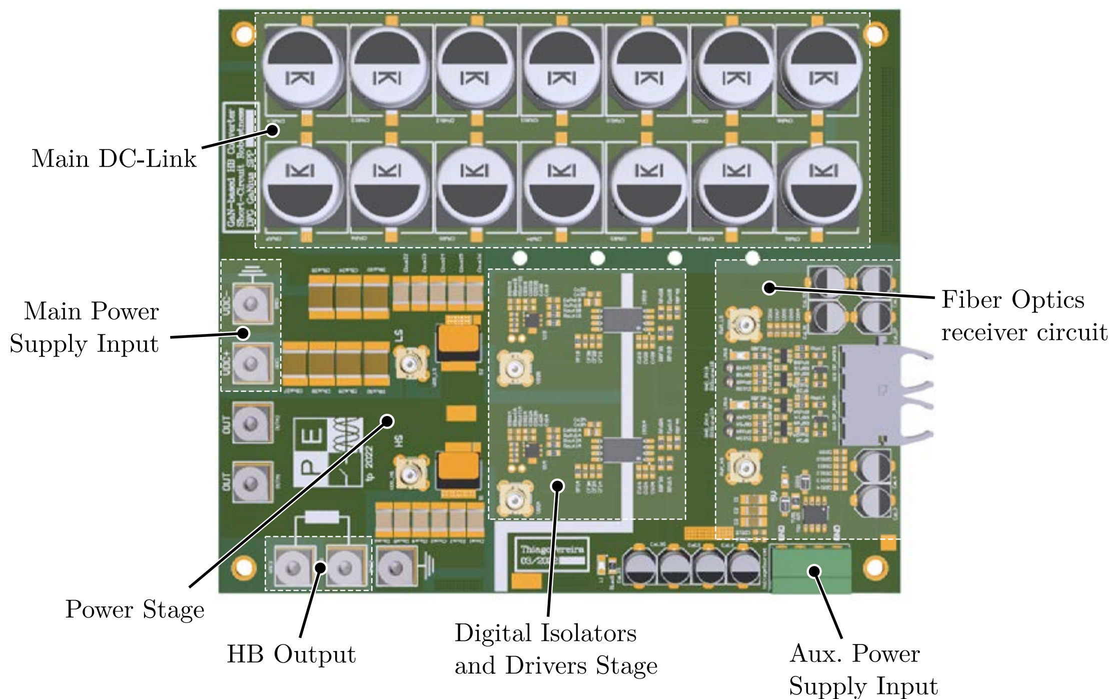


Fig. 3.9 3-D rendering of the realized PCB for the GaN-based Half Bridge: top view.

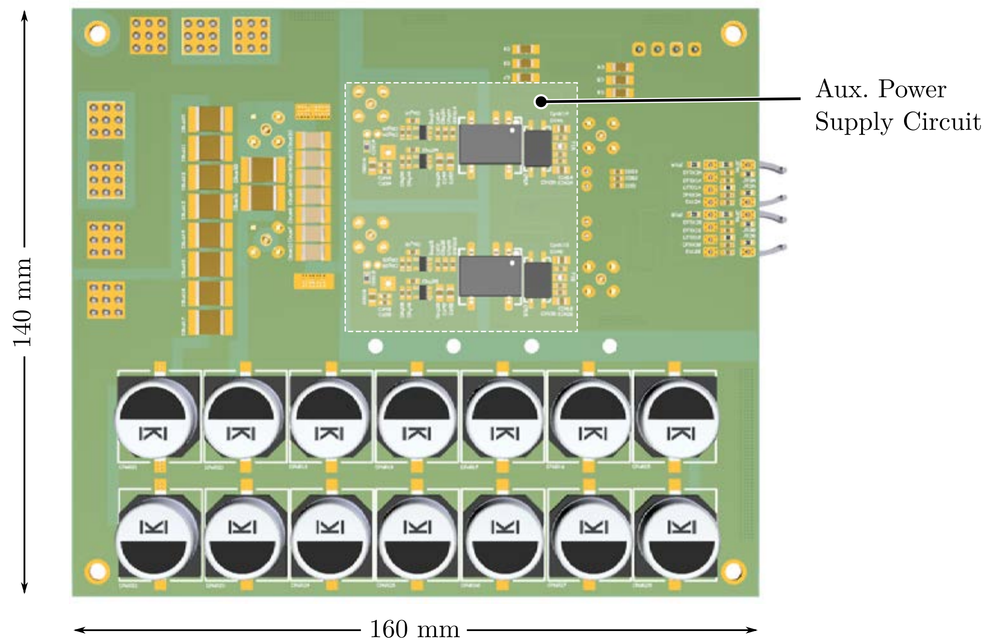


Fig. 3.10 3-D rendering of the realized PCB for the GaN-based Half Bridge: bottom view.

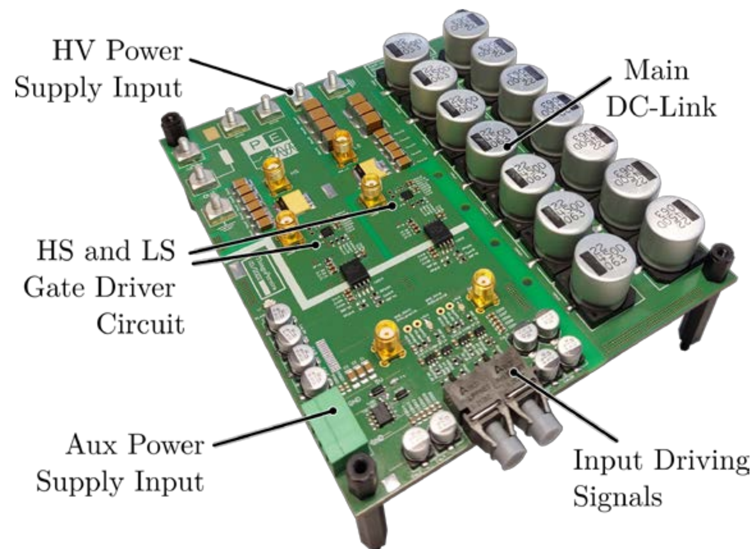


Fig. 3.11 Realized prototype of the GaN-based Half Bridge.

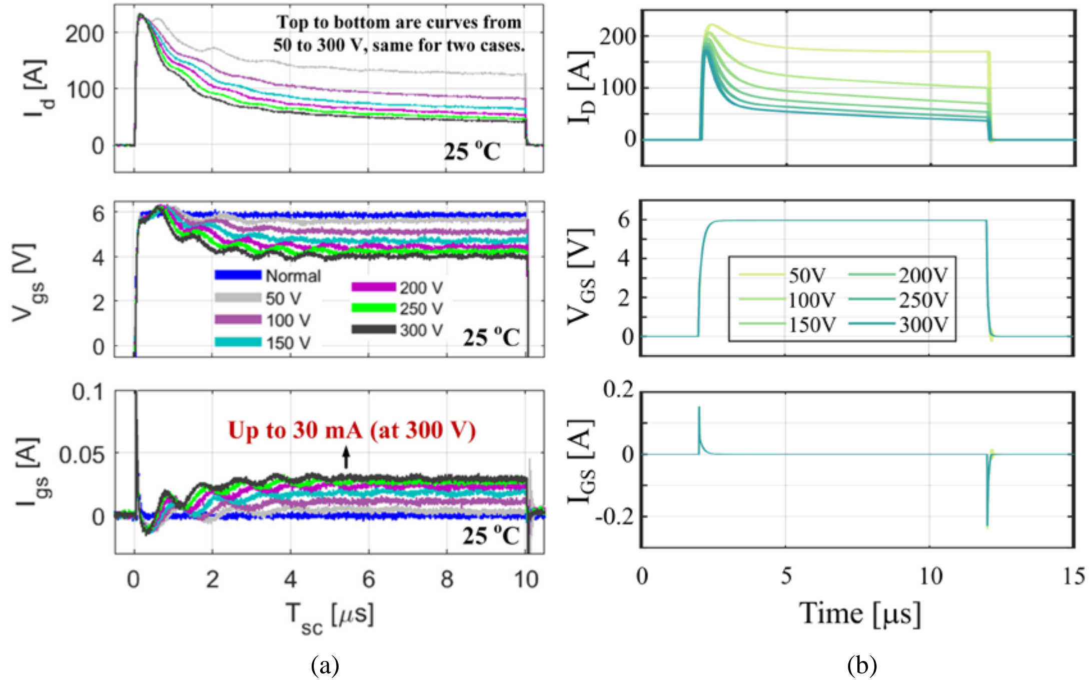
4
Modeling of GaN HEMTs in Short Circuit

Even if many investigations on the Short Circuit (SC) capability of normally-off p-GaN HEMTs have been conducted and presented in many works, poor analytical discussion is provided on the SC behavior of the GaN HEMT. This is mainly due to the physical complexity of GaN HEMT structure and the absence of a quite simple but at the same time accurate simulation model. The most accurate physical models, such as the ones proposed in [63], [65], [67], [68], introduce complex equations and numerous parameters and, even if possible, their use in simulating power electronic converters is not handy, also because of the long time required for the simulation. In fact, in this field a trade-off between accuracy and computational speed is commonly accepted, since the main goal is to simulate the entire system, including the main behaviors of the power device that can affect the operation of converters. For this reason, behavioral and semi-physical models are often preferred, since they are simpler and provide fast and sufficiently accurate results, therefore representing the best trade-off between time-cost and accuracy.

In the case of the SC behavior of GaN HEMTs, it would be greatly beneficial to have the availability of a reliable simulation model that represents all the mechanisms involved in the SC. Among the advantages of having an accurate simulation model, it could be an useful instrument to evaluate the SC behavior of a GaN device without exclusively performing SC tests, that are time-expensive and often result in the deteriorating many devices and producing high costs. Moreover, it could help in designing a protection circuit against SC for different GaN HEMTs.

For the specific case of the 650 V – 60 A GaN HEMT, and the other GaN devices of the same manufacturer, SPICE simulation models with different levels of accuracy are provided. However, even the most accurate one does not fully represent the real behavior of the GaN HEMT when operating in SC conditions. In fact, many manufacturer simulation models are mainly focused on the operation of the device in its linear region, which nevertheless hardly represent all the phenomena related to the SC operation, such as the gate leakage current increase. Anyway, it can be used to obtain a general overview on the SC behavior of the device, even if it is not fully comparable with the experimental results.

For example, Fig. 4.1 (a) depicts the experimental waveforms of SC current and gate voltage and current presented in [34], where SC tests are performed on a 650 V – 60 A GaN HEMT with $V_{GS} = 6$ V, a V_{dc} variation from 50 V to 300 V and case temperature $T_C = 25$ °C. The value of the gate resistor R_g is derived by voltage and current waveforms of the gate, since it is not reported by the authors, and it is 66 Ω. A LTSpice simulation in the same conditions is made to compare the results with the experimental data, shown in Fig. 4.1 (b).



(a) (b)

Fig. 4.1 Comparison between waveforms of drain current I_D and gate voltage and current, V_{GS} and I_{GS}, obtained from experimental results in [34] and LTSpice simulation (b) in the same conditions, for a V_{dc} variation from 50 V to 300 V.

As visible from the drain current waveforms, the simulation model incorporates the thermal effect, but it is not very accurate in determining the peak SC current, which is about 230 A in the experimental tests and it shifts from 230 A to 170 A in the simulation. Instead, the waveforms of gate voltage and current are completely different from the experimental ones, indicating that the gate leakage current effect is completely neglected by the model.

For this reason, a behavioral model for the 650 V – 60 A GaN HEMT is developed in this chapter, based on the drain and gate current characterization, with the aim of correctly simulating the SC behavior of this device. The model can be easily integrated in the SPICE simulation model of the manufacturer to improve its accuracy and, although developed for the 650 V – 60 A GaN HEMT, it is completely general and can be applied to other GaN devices of the same family and with the same physical structure, not only in SC conditions.

4.1 Drain *I* – *V* characterization

In general, the drain current I_D of the GaN HEMT is a function of the gate-source voltage V_{GS}, the drain-source voltage V_{DS} and the junction temperature T_j. In the saturation region, the V_{DS} dependence is slight and the device can be considered as a current source, whose value is controlled by V_{GS} and T_j. Therefore, it is necessary to determine the output I – V characteristic of the device.

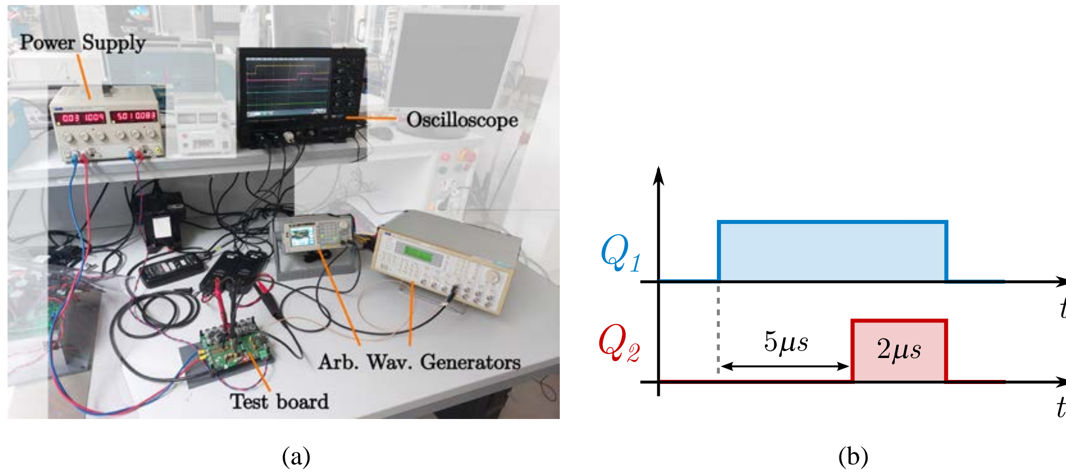
4.1.1 Test setup

The drain characterization has been performed according to the pulsed gate I – V test, using the designed PCB with two identical GaN HEMTs. The instrumentation used for the test consists in:

- an isolated 30 V – 2 A dual power supply, for the auxiliary and the main DC-link power supplies;
- two arbitrary waveform generators 40 MHz TGA1244 and a 10 MHz T3AFG10;
- a 4 channel – 1 GHz HDO6104-MS high definition oscilloscope with 2.5 GS/s sample rate;
- two 1500 V – 120 MHz HVD3106 differential probes;
- one 500 V – 500 MHz PP022-1 voltage passive probe;
- one Rogowski current transducer with 2.0 mV/A sensitivity;

- a FLIR thermal camera with wide temperature range (-20 °C to 250 °C).

A picture of the test setup is shown in Fig. 4.2 (a). The driving signals of the two devices have been generated through two synchronized arbitrary waveform generators, according to the logic signals shown in Fig. 4.2 (b), where the device Q_2 is in the off state for 5 µs blocking the DC-link voltage V_{dc} and after that is turned on for 2 µs to avoid an excessive increase of its temperature Therefore, Q_2 is the device under test (DUT) for the I – V characterization.



(a) (b)

Fig. 4.2 Setup for the experimental drain I – V characterization (a) and logic driving signals used for the tests (b).

The tests have been performed according to the following procedure:

- V_{GS} of the DUT was varied from 2 V to 6 V in 1 V steps;
- the DC-link voltage V_{dc} was changed from 0.5 V to 5 V in 0.5 V steps, from 5 V to 14 V in 1 V steps and from 14 V to 30 V in 2 V steps.
- The case temperature of the DUT was monitored with the thermal camera during the tests to ensure to keep constant its value. The ambient temperature during the test was 23 °C.

The DC-link voltage has been varied up to 30 V to reach at least the beginning of the saturation region for each applied V_{GS}. Since during each test the junction temperature undergoes a fast increase that is not detectable monitoring the case temperature, some seconds were waited between consecutive tests in order to ensure that T_j has returned to the same value of $T_C = 23$ °C. In fact, the thermal time constant of the DUT has been evaluated through the thermal model provided by the manufacturer and it is about 2 ms. A summary of the test conditions and the main parameters is provided in Table 4.1.

Table 4.1 Summary of the test conditions for the drain I – V characterization

Parameter	Description	Value / Range
$t_{p,Q1}$	Pulse duration of Q1	7 µs
$t_{p,Q2}$	Pulse duration of Q2, with a 5 µs delay	2 µs
V_{dc}	DC-link voltage applied on Q2	0 – 30 V
$V_{GS,Q1}$	Gate-to-source voltage of Q1	5 V
$V_{GS,Q2}$	Gate-to-source voltage of Q2	[2, 3, 4, 5, 6] V
I_D	Drain current, measured with a Rogowski coil (2.0 mV/A)	0 – 250 A

4.1.2 Results of experimental characterization

For each test, the measured waveforms are: V_{GS} of both GaN HEMTs and I_D and V_{DS} of Q_2. The peak drain current $I_{D,pk}$ and the value V_{DS}^* at which $I_{D,pk}$ occurs are used to build the drain I – V curves, as highlighted in Fig. 4.3, that shows the measured waveforms for the test conditions $V_{GS} = 6$ V, $V_{dc} = 30$ V. In this condition, the measured $I_{D,pk}$ is 230 A and the correspondent V_{DS}^* is 7 V. To evaluate the possible impact of the junction temperature increase in determining the value of $I_{D,pk}$, a simulation has been performed using the manufacturer's thermal model of the GaN HEMT. It showed that T_j increases of 1.5 °C from the initial 23 °C when the current reaches $I_{D,pk}$ in the condition $V_{GS} = 6$ V, $V_{dc} = 30$ V, that represents the worst case during the characterization. Therefore, the I – V curves can be considered at $T_j = 23$ °C with a maximum variation of +1.5 °C.

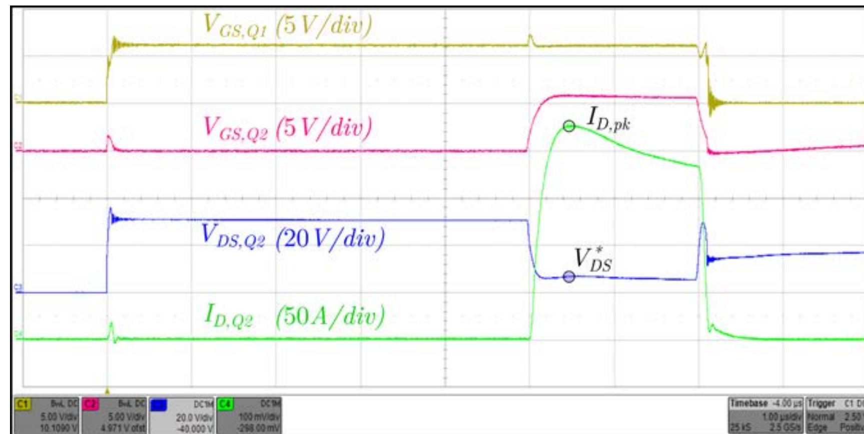


Fig. 4.3 Experimental waveforms in the test conditions: $V_{GS} = 6$ V, $V_{dc} = 30$ V, where the values $I_{D,pk}$ and V_{DS}^* are also highlighted.

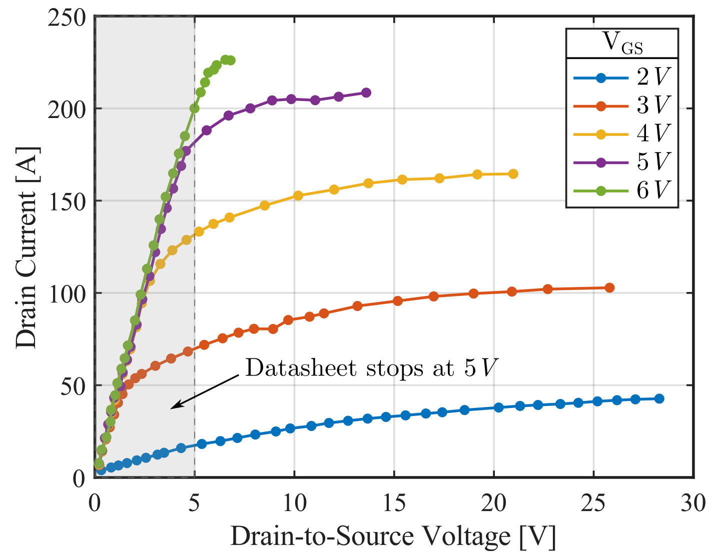


Fig. 4.4 Experimental results of the pulsed gate I – V characterization of the 650 V – 60 A GaN HEMT at different V_{GS} and T_j = 23 °C.

The results of the full I – V characterization are shown in Fig. 4.4, where the grey region represents the area of the $I_D - V_{DS}$ graph that is covered by data in the manufacturer datasheet. The datasheet doesn't provide sufficient information about the saturation region of the GaN HEMT in the output characteristics, as it can be easily seen from the figure, because it stops in the linear region for $V_{GS} > 3$ V. Even if the transfer characteristic is provided at $V_{DS} = 10$ V, the complete drain current behavior cannot be determined with the same accuracy for both the linear and the saturation regions, because of the lack of data in the saturation region. On the contrary, the experimental data obtained through this characterization are sufficiently thorough to derive a mathematical model to correctly fit the GaN HEMT drain current also in the saturation region.

The experimental results are compared with the I – V characteristics provided by the manufacturer's datasheet in Fig. 4.5. The results appear quite different mainly because of two facts.

First, the datasheet provides the electrical characteristics of the "average" device, that is not fully representative of all devices with the same rating. In fact, the threshold voltage ($V_{GS,th}$) of the device can vary in a wide range, from 1.1 V to 2.6 V, as defined in the datasheet, but the output and transfer characteristics shown by the manufacturer only refer to a single condition with $V_{GS,th} \approx 1.7$ V. It is likely that the tested device has a higher $V_{GS,th}$ that causes such differences between the experimental data and the datasheet. Second, the temperature effect should be considered, especially for the tests at $V_{GS} \geq 5$ V. In fact, the datasheet provides the results of DC characterization, where the self-heating

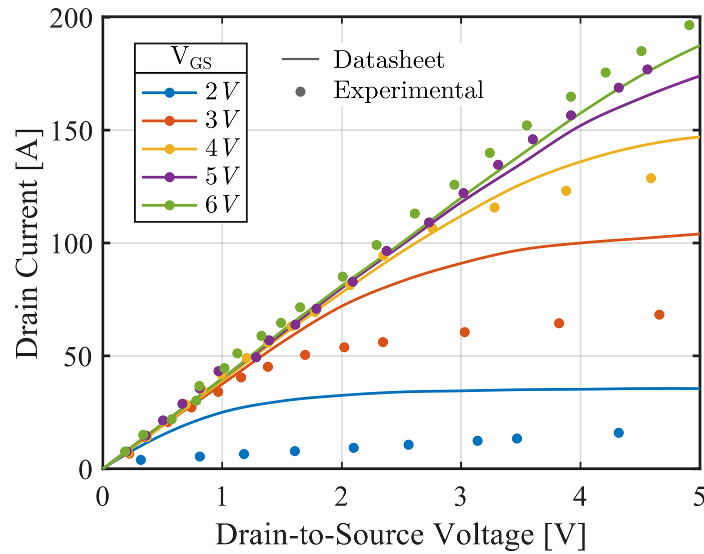


Fig. 4.5 Comparison between experimental results of the pulsed gate I – V characterization and the drain I – V characteristic provided in the datasheet of the 650 V – 60 A GaN HEMT.

effect is prominent at high currents and causes the reduction of the drain current. However, the pulsed I – V characterization is more meaningful both for the normal operation of the device in switching converters and for SC tests, where the gate of the GaN HEMT is driven according to a pulse signal. The pulsed-gate output curves are not affected by self-heating and higher current values in the characteristic are obtained. Furthermore, the lower $r_{DS,on}$ obtained from the experimental data is due to the lower T_j during the test, that instead was 25 °C for the characteristics of the datasheet.

4.2 Gate *I* – *V* characterization

The gate leakage has been extensively studied in the literature and has been shown to depend on multiple factors besides the applied voltage, such as the physical structure, the type of metallic contact, the temperature and the aging of the device [107]–[111], [117]. One of the common procedures to realize the gate structure of normally-off GaN HEMTs consists in creating a Schottky junction underneath the gate by inserting a p-doped GaN or AlGaN region between the metal contact and the GaN layer, as introduced in 1.4.1. This structure makes the gate leakage current follow the diode-like current behavior, involving physical mechanisms like Thermionic Emission (TE), Thermionic Field Emission (TFE), Poole-Frenkle Emission (PFE) and Fowler-Nordheim Tunneling (FNT) [110], [118], [119]. The gate leakage current behavior can be explained and modeled by a combination of these complex mechanisms, though this requires a deep knowledge of

quantum mechanics, solid state physics and, not the last, the physical structure of the GaN HEMT.

In order to derive a model of the gate leakage current of the 650 V – 60 A GaN HEMT to be incorporated in simulations, an experimental gate I – V characterization has been performed.

4.2.1 Test setup

The gate characterization was performed using a second identical PCB with only the DUT and the measurement connectors mounted and the instrumentation used for the tests consists in:

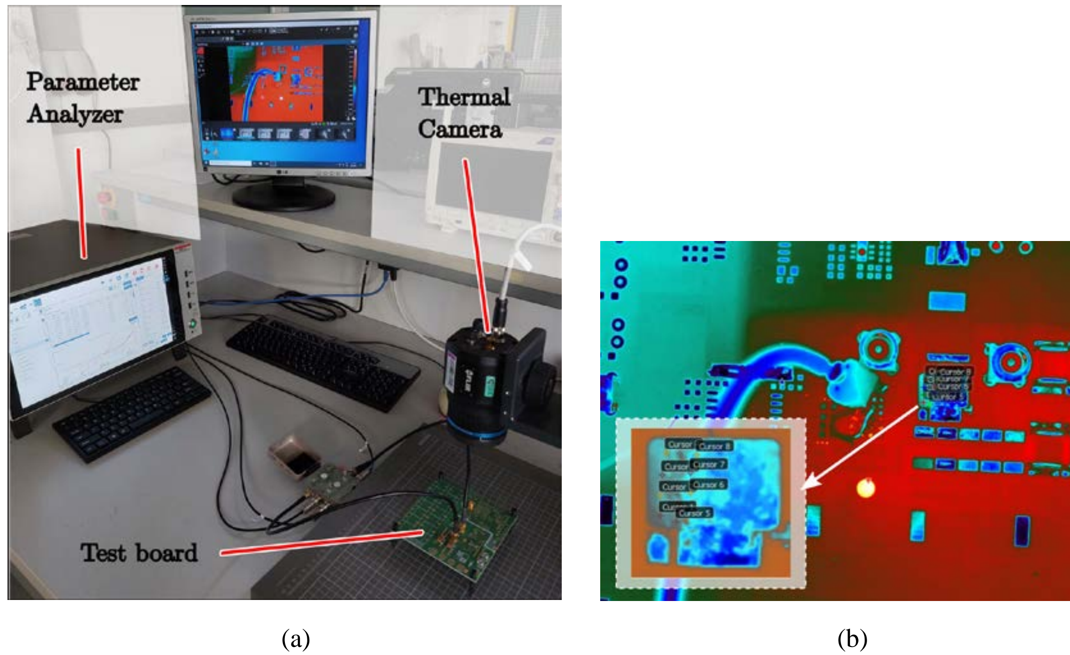
- the 4200A-SCS parameter analyzer;
- a FLIR thermal camera with wide temperature range (-20 °C to 250 °C);
- a controllable heating source;
- a PC for the online monitoring of the case temperature of the DUT.

The 4200A-SCS parameter analyzer offers the possibility to perform fast I – V characterization through dedicated source measure units (SMUs) up to 200 V/1 A with 100 fA measure resolution. Moreover, it has a built-in software that easily allows the user to run predefined tests, visualize and acquire the results. The connections between the instruments and the board were made through triaxial cables to ensure the correct measurement of the current. In fact the gate current can vary in a very wide range, from few nA to hundreds of mA, and therefore a crucial attention needs to be provided for very low current measurement. The DUT was connected to the parameter analyzer through its custom interface, with the source and drain contacts internally shorted and connected to the ground unit of the instrument. Instead, the gate contact was connected to a SMU.

The thermal camera was used to constantly monitor the case temperature T_C of the DUT and visualize the temperature profile over time thanks to a dedicated software for the online temperature monitoring. A picture of the setup is shown in Fig. 4.6 (a).

The tests have been led according to this methodology:

- The case temperature T_C of the DUT was set through a controllable heating source placed on the thermal pad of the device. T_C was varied starting from the ambient temperature up to 170 °C, waiting for the thermal steady state for each imposed T_C, in the way that $T_j = T_C$. After reaching the thermal steady state, the gate I – V characterization was performed with the parameter analyzer.



(a) (b)

Fig. 4.6 Setup for the experimental characterization of gate current (a) and picture taken from the thermal camera for the thermal monitoring of the DUT (b).

- The gate-source voltage V_{GS} was set in the parameter analyzer and it was varied from -4 V to 6 V in 0.25 V steps.

The temperature of the DUT was measured in different regions of its case to take into account the different temperature distribution along the case itself. A picture of the thermal camera measurement on the DUT is shown in Fig. 4.6 (b), where the different cursors indicate the points taken to evaluate the temperature. At the thermal steady state, T_j was computed as the average of the measured temperatures at those specific points.

4.2.2 Results of experimental characterization

The results of the gate I – V characterization are plotted in Fig. 4.7 versus V_{GS} at different T_j values, both in linear and in logarithmic scale of the current. The temperature was varied in about 8 °C steps according to the test procedure described above.

As visible in the figure, two main trends can be observed, that depend both on the applied V_{GS} and T_j. For positive V_{GS} and low T_j, the gate current exponentially increases up to $V_{GS} = 3$ V, where it shows a knee and then it continues to increase with a lower slope. As T_j is increased, the slope tends to be the same in all the positive V_{GS} region. For negative V_{GS} the situation is quite different, since for low T_j the current is practically

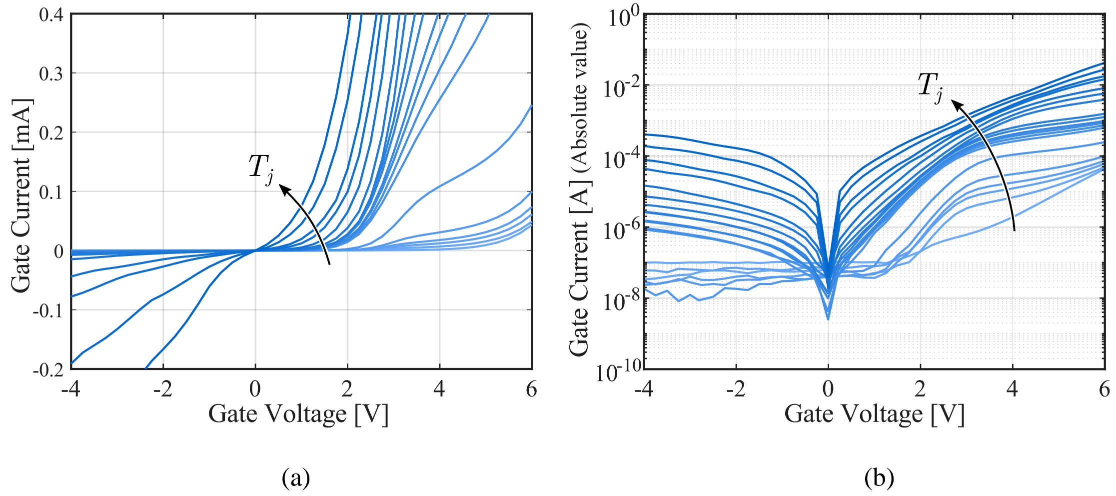


Fig. 4.7 Experimental results of gate I – V characterization of the 650 V – 60 A GaN HEMT at different T_j from 25 °C to 170 °C, in a zoomed linear scale (a) and in logarithmic scale (b) of the current.

constant and it varies between 10 nA and 100 nA, depending on T_j. For higher T_j the current becomes negative and its absolute value increases with T_j. However, unlike in the case for positive V_{GS}, no changes in the trend are observed when the absolute value of V_{GS} is increased. Moreover, for the same T_j and absolute value of V_{GS}, the absolute value of the current is lower in the negative V_{GS} region than in the positive one. In fact, considering the curves at the highest T_j, at $V_{GS} = 4$ V the current is about 6 mA, while its absolute value is 0.4 mA at $V_{GS} = -4$ V.

To analyze the temperature dependence of the gate current, the experimental data of Fig. 4.7 have been extracted at constant V_{GS} values and plotted versus T_j. The dependence of the gate current with T_j was derived for positive values of V_{GS} and it is shown in Fig. 4.8. Since the GaN HEMT is commonly driven in the off state with $V_{GS} = 0$ V and the gate leakage current mainly impacts the operation of the device in its on state, only positive values of V_{GS} have been considered for the temperature dependence. As visible in Fig. 4.8, the T_j dependence is also of exponential type, as the trends with T_j are quite linear in the logarithmic scale of the current.

Considering $V_{GS} = 6$ V, the gate current is about 30 μA at 25 °C and it becomes ten times higher at 70 °C. At $T_j = 150$ °C, which is the maximum operating temperature for the DUT as stated in the datasheet, the gate current is about 10 mA. Therefore, the gate current is extremely dependent on T_j, suffering from about three orders of magnitude increase in the operating range 25 °C – 150 °C. The gate current becomes even larger during the SC operation of the device, where significantly higher T_j are reached because

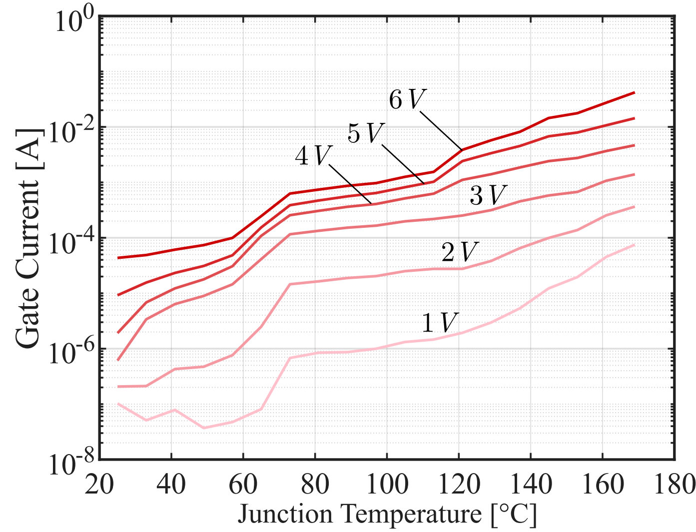


Fig. 4.8 Gate current dependence with T_j of the 650 V – 60 A GaN HEMT for positive values of V_{GS}.

of the huge instantaneous power dissipation, and so it can be a sensitive indicator of the SC event, since the fast increase of T_j is strictly linked to the fast increase of the gate leakage current.

4.3 Drain current model

The experimental results of drain I – V characterization on the DUT were used to derive a behavioral model for the drain current I_D as a function of V_{GS}, V_{DS} and T_j.

The manufacturer models the drain current using three equations, as described in section 1.2.5, defining the controlled current source and two variable resistances that simulate the access resistance of drain and source side of the device. Here, starting from the manufacturer model equation for the drain current and exploiting the experimental I – V characterization, an alternative unique and fully descriptive equation for the drain current is proposed. This equation incorporates the behavior of the GaN HEMT both in the linear and in the saturation regions without adding other equations or boundary conditions.

The general function used to fit the experimental data of drain current characterization is expressed by

$$I_D = \alpha(T_j) \cdot \beta(V_{GS}) \cdot \gamma(V_{GS}, V_{DS}) \cdot (1 + \delta V_{DS}) \tag{4.1}$$

where the functions $\alpha(T_j)$, $\beta(V_{GS})$ and $\gamma(V_{DS})$ are respectively:

$$\alpha(T_j) = I_0\left(a_1 - a_2(T_j - T_0)\right) \tag{4.2}$$

$$\beta(V_{GS}) = ln\left[1 + e^{b(V_{GS}-V_{th})}\right] \tag{4.3}$$

$$\gamma(V_{GS}, V_{DS}) = L_1 tanh(h_1 V_{DS}^3 + k_1 V_{DS}) + L_2 tanh(k_2 V_{DS}) \tag{4.4}$$

The function $\alpha(T_j)$ incorporates the thermal dependence of the drain current, while the function $\beta(V_{GS})$ is used to shape the transfer characteristic of the GaN HEMT, defining the dependence of I_D with V_{GS} and the threshold voltage V_{th}. Both the functions $\alpha(T_j)$ and $\beta(V_{GS})$, with their parameters, are taken from the manufacturer model [50], which exploits the behavioral model commonly used for HEMTs, merging equations like in [62] and MOSFETs equations [66], [75].

On the other hand, $\gamma(V_{GS}, V_{DS})$ is the proposed function used to achieve the best fit of the experimental data of the I – V characterization and integrate the manufacturer equations. It uses L_1, L_2, h_1, k_1, k_2 as the fitting parameters of the I – V curves for each V_{GS}. Finally, the term $1 + \delta V_{DS}$ is used to take into account the self-heating effect of the GaN HEMT, that is responsible of the reduction of the current in the saturation region. All the constant parameters used in (4.1), (4.2), and (4.3) are listed in Table 4.2.

Table 4.2 Constant parameters for the drain current model.

Drain Current Model		
Symbol	***Value***	***Unit***
I_0	0.105	A
T_0	25	°C
a_1	174.1	-
a_2	0.798	°C^{-1}
b	26.0	V^{-1}
V_{th}	1.61	V
δ	- 0.0004	V^{-1}

The fitting parameters of the function $\gamma(V_{GS}, V_{DS})$ are dependent on V_{GS} and they have been extracted using a MATLAB code implementing the Levenberg–Marquardt algorithm. Their values have been computed for five values of V_{GS}, from 2 V to 6 V in 1 V steps, according to the experimental data.

After obtaining the values of the parameters for each V_{GS}, they have been interpolated using the piecewise cubic hermite interpolating polynomial (PCHIP). Fig. 4.9 shows the

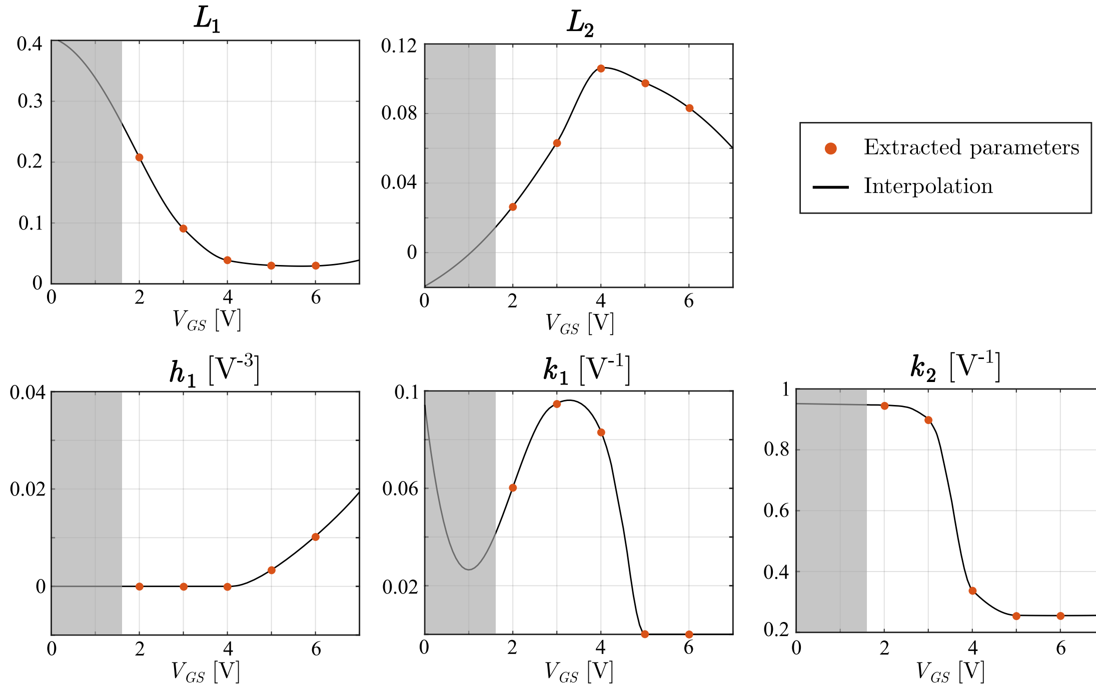


Fig. 4.9 Fitting parameters of function $\gamma(V_{GS}, V_{DS})$ for the drain current model. The red dots represent the values obtained from the fitting of the experimental data, while the black lines are the interpolation of the extracted data.

values of the fitting parameters at each tested V_{GS} and the related interpolation. The shaded grey region in the plots covers the values obtained by extrapolation for $V_{GS} \leq V_{th}$, since in that region the drain current is forced to be zero by the term $\beta(V_{GS})$. In fact, for $V_{GS} < V_{th}$ the term $ln\left[1 + e^{b(V_{GS}-V_{th})}\right]$ is practically equal to zero.

The proposed drain current model expressed by (4.1) has been compared to the experimental data and the manufacturer model, evaluated in the same conditions of the experimental tests. The comparison is shown in Fig. 4.10, where the dots represent the experimental values of the I – V characterization, the dash-dotted lines refer to the manufacturer model and the solid lines refer to the proposed one. A zoom of the linear region is also highlighted in Fig. 4.10 to underline that the proposed model can correctly represents the $r_{DS,on}$ of the GaN HEMT with a unique analytical expression.

The goodness of the model has been evaluated computing the residual errors with respect the experimental data, both for the manufacturer model and the proposed one. The plots of the residuals are shown in Fig. 4.11 for each V_{GS}. The maximum absolute errors E_{max} for each V_{GS} are also reported in Table 4.3, along with the maximum relative error e_r, computed as

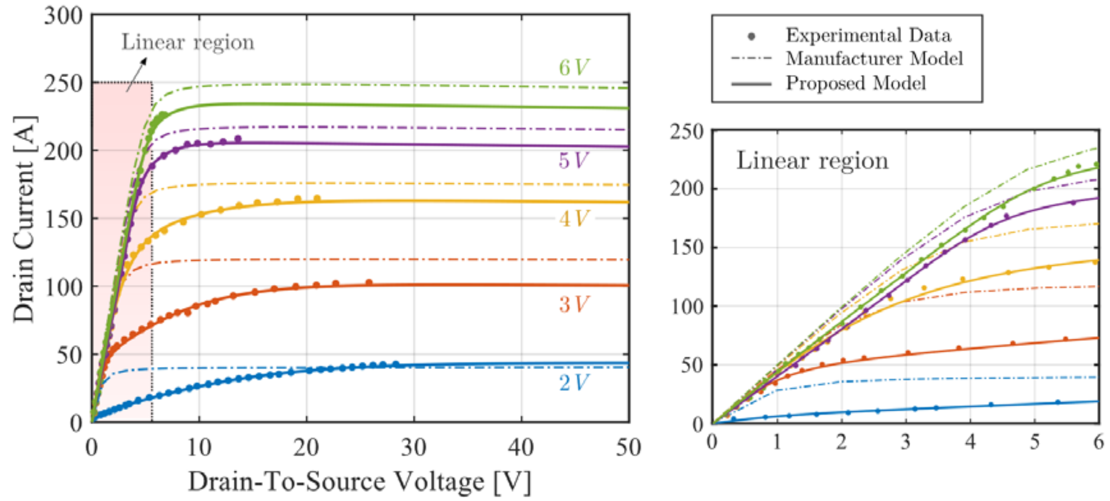


Fig. 4.10 Comparison of the proposed drain current model with the manufacturer one and the experimental data of the I – V characterization, with a detail of the I – V curves in the linear region.

$$e_r = \frac{(y_{exp} - y_m)_{max}}{y_{exp}} \cdot 100 \tag{4.5}$$

where y_{exp} and y_m represent the experimental data and the model values, respectively.

It is worth noting that the proposed model achieves high accuracy, with an error close to zero for all the cases plotted in Fig. 4.11, while the absolute error for the manufacturer model is higher than 20 A and even 40 A at $V_{GS} = 3$ V. Moreover, it can be obtained with the fitting of only six parameters (L_1, L_2, k_1, k_2, h_1, δ) since the other ones can be taken from the manufacturer SPICE model. This is a great advantage in terms of time-costs and complexity in comparison with other behavioral models such as [62], [64], [66], [120], [121] where the authors use more than 10 – 20 fitting parameters.

Table 4.3 Maximum absolute and relative errors of the manufacturer's and proposed models.

	Manufacturer model		**Proposed model**	
V_{GS} **[V]**	E_{max} **[A]**	e_r **[%]**	E_{max} **[A]**	e_r **[%]**
2	26.69	288.0	1.70	– 43.3
3	46.90	72.8	3.26	48.9
4	34.41	26.7	6.61	– 6.2
5	22.25	20.4	4.22	– 9.8
6	21.32	11.5	5.22	– 2.4

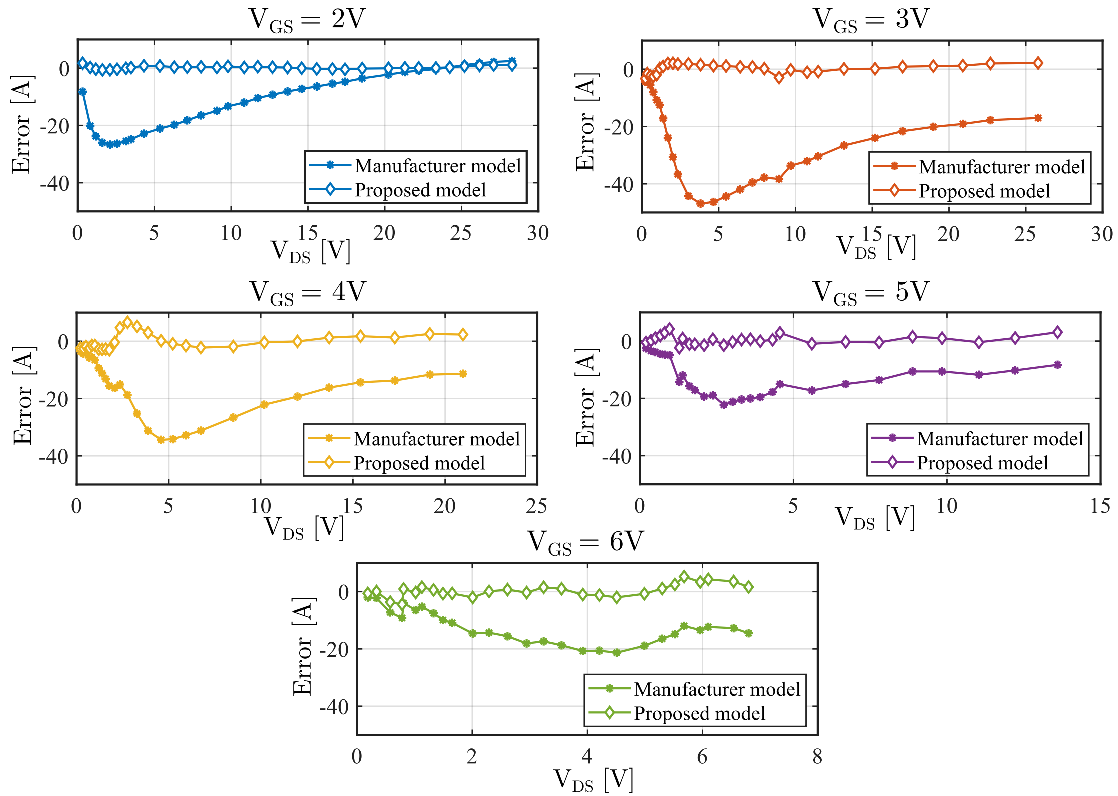


Fig. 4.11 Residuals plots for the manufacturer's and the proposed model for each tested V_{GS}.

Moreover, the proposed model can be easily integrated with the full manufacturer model in SPICE using look-up tables and therefore is suitable for the simulation of power converters.

To prove the consistence of the drain current model, (4.1) has been evaluated at V_{GS} different from the experimental data, using the interpolated fitting parameters of Fig. 4.9. The output curves obtained through the model for V_{GS} varying from 0.5 V to 6 V in 0.5 V steps are shown in Fig. 4.12 for two values of junction temperature, 25 °C and 150 °C. As highlighted in Fig. 4.12 (c) and (d), the values of $r_{DS,on}$ at 18 A and $V_{GS} = 6$ V are correctly determined by the proposed model for both the temperatures, as indicated in the datasheet. The model is therefore suitable for accurate simulation of the drain current of the 650 V – 60 A GaN HEMT both in the linear and in the saturation region.

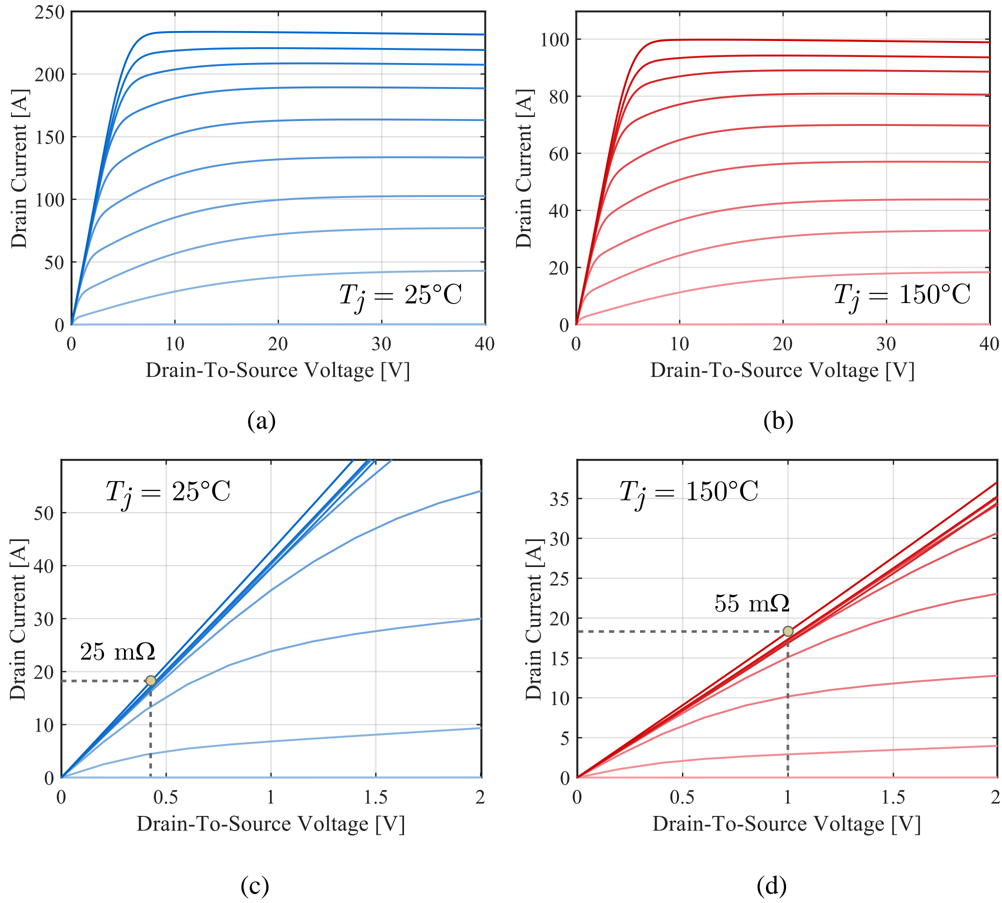


Fig. 4.12 Output I – V curves obtained with the proposed model from $V_{GS} = 0.5$ V to $V_{GS} = 6$ V in 0.5 V steps: (a) and (c) at $T_j = 25$ °C, (b) and (d) at $T_j = 150$ °C.

4.4 Gate current model

The experimental results of the gate current characterization have been used to derive a simple behavioral model for the gate leakage current $I_{G,Lk}$ for positive values of V_{GS}, depending on V_{GS} and T_j. A similar approach was presented in [122], where a different behavioral model is proposed and used to determine T_j during the operation of the GaN HEMT, though a few information about the fitting of the model are provided.

In the proposed approach, the curves of $I_{G,Lk}$ versus T_j, extrapolated from the experimental tests with the parameter analyzer and shown in Fig. 4.8, have been used to perform an exponential regression of the experimental data. Since the curves are obtained for six values of V_{GS}, from 1 V to 6 V in 1 V steps, if each curve is identified by the index $k = 1, \dots, 6$, referring to the specific V_{GS} at which the regression is applied, the exponential regression is expressed as

$$f_k(T_j) = I_{G0} \cdot e^{r_k(T_j)} \tag{4.6}$$

where I_{G0} is constant parameter, equal for all k values, and

$$r_k(T_j) = m_k T_j + q_k \tag{4.7}$$

is the equation used to fit the data in Fig. 4.8, since in logarithmic scale (4.6) becomes $ln(f_k(T_j)/I_{G0}) = r_k(T_j)$ and the experimental data show a quite linear trend in this scale. In this equation, m_k and q_k are the fitting parameters.

The trust-region algorithm was used to derive m_k and q_k for each k, implemented in MATLAB, and the obtained values of the fitting parameters are reported in Fig. 4.13. After noticing that the obtained values of m_k where very close to each other, a simplified exponential regression was computed considering a unique coefficient m for all the curves, computed as

$$m = \frac{1}{6}\sum_{k=1}^{6} m_k \tag{4.8}$$

The value of m is also plotted along the values m_k in Fig. 4.13 (a) to highlight that the latter approximation is acceptable.

The values of q_k incorporate the V_{GS} dependence and have been also interpolated using a rational function $q(V_{GS})$, expressed by

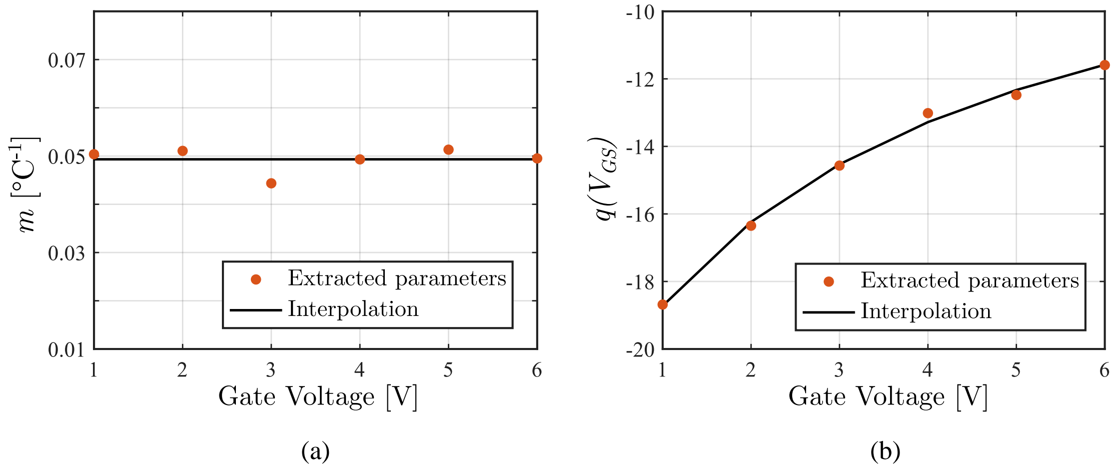


Fig. 4.13 Values of the parameters for the exponential regression of the gate leakage current and their related interpolation: (a) m_k and (b) q_k, for $k = 1, \ldots, 6$.

$$q(V_{GS}) = \frac{n_1 V_{GS} + n_2}{d_1 V_{GS} + d_2} \tag{4.9}$$

and the values of the coefficients q_k and their interpolation are shown in Fig. 4.13 (b).

Therefore, the final expression for the gate leakage current, incorporating both the T_j and the V_{GS} dependence, is

$$I_{G,Lk}\left(V_{GS}, T_j\right) = I_{G0} \cdot e^{mT_j + q(V_{GS})} \tag{4.10}$$

All the constant parameters used in (4.10) are listed in Table 4.4.

The proposed model for the gate leakage current has been compared to the experimental results of the gate I – V characterization to evaluate the goodness of the model. Fig. 4.14 shows the experimental data of $I_{G,Lk}$ versus T_j measured with 100 fA resolution, previously plotted in Fig. 4.8, with the related exponential regressions for each tested V_{GS}. The exponential regression without simplification, i.e. using the extracted values of m_k and q_k for each k, are represented with dash-dotted lines, while the simplified exponential regression, expressed according to (4.10), is represented with solid lines.

Table 4.4 Parameters of the gate current model.

Gate Current Model		
Symbol	***Value***	***Unit***
I_{G0}	10.0	nA
m	0.049	$°C^{-1}$
n_1	13.14	V^{-1}
n_2	-14.46	-
d_1	1.0	V^{-1}
d_2	3.41	-

As visible in Fig. 4.14, the simplification coming from using the same coefficient m for all the curves does not strongly affect the regression of the data, except for the case of $V_{GS} = 3$ V, where the error is larger.

To provide a thorough analysis of the accuracy for the proposed model, the residuals have been computed and plotted in Fig. 4.15, expressing the error between the experimental data and the modeled data. The proposed model is quite accurate for T_j up to 150 °C, especially for V_{GS} lower than 5 V, where the error is lower than 500 µA, while it is less accurate for V_{GS} between 5 V and 6 V, although the error is still lower than 2 mA.

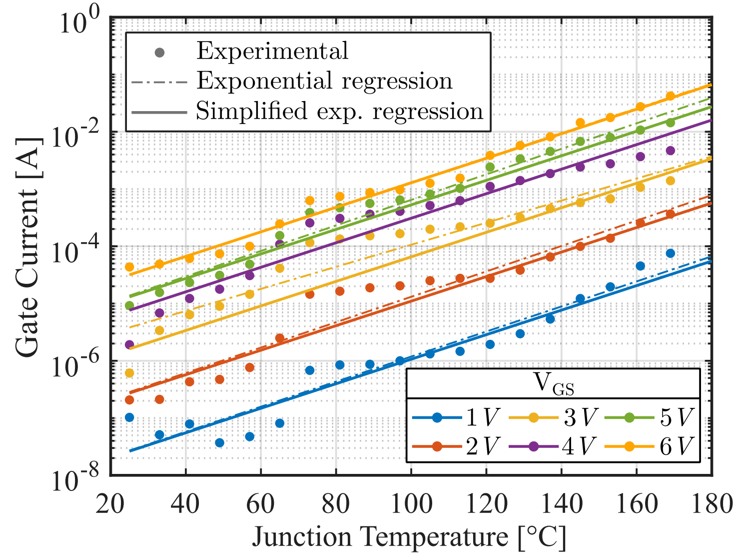


Fig. 4.14 Comparison among the experimental data of the gate current versus T_j (dots), exponential regression (dash-dotted lines) and simplified exponential regression used to derive the gate current model (solid lines).

For T_j higher than 150 °C, that is also the maximum operating temperature indicated by the manufacturer, the accuracy is lower and the maximum error is less than 3 mA for V_{GS} equal to 4 V and 5 V, and is less than 5 mA at 6 V. However, even if the impact of the error on $I_{G,Lk}$ is higher at high T_j and V_{GS}, the model can still predict the gate leakage current in those conditions. Moreover, for V_{GS} equal to 3-, 4- and 5- V, the model overestimates the current and therefore it defines an upper limit for the determination of the gate leakage current. On the contrary, at $V_{GS} = 6$ V, the gate leakage current is underestimated by the model of about 15 %.

During the nominal operation of the GaN HEMT V_{GS} is often set to 5 V or 6 V and T_j is commonly lower than 100 °C. In these conditions the model shows the best accuracy and, since it is based on a straightforward relation between $I_{G,Lk}$ and T_j, it could be used as a mathematical tool for the online measurement of the device junction temperature through the sensing of the gate current, as initially proposed in [122]. In addition, in SC conditions, where T_j reaches values higher than 150 °C, the model is able to take into account the huge increment of the gate leakage current and allows to determine its impact on the behavior of the GaN HEMT under SC.

As for the drain current model, the maximum absolute and relative errors, E_{max} and e_r, for each V_{GS} are also reported in Table 4.5.

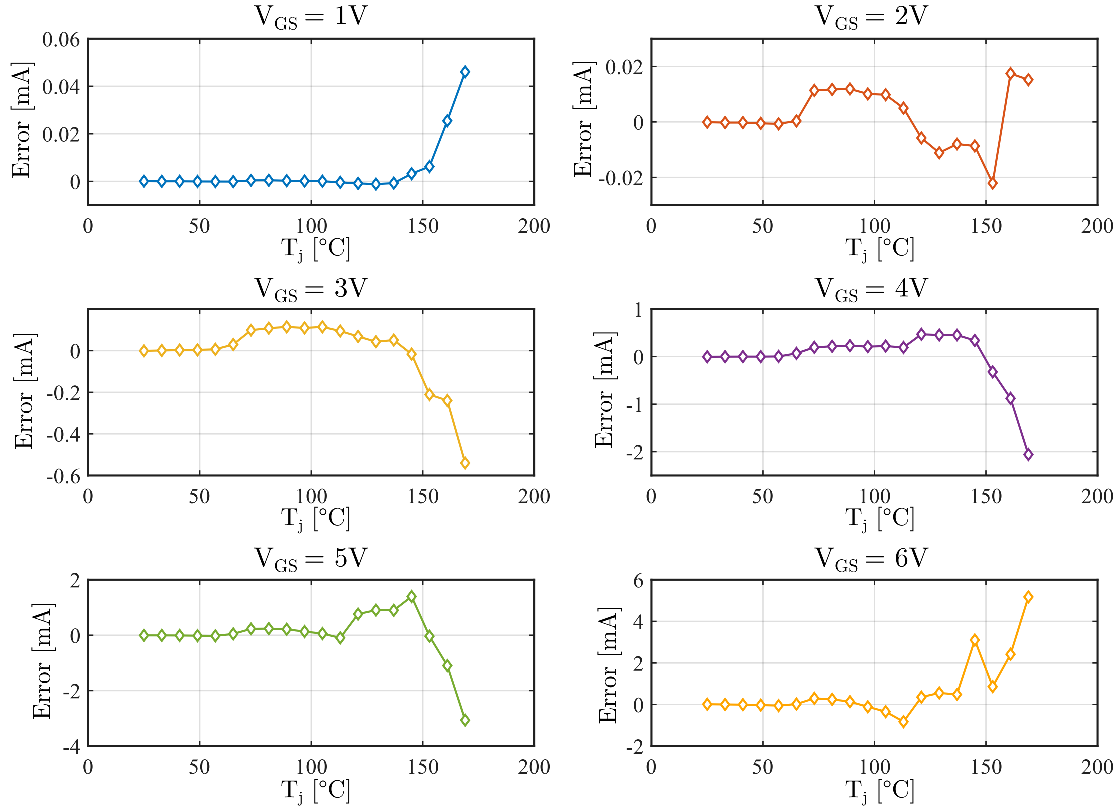


Fig. 4.15 Residuals plots for the proposed model for each tested V_{GS}.

Table 4.5 Maximum absolute and relative errors of the proposed gate current model.

V_{GS} [V]	E_{max} [mA]	e_r [%]
1	0.05	-61.2
2	0.02	16.0
3	0.54	38.7
4	2.06	44.0
5	3.06	21.3
6	5.17	-12.3

4.5 Equivalent model of the GaN HEMT

The obtained drain (4.1) and gate (4.10) equations are used to derive an equivalent model of the GaN HEMT, applicable also in SC conditions. This model can be expressed as a set of analytical equations and incorporated in a circuit-level simulation, for instance in a SPICE-based software. It is also possible to implement the whole model in softwares

such as Simulink and PLECS after defining the dependence of the device electrical parameters (V_{GS}, I_G, V_{DS}, I_D) with the circuit.

The block scheme of Fig. 4.16 represents this equivalent analytical model and includes the thermal network, which is based on manufacturer's Cauer model. Each block represents the analytical function that has to be applied to the input parameters to determine the output quantity. The functions f_2 and f_3 are represented by the gate leakage equation (4.10) and the drain current equation (4.1), while $f_{1,1}$ and $f_{1,2}$ represent the gate circuit equations that determine the whole gate current I_G and voltage. They are obtained writing the circuit equations in the gate path as

$$f_{1,1}: \qquad I_G = \frac{1}{L_G} \int (V_{GG} - V_{GS} - R_G I_G)\, dt \tag{4.11}$$

$$f_{1,2}: \qquad V_{GS} = \frac{1}{C_{iss}} \int \left(I_G - I_{G,Lk}\right) dt \tag{4.12}$$

where V_{GG}, R_G and L_G are the gate driver voltage, the gate resistance and the stray inductance of the gate path, respectively, while C_{iss} is the input capacitance of the GaN HEMT, that is non-linear and dependent on V_{GS} and V_{DS}.

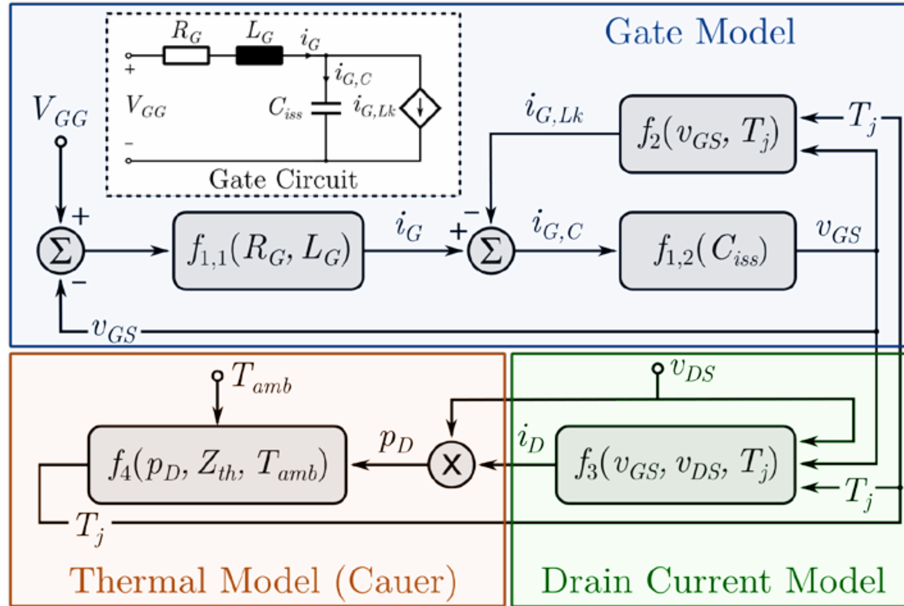


Fig. 4.16 Block scheme of the proposed model for the GaN HEMT, including gate circuit equations and Cauer thermal model.

The function f_4 is based on the Cauer thermal model of the GaN HEMT provided by the manufacturer and computes the junction temperature T_j starting from the thermal impedance Z_{th} of the device, the ambient temperature T_{amb} and the instantaneous power dissipation $P_D = V_{DS}I_D$, neglecting the power losses on the gate. The thermal equation can be easily expressed in Laplace domain as

$$T_j(s) = Z_{th}(s)P_D(s) + T_{amb} \tag{4.13}$$

The whole model of Fig. 4.16 has been implemented both in Simulink and in LTSpice. However, the Simulink implementation requires the definition of other "boundary" conditions, depending on the circuit connections of drain and source pins of the device with the rest of the circuit. For example, in the case of the SC of a HB, two models as the one of Fig. 4.16 should be implemented and connected together with a further equation derived from the power circuit, that can be expressed by

$$I_D = \frac{1}{L_p}\int \left(V_{dc} - V_{DS,1} - V_{DS,2} - R_p I_D\right) dt \tag{4.14}$$

where R_p and L_p are the parasitic resistance and inductance on the power loop and $V_{DS,1}$, $V_{DS,2}$ are the drain-source voltage of the two devices. This fact makes less convenient the use of Simulink to implement the proposed model, since any change in the circuit requires the add or modifications of the equations.

For that reason, the drain and gate current models have been implemented in LTSpice by simply modifying the manufacturer's library of the 650 V – 60 A GaN HEMT. The resulting equivalent circuit of the device after the modifications is shown in Fig. 4.17. In comparison with the manufacturer model, the controllable current source defined by $I_{G,Lk}$ was added between the internal gate and source contacts to model the gate leakage current. Moreover, the current source I_D is replaced by the drain current equation defined by (4.1), that also incorporates the variable behavior of $r_{DS,on}$. Therefore, R_D and R_S shown in Fig. 4.17 simply represent parasitic resistances on the drain and source contacts. The parasitic inductances and the capacitance models are the same of those defined by the manufacturer.

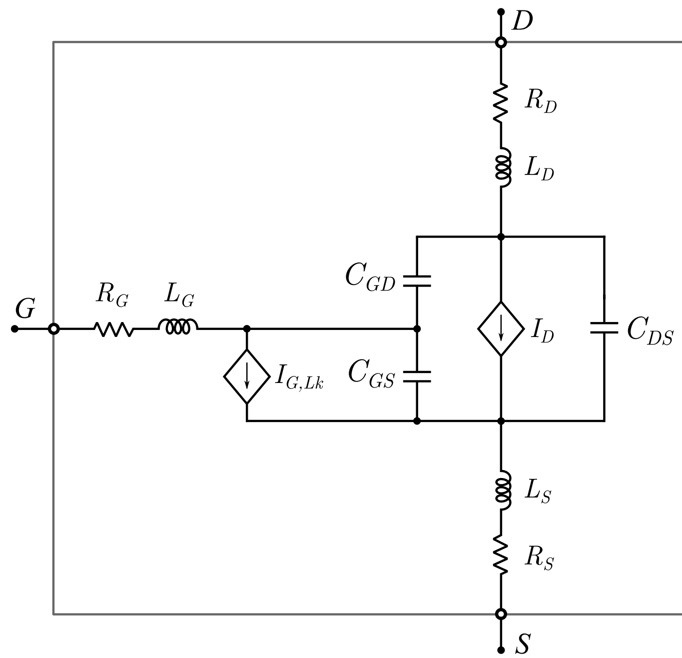


Fig. 4.17 Equivalent circuit scheme of the 650 V – 60 A GaN HEMT with the added drain and gate current equations.

5

Experimental Short Circuit tests and model validation

Non-destructive Short Circuit (SC) tests are conducted at different DC-link voltages and for two values of gate resistances, showing quite different results. The SC energy and an estimation of the junction temperature are also provided. The validation of the proposed model for the 650 V – 60 A GaN HEMT is performed comparing the LTSpice simulations with the manufacturer model and the experimental results. The capability of the model to predict the SC behavior is discussed and a junction temperature estimation method is proposed, starting from the gate leakage current model.

5.1 Setup description for Short Circuit tests

The SC tests have been performed using the constructed Half Bridge (HB) prototype, described in Chapter 3. The instrumentation adopted for the tests consists of:

- a 8 kV – 150 mA high-voltage power supply;
- a 30 V – 2 A isolated power supply;
- a 4 channel – 1 GHz HDO6104-MS high-definition oscilloscope with 2.5 GS/s sample rate;
- one 1500 V – 120 MHz HVD3106 differential probes;
- three 500 V – 500 MHz PP022-1 voltage passive probe;
- one Rogowski current transducer with 20.0 mV/A sensitivity;

- a Cyclone II FPGA board for the generation of the driver input signals.

All the tests were executed according to the logic driving signals shown in Fig. 5.1, which also depicts the equivalent circuit of the constructed HB prototype, also used for the simulations and already presented in Chapter 2 and reported here for completeness. First, device Q_1 turns on applying the DC-link voltage to Q_2 and, after 4 µs device Q_2 turns on, creating the SC on the HB with a 5 µs pulse-width. In this condition, Q_2 experiences a type I SC, while Q_1 undergoes a type II SC, where the load current is zero.

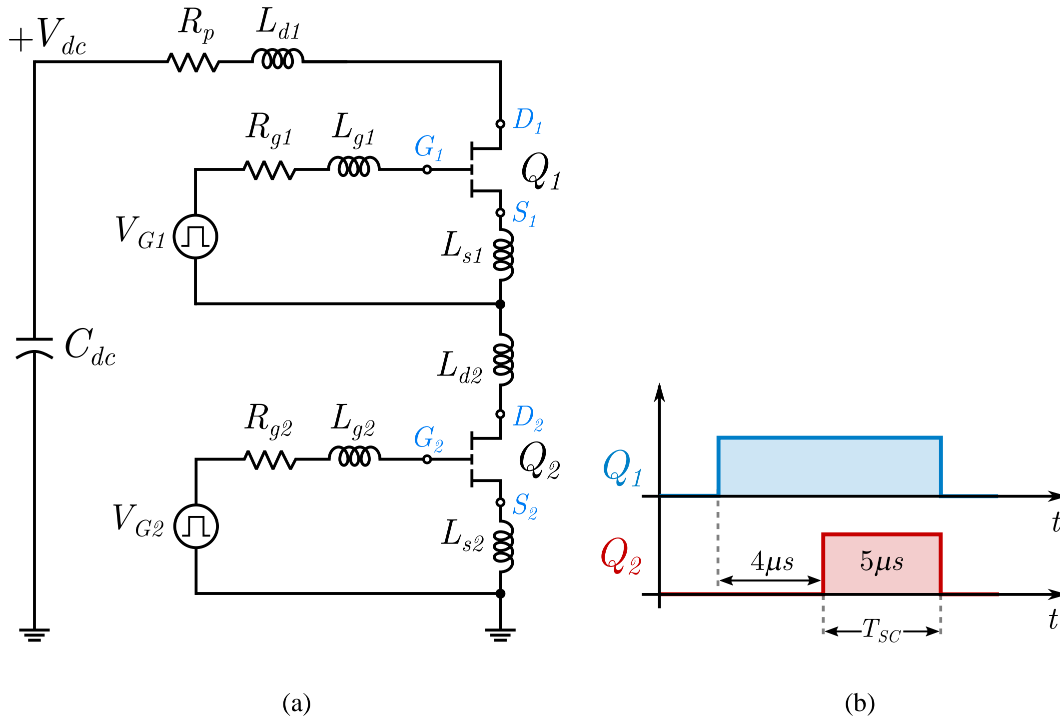


Fig. 5.1 Circuit used in simulation based on the real prototype board (a) and driving signals for the SC tests (b).

The stray components of the circuit of Fig. 5.1 have been placed according to their real distribution in the PCB and their values have been measured with a vector network analyzer and reported in Table 5.1.

The DC-link voltage V_{dc} was varied from 50 V to 400 V in 50 V steps, while the gate driver voltage V_G was set to 5 V. In this case, the 5 V driving voltage is preferred in order to avoid the possible failure of the device at high V_{dc} with the recommended 6 V driving voltage, which has been proven to happen in less than 1 µs. Anyway, this condition is also suitable for practical applications, thanks to the low threshold voltage of the GaN HEMT

that is about 1.6 V for the 650 V – 60 A device and the slight increase of the on-resistance with respect $V_{GS} = 6$ V, that remains acceptable.

Table 5.1 Measured values of the stray components of the HB prototype, used also for the simulations.

Parameter	Value
L_{d1}, L_{d2}	3.0 nH
R_p	10.0 mΩ
L_{s1}	0.8 nH
L_{s2}	1.2 nH
L_{g1}, L_{g2}	1.0 nH

The SC tests have been performed in the conditions described above for two values of gate resistance, namely 100 Ω and 22 Ω. In the majority of the experimental SC tests presented in the literature, large gate resistors are used to slow down the switching transients and avoid turn-off oscillations or even instabilities during the SC event (cf. 1.5). This condition has no impact on the hard switching fault-SC of the single device, but it may affect the SC behavior of the HB, and for this reason two very different values of gate resistance are used. Moreover, the 22 Ω-resistance has practical usefulness when working with GaN in normal operations, at the opposite of the 100 Ω resistance, that makes no practical sense at all.

5.2 Results with 100 Ω gate resistance

The following waveforms have been measured during the SC tests: the SC current I_{SC} (also identified as the drain current I_D in the following), the gate-source voltage V_{GS} of device Q_2, the drain-source voltage of both devices and the DC-link voltage V_{dc}. The results of the experimental tests using 100 Ω gate resistors are shown in Fig. 5.2 and Fig. 5.3, at different V_{dc} values.

The drain current waveform shows the typical behavior during the SC, reaching a peak value in about 900 ns and then decreasing to lower values because of the increase of junction temperature. In particular, the current reaches a peak of 173 A and then decreases to about 125 A at $V_{dc} = 50$ V. As V_{dc} increases, the peak of the SC current slightly decreases to about 166 A, while its final value undergoes a huge drop, that becomes larger with increasing V_{dc}. At $V_{dc} = 400$ V the peak SC current is about 160 A and it is reduced by 70% after 2 μs, becoming equal to about 50 A. At the end of the SC, the final value is 35 A, indicating that the current decreased by 80% with respect the initial value.

The effect of increasing V_{dc} is clearly visible also in the V_{GS} waveforms of device Q_2, shown in Fig. 5.2 (b). At $V_{dc} = 50$ V, V_{GS} reaches the 5.0 V imposed by the gate driver and then slightly decreases, indicating a weak increment of the gate leakage current. As V_{dc}, and consequently T_j, increases, the effect of the gate leakage current becomes prominent in determining both the peak value of V_{GS} and its reduction during the SC event.

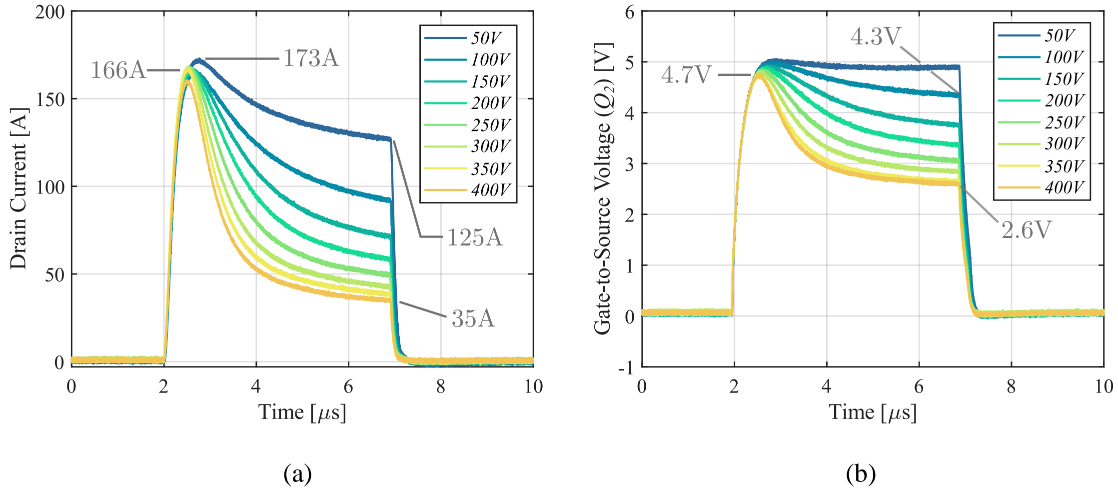


Fig. 5.2 Experimental waveforms of drain current and gate-source voltage of device Q_2 during the SC tests, for a V_{dc} variation from 50 V to 400 V in the conditions $V_G = 5$ V, $R_g = 100\ \Omega$.

At $V_{dc} = 100$ V V_{GS} still starts from 5.0 V, but then decreases to 4.3 V. When V_{dc} is increased to 400 V, the presence of the leakage current reduces the peak value of V_{GS} from the expected 5.0 V to 4.7 V and at the end of the SC pulse-width V_{GS} collapses to 2.6 V, that is about the 50% of the nominal gate voltage. From the voltage drop on V_{GS} of device Q_2 it is possible to perform an estimation of the final value of the gate leakage current as $\Delta V_{GS}/R_G$, obtaining a minimum of 1.2 mA at 50 V and a maximum value of 24 mA at 400 V.

The drain-source voltages V_{DS1} and V_{DS2} of devices Q_1 and Q_2, respectively, and the DC-link voltage are shown in Fig. 5.3. They are indicative of the roles played by the two devices during the SC event, but before proceeding with the discussion, it must be clarified that the drain-source voltage of Q_1 (V_{DS1}) was not directly measured during the tests, but it was obtained from the voltage balance in the output mesh as $V_{dc} - V_{DS2} - L_p dI_D/dt$, where L_p is the total parasitic inductance in the power path. The contribution of L_p has been numerically included during the computation of V_{DS1} and although this fact causes some numerical errors when evaluating V_{DS1}, especially at the turn-on and turn-off

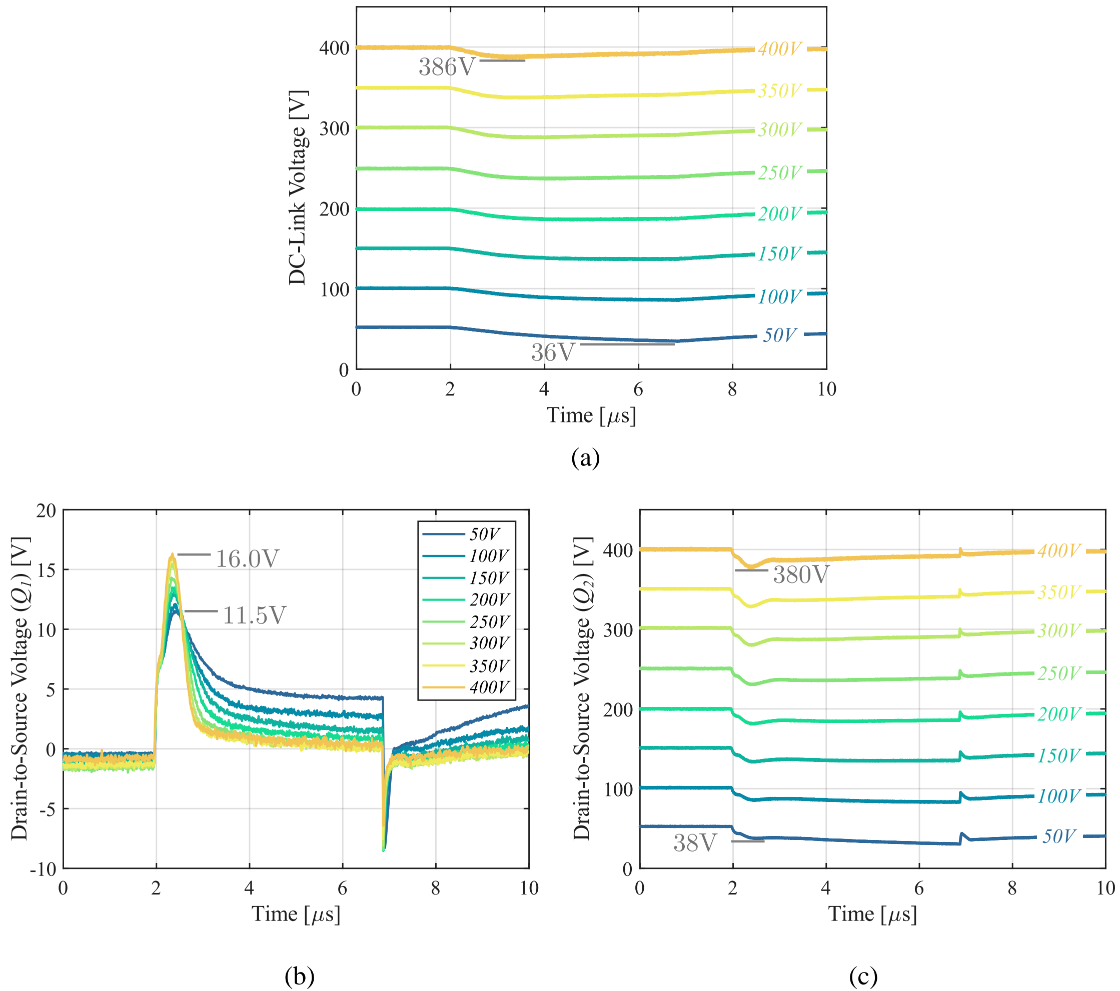


Fig. 5.3 Experimental waveforms of DC-link voltage (a) and drain voltages (b), (c) during the SC tests, for a V_{dc} variation from 50 V to 400 V in the conditions $V_G = 5$ V, $R_g = 100\ \Omega$.

transients, the waveform of V_{DS1} during the SC event is reliable and can be used to evaluate the SC behavior of the device.

As shown in Fig. 5.3 (a), V_{dc} has a voltage drop when the SC starts, but it remains in the expected range as defined in the design section in Chapter 3, where a maximum 15 V voltage drop was assigned. Almost all the DC-link voltage is applied to Q_2, that works in the saturation region for all the SC duration. On the contrary, Q_1 starts from 0 V and in 1 µs reaches a peak value, that increases with V_{dc} but remains between 11.5 V and 16.0 V. After that, its value decreases to less than 5 V and at $V_{dc} = 400$ V it goes to about 0.3 V (see Fig. 5.3 (b)). In correspondence of the peak value of V_{DS1}, V_{DS2} experiences the largest voltage drop, reaching 380 V and 38 V in the extreme cases of $V_{dc} = 400$ V and

V_{dc} = 50 V, respectively (see Fig. 5.3 (c)). Therefore, the behavior of the two devices complies with the theoretical analysis introduced in Chapter 2. In fact, Q_2 works in the saturation region and Q_1, after a transient working point in the saturation region operates in its linear region.

5.2.1 Energy and temperature estimation

To better investigate the electro-thermal stress caused by the two GaN HEMTs during the SC event, the instantaneous power dissipations have been computed for both of them as the product between their V_{DS} and the drain current I_D, that is the same for the two devices. Fig. 5.4 shows the graphs of the instantaneous power of the two devices versus time.

As clearly visible, the amounts of dissipated power are very different between the two devices. Q_1 has a peak power dissipation that varies between 1.8 kW and 2.5 kW and after 2 μs quickly decreases to less than 500 W. As V_{dc} increases, since Q_1 operates more and more in its linear region the width of the power pulse decreases, thus reducing the mean power dissipation and so the SC energy. The opposite happens to device Q_2, which endures a much higher power that increases with V_{dc}. Its peak power is 6.6 kW at V_{dc} = 50 V and increases by about 7.5 kW at each V_{dc} voltage step, up to 60 kW at 400 V. After the initial peak, the reduction of the current fosters the decrease of the instantaneous power during the SC, enhancing the capability of the GaN HEMT to survive the SC. In

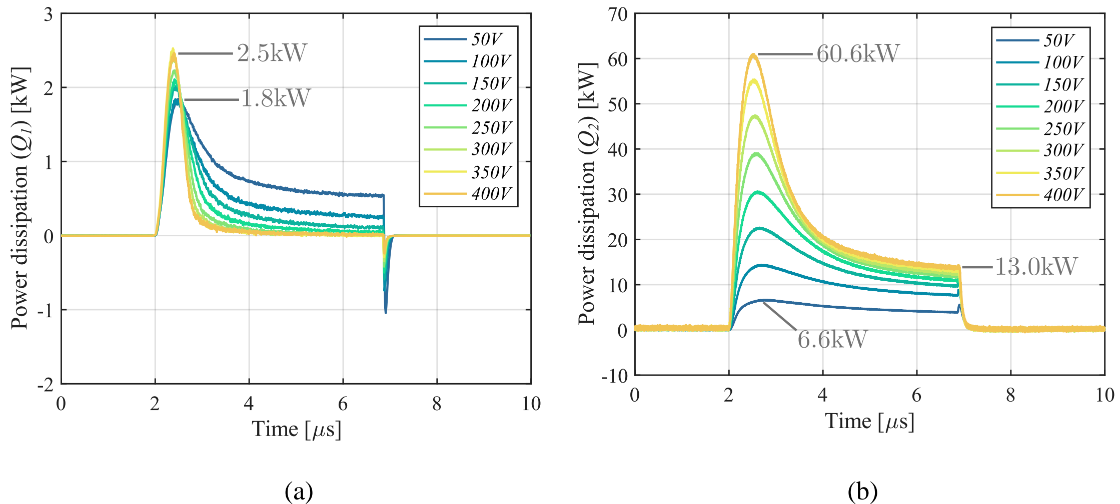


Fig. 5.4 Instantaneous power dissipation of device Q_1 (a) and Q_2 (b), computed from the measured experimental waveforms. V_{dc} varies from 50 V to 400 V in the conditions V_G = 5 V, R_g = 100 Ω.

fact, at the end of the SC the power decreases by about 80% from its peak value to 13.0 kW at $V_{dc} = 400$ V.

From the instantaneous power dissipation, the SC energy E_{SC} for the two devices has also been derived, computed at each V_{dc} as

$$E_{SC}^{k} = \int_{t_i}^{t_f} P_k(t)\, dt \tag{5.1}$$

where $k = 1, 2$ identifies device Q_1 or Q_2, respectively, $P_k(t)$ is the instantaneous power dissipation and t_i, t_f are the initial and final instants of the SC event, respectively. According to the test conditions, $t_i = 2$ μs and $t_f = 7$ μs. The computed SC energies are plotted in Fig. 5.5 as a function of V_{dc}. The results give a sensitive representation of the difference between the electrical stress of the two devices, that show a noticeable different behavior during the SC, as already expected from the theoretical analysis. At all the tested DC-link voltages device Q_2 shows the largest energy dissipation, that goes from 24 mJ at 50 V up to 121 mJ at 400 V, while the energy related to device Q_1 is between 4 mJ and 1 mJ, decreasing with V_{dc}. Even if much lower than the amount of energy dissipated by Q_2, its value is still noticeable if compared to the energy loss during the normal switching operations, that is in the order of 100 μJ [50].

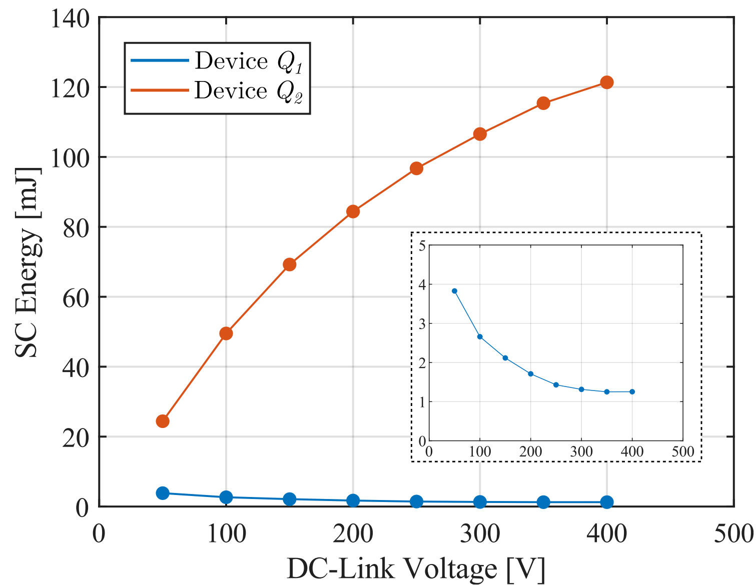


Fig. 5.5 Short Circuit energy of device Q_1 and Q_2 versus V_{dc} in the conditions $V_G = 5$ V, $R_g = 100\ \Omega$.

To understand the impact of such high energy dissipation on the devices their junction temperatures (T_j) have been estimated using the thermal model provided by the manufacturer. For this purpose, the thermal model of the GaN HEMT was implemented in Simulink by computing the equivalent transfer function between junction and case, according to the Cauer model presented in section 1.4.5. The computed data of the instantaneous power dissipation obtained from the experimental tests were given as inputs to the Simulink model, that provided the junction temperatures of the two devices as output.

The obtained estimation for the two junction temperatures, considering an ambient temperature of 25 °C, is shown in Fig. 5.6. The thermal stress of device Q_1 is negligible, as its junction temperature reaches a maximum value of 32 °C. On the other hand, device Q_2 undergoes a strong thermal stress and its T_j overcomes the maximum limit of 150 °C, highlighted in Fig. 5.6 (b), for all the values of V_{dc} higher than 150 V. The temperature reaches its peak value of 267 °C at $V_{dc} = 400$ V, right after the peak power dissipation, and then decreases to 205 °C before the end of the SC, due to the sudden decrease of the power dissipation. For V_{dc} greater than 150 V the trend is practically the same, but for lower values, since the power dissipation reduces more slowly, T_j reaches the maximum value at the end of the SC, as highlighted at $V_{dc} = 50$ V where it reaches 68 °C.

The temperature estimation could be also performed considering the transient thermal impedance characteristic defined in the datasheet and computing the mean power dissipation. However, this could lead to a different result because of the different response of the thermal impedance to a step power pulse with respect the real impulsive power of

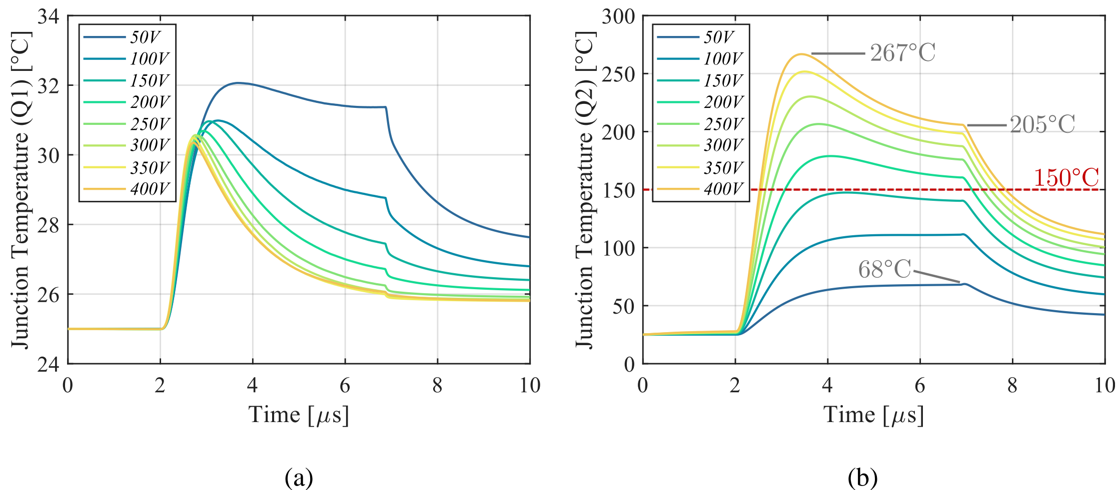


Fig. 5.6 Junction temperature estimation of device Q_1 (a) and Q_2 (b) using the manufacturer's Cauer thermal model. V_{dc} varies from 50 V to 400 V in the conditions $V_G = 5$ V, $R_g = 100\ \Omega$.

Fig. 5.4 (b). For instance, considering the condition $V_{dc} = 400$ V, the mean power dissipation during the SC is $P_m = 24$ kW, computed as the SC energy at 400 V (≈ 120 mJ) divided by the SC pulse-width (5 µs). The nominal DC thermal impedance for the 650 V – 60 A GaN HEMT is $R_\theta = 0.27$ °C/W, while the correction factor for a single pulse with a duration of 5 µs is $k_{n\theta} = 0.04$. Both the values are taken from the datasheet.

Therefore, the junction temperature at the end of the SC can be estimated by the expression

$$T_j = T_{amb} + k_{n\theta} R_\theta P_m \tag{5.2}$$

obtaining $T_j = 284$ °C when $T_{amb} = 25$ °C. In the real case, however, the real junction temperature is 205 °C at the end of the SC and even its maximum value (267 °C) is overestimated by about 20 °C.

5.3 Results with 22 Ω gate resistance

A 22 Ω gate resistance for both the devices have been used to investigate the possible effects on the SC behavior of the Half Bridge. Two 650 V – 60 A GaN HEMTs, different from those previously employed, have been used for this test in order to avoid any possible corruption of the results due to degradation effects. The tests have been performed under the same conditions as the previous case with 100 Ω resistor, i.e. $V_G = 5$ V and V_{dc} varied from 50 V to 400 V in 50 V steps. The main waveforms measured during the tests are

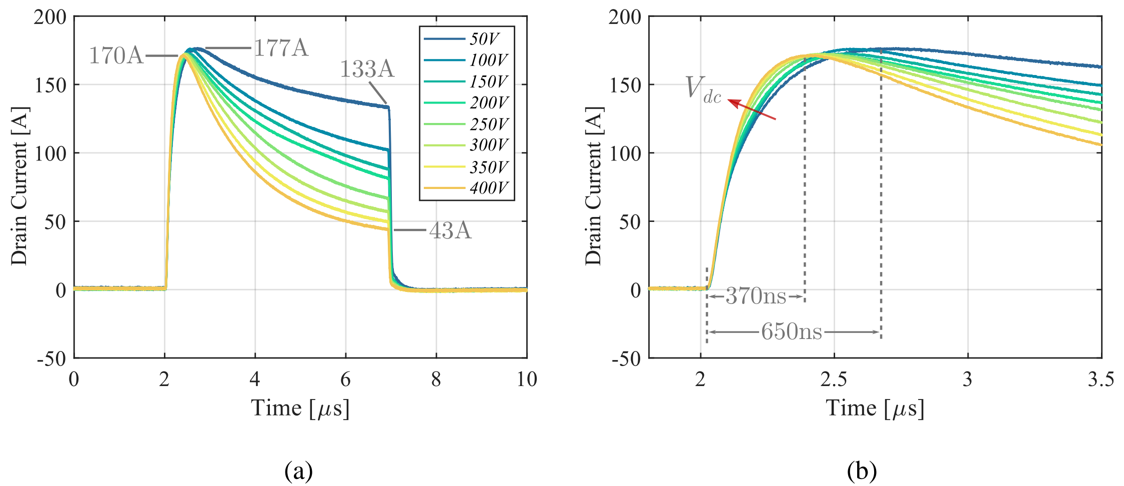


Fig. 5.7 Experimental waveforms of drain current during the SC tests, for a V_{dc} variation from 50 V to 400 V in the conditions $V_G = 5$ V, $R_g = 22$ Ω.

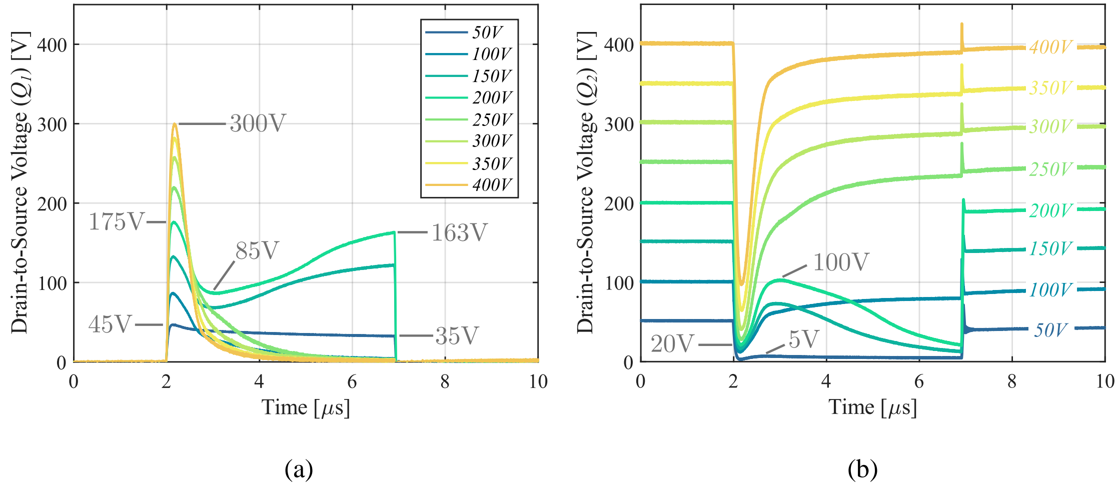


Fig. 5.8 Experimental waveforms of drain voltage of device Q_1 (a) and Q_2 (b) during the SC tests, for a V_{dc} variation from 50 V to 400 V in the conditions $V_G = 5$ V, $R_g = 22$ Ω.

shown in Fig. 5.7, Fig. 5.8 and Fig. 5.9, where the V_{dc} waveforms are not reported, since they are equal to the previous case.

The drain current reaches a peak value of about 177 A at $V_{dc} = 50$ V and then it slightly decreases with the increase of V_{dc}, up to 170 A at 400 V. As visible in the zoomed region of Fig. 5.7 (b), the slope of the current depends on V_{dc} and increases with it. The lower gate resistance shortens the rise time of I_D, that goes from about 650 ns to 370 ns at 50 V and 400 V, respectively, while it was 750 ns and 500 ns with 100 Ω gate resistor for the same V_{dc}. Instead, the I_D value at the end of the SC reaches 133 A at $V_{dc} = 50$ V and 43 A at $V_{dc} = 400$ V, that represent a drop of the 25% and 75% with respect the peak value, respectively. These final values of I_D are quite higher than the final values in the previous case. Assuming the same thermal impedance for the devices in the two tests, this may indicate that also the reduction of V_{GS} can play a role in determining the reduction of the current during the SC, that has a major impact when using a large gate resistance.

Looking at the drain voltage waveforms of the two devices in Fig. 5.8 it can be noted that the behavior of Q_1 and Q_2 is very different in this case. For $V_{dc} \leq 200$ V, except for $V_{dc} = 100$ V, Q_1 blocks a higher voltage than Q_2, even if, from a theoretical point of view, Q_2 should block a higher percentage of V_{dc}. In fact, at $V_{dc} = 50$ V V_{DS1} reaches 45 V and then decreases to 35 V, because V_{dc} also decreases, while V_{DS2} remains at about 4.5 V. This means that the roles of the two devices are swapped and Q_1 operates in the saturation region, while Q_2 is in its linear region. The behavior is inverted at $V_{dc} = 100$ V, where Q_2 blocks almost all V_{dc}.

However, at 150 V and 200 V, both Q_1 and Q_2 operate at high V_{DS} for a long period of the SC event. In fact, at $V_{dc} = 200$ V, V_{DS1} shows a peak of 175 V, then has a drop to 85 V and then increases again up to 163 V. V_{DS2} shows the opposite behavior, with a drop from 200 V to 20 V at the beginning of the SC, a consequent increase up to 100 V and, then, a further reduction to 20 V at the end of the SC.

For V_{dc} higher than 200 V, the two devices return to operate as expected, with Q_2 blocking almost all V_{dc} for a large part of the SC pulse-width. However, it is worth noting a strong voltage dip in V_{DS2} at the beginning of the SC, caused by the high *di/dt*, that is responsible also for the transient increase of V_{DS1}.

The difference in the behavior of the two devices is also visible in the gate voltage waveforms, shown in Fig. 5.9. Another oscilloscope, synchronized with the main one was used to measure V_{GS1}, which is reported in Fig. 5.9 (a) in a larger time window but with the same time reference. In correspondence of the rising edge of the SC current, at $t = 2$ µs, V_{GS1} has a voltage drop that becomes deeper with V_{dc}, up to 3 V. For V_{dc} equal to 50-, 150- and 200-V the gate voltage of Q_1 undergoes a reduction because of the increase of its T_j, as it is under the SC electro-thermal stress and it reduces to 4.5 V at $V_{dc} = 200$ V. On the contrary, Q_2 has a much lower reduction of V_{GS2}, that starts from 5.2 V and reaches 5.0 V at $V_{dc} = 50$ V. The voltage drop of V_{GS2}, depending on the gate leakage current, that in turns depend on T_j, follows the electrical stress on the device: in fact, considering $V_{dc} = 200$ V, V_{GS2} decreases to 4.8 V in the middle of the SC event, when its drain voltage shows the highest value, and then increases again to 5.0 V when V_{DS2} decreases.

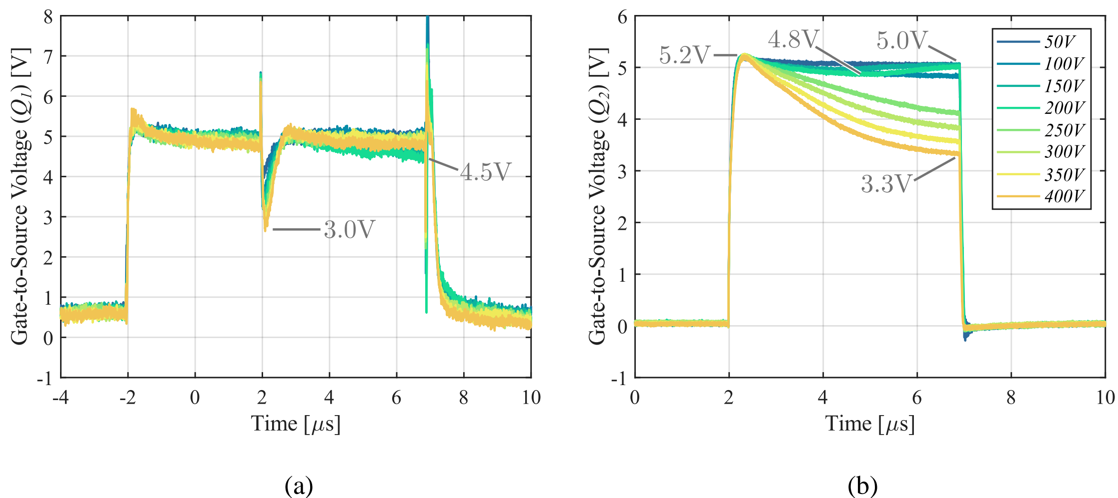


Fig. 5.9 Experimental waveforms of gate voltage of device Q_1 (a) and Q_2 (b) during the SC tests, for a V_{dc} variation from 50 V to 400 V in the conditions $V_G = 5$ V, $R_g = 22\ \Omega$.

For V_{dc} higher than 200 V, the reduction of V_{GS} is only noticeable in device Q_2 and increases with V_{dc}, reaching 3.3 V at $V_{dc} = 400$ V, that means a reduction of about 40% with respect the peak value. The estimated gate leakage current at $V_{dc} = 400$ V is 84 mA, that is much higher than the estimated leakage current for the case $R_g = 100\ \Omega$, equal to 24 mA. This indicates that the temperature reached in device Q_2 is higher than in the previous case.

As already discussed in 2.2.5, the different parasitic inductance on the source of the two devices leads to the described behavior and its impact is increased by the fast switching transition imposed by the lower gate resistance. In this condition the two GaN HEMTs act like a "bistable" system: depending on the operating conditions and the evolution of V_{GS} and T_j, each device can operate in saturation or in linear region, independently from the conditions before the SC event. For example, at $V_{dc} = 100$ V the gate voltages of the two devices are equal at the beginning of the SC, but then the transient decrease of V_{GS2} brings Q_2 to operate in the saturation region, blocking a higher voltage. The high V_{DS2} across Q_2 makes T_j and the gate leakage current increase, causing the further decrease of V_{GS2}. This positive feedback mechanism leads Q_2 to operate more and more in saturation, while Q_1 works in its linear region.

5.3.1 Energy and temperature estimation

As in the previous case, the instantaneous power dissipation of each device has been computed and used to obtain both their SC energy and an estimation of their junction temperatures. The waveforms of the instantaneous power dissipation are depicted in Fig. 5.10.

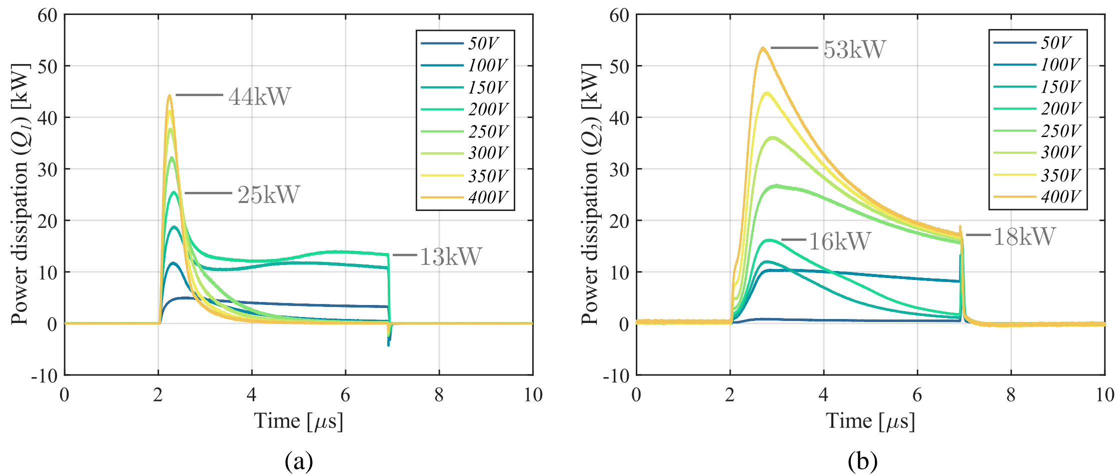


Fig. 5.10 Instantaneous power dissipation of device Q_1 (a) and Q_2 (b), computed from the measured experimental waveforms. V_{dc} varies from 50 V to 400 V in the conditions $V_G = 5$ V, $R_g = 22\ \Omega$.

Compared to the case of $R_g = 100\ \Omega$ the peak power dissipation of device Q_1 has increased to much higher values, becoming comparable to the power dissipation of device Q_2. They reach 44 kW and 53 kW at $V_{dc} = 400$ V, respectively, but then P_{D1} decreases to almost zero in 2 µs, while P_{D2} decreases to 18 kW at the end of the SC. For V_{dc} lower than 200 V, however, the power dissipation is higher for device Q_1 (except for $V_{dc} = 100$ V). In fact, at 200 V, both the peak and the final value of the power dissipated in Q_1 are higher than the ones of Q_2.

This different distribution of power dissipation between Q_1 and Q_2 leads to a non-monotonic trend of their SC energy with V_{dc}, as shown in Fig. 5.11 (a), in opposition to the case with $R_g = 100\ \Omega$, also reported in Fig. 5.11 (a) for a straight comparison. As clearly visible, the SC energy of Q_1 is much higher with $R_g = 22\ \Omega$ than in the case with $R_g = 100\ \Omega$ for all V_{dc} values and the same happens for Q_2 for V_{dc} higher than 250 V. A global comparison between the total SC energy, computed as the sum of Q_1 and Q_2 energies, for the two values of R_g is shown in Fig. 5.11 (b), where it can be noted that the total SC energy is higher for $R_g = 22\ \Omega$ in all V_{dc} conditions, and the difference between the total energies becomes larger as V_{dc} increases. Therefore, using a large gate resistor may lead to an underestimation of the real impact of the SC on the two devices in terms of energy and, therefore, in terms of electro-thermal stress.

The junction temperature estimation of the two devices is shown in Fig. 5.12 and was obtained using Simulink, as in the previous case. On the contrary of the condition

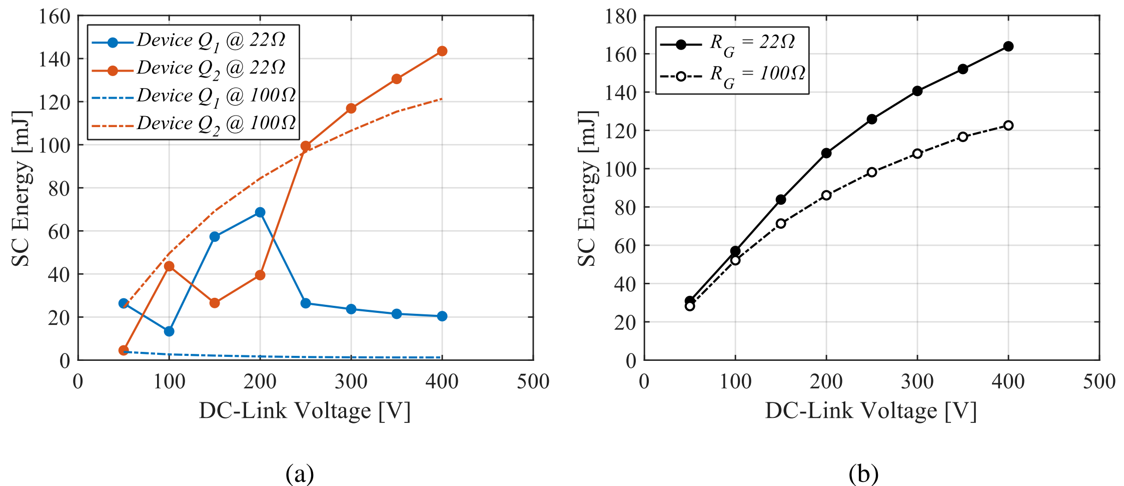
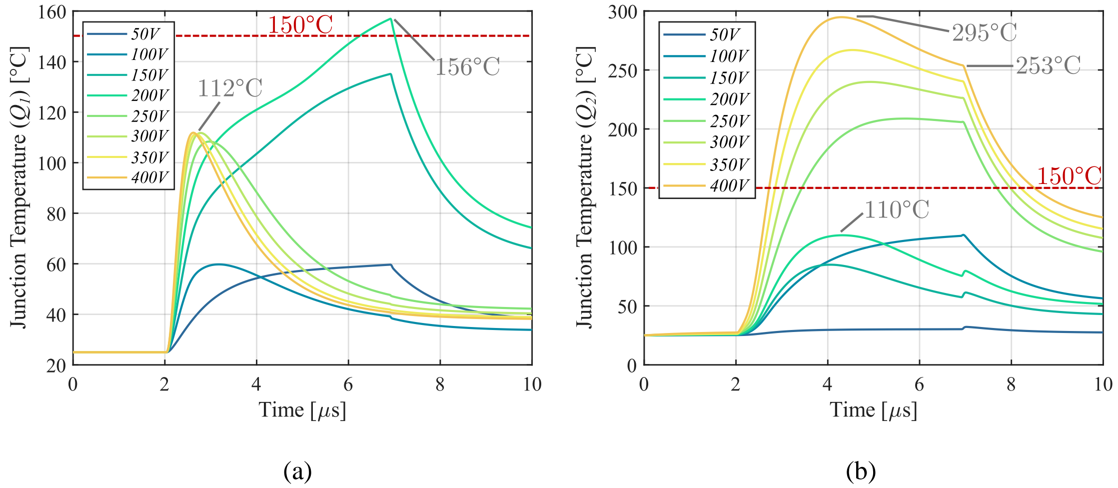


Fig. 5.11 Short Circuit energy of device Q_1 and Q_2 versus V_{dc} (a) and total SC energy in comparison between $R_g = 22\ \Omega$ and $R_g = 100\ \Omega$, in the condition $V_G = 5$ V.



(a) (b)

Fig. 5.12 Junction temperature estimation of device Q_1 (a) and Q_2 (b) using the manufacturer's Cauer thermal model. V_{dc} varies from 50 V to 400 V in the conditions $V_G = 5$ V, $R_g = 22\ \Omega$.

$R_g = 100\ \Omega$, device Q_1 is also interested by a noticeable increase of its T_j, that reaches a peak of 156 °C at $V_{dc} = 200$ V and about 112 °C for higher V_{dc}.

Anyway, its value overcomes the maximum limit of 150 °C only for 1 μs when V_{dc} is 200 V and is always lower in the other conditions. So, even if not negligible, the thermal stress of device Q_1 still remains limited. On the other hand, Q_2 undergoes a higher thermal stress and its T_j overcomes 150 °C for V_{dc} higher than 200 V. At $V_{dc} = 400$ V it reaches 295 °C and then decreases to 253 °C at the end of the SC. In the condition $R_g = 22\ \Omega$ the junction temperature of Q_2 reaches higher values than with $R_g = 100\ \Omega$, and this is compliant with the estimated higher values of the gate leakage current, that is directly related to T_j. The higher temperature at the end of the SC is a direct consequence of the higher drain current, as observed in the previous section.

5.4 Validation of the model

The experimental SC tests at different DC-link voltages and gate resistance are used to validate the behavioral model derived in Chapter 4. The model was implemented in LTSpice, integrating the manufacturer model with the drain and gate current equations derived from the I – V characterization of the 650 V – 60 A GaN HEMT. The simulations are performed according to the circuit scheme of Fig. 5.1 in the same conditions of the experimental tests. The stray parameters used in the circuit are listed in Table 5.1. The results are compared with both the experimental data and the simulation results obtained

with the manufacturer model. To simplify the discussion and the visualization of the results, two V_{dc} values are considered in the following, namely 100 V and 400 V. In fact, in these conditions the experimental results show considerable variations and therefore are suitable to validate the model in two different extreme conditions. Since the proposed model mainly affects the drain and gate currents, the discussion will be focused on the drain current I_D, the gate-source voltage V_{GS} and the gate current I_G.

The comparative results among the experimental data and the models are shown in Fig. 5.13 in the conditions $V_G = 5$ V and $R_g = 100\ \Omega$. In this condition, since the SC stress mostly involves device Q_2, as shown in 5.2, the attention is focused on its waveforms. The experimental waveforms of the drain current are compared with the simulation results of the manufacturer model and the proposed one in Fig. 5.13 (a) and (b), respectively. As shown in the figures, the manufacturer model overestimates the drain current at both 100 V and 400 V. The peak values of the simulated I_D are 200 A and 175 A at 100 V and 400 V respectively, with respect the real 165 A and 160 A. At the same time, the reduction of the current because of the increase of T_j does not represent the real behavior of the current. In fact, an overestimation of about 30 A is made at 100 V and 15 A at 400 V. The drain current is much more realistic with the proposed model, that accurately simulates both the peak and the final values at both V_{dc} values. The error in estimating the peak value is less than 2 A and is not appreciable in Fig. 5.13 (b). The difference between the experimental data and the simulated ones with the proposed model during the SC is mainly linked to the thermal model of the device, that probably underestimates the thermal time constant of the real device. Further insights about the

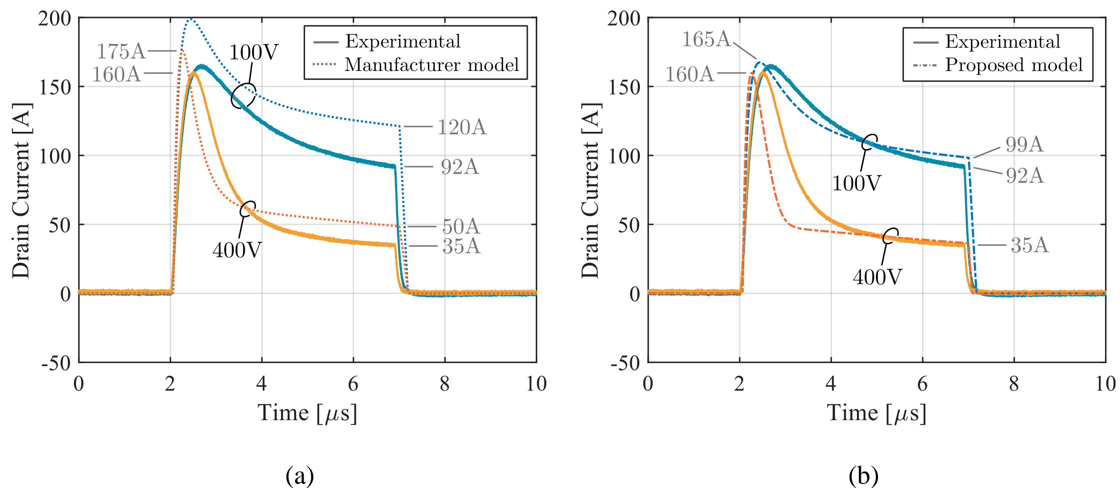


Fig. 5.13 Comparison between experimental and simulated waveforms of the drain current with (a) manufacturer model and (b) proposed model for V_{dc} equal to 100- and 400- V, in the condition $V_G = 5$ V, $R_g = 100\ \Omega$.

impact of the thermal model on the SC waveforms will be provided at the end of this section.

It must be noted that the thermal model is the manufacturer's one and it is used to obtain both the simulation results of Fig. 5.13 (a) and the ones of Fig. 5.13 (b). Therefore, the difference in the final values of I_D between the manufacturer and the proposed model is exclusively linked to the gate voltage reduction because of the increase of the gate leakage current $I_{G,Lk}$. This means that the gate leakage current effectively plays a role in the self-regulation mechanism of the drain current during the SC event. Its impact on the SC is only valuable with the proposed model, that takes into account the increment of $I_{G,Lk}$ with the temperature, providing a reliable instrument to characterize the SC behavior of the GaN HEMT under study.

The impact of $I_{G,Lk}$ is better highlighted in Fig. 5.14, that shows the gate-source voltage of device Q_2 during the SC and the simulated gate leakage current. The proposed model can correctly follow the real variation of V_{GS} and determine its value at the end of the SC, while with the manufacturer model V_{GS} remains fixed to 4.9 V, with a negligible gate leakage current. With the proposed model, V_{GS} decreases to 4.6 V at V_{dc} = 100 V, while the real value is about 4.3 V, and decreases to 2.7 V at V_{dc} = 400 V, that is very close to the real measured value of 2.6 V. The leakage current estimated from the drop of the measured V_{GS} at 100 V and 400 V is 6 mA and 24 mA (cf. 5.2), respectively. Instead, the leakage currents obtained from the simulation in the same conditions are about 3 mA and 24 mA. Therefore, the proposed model can predict the gate leakage current increase and

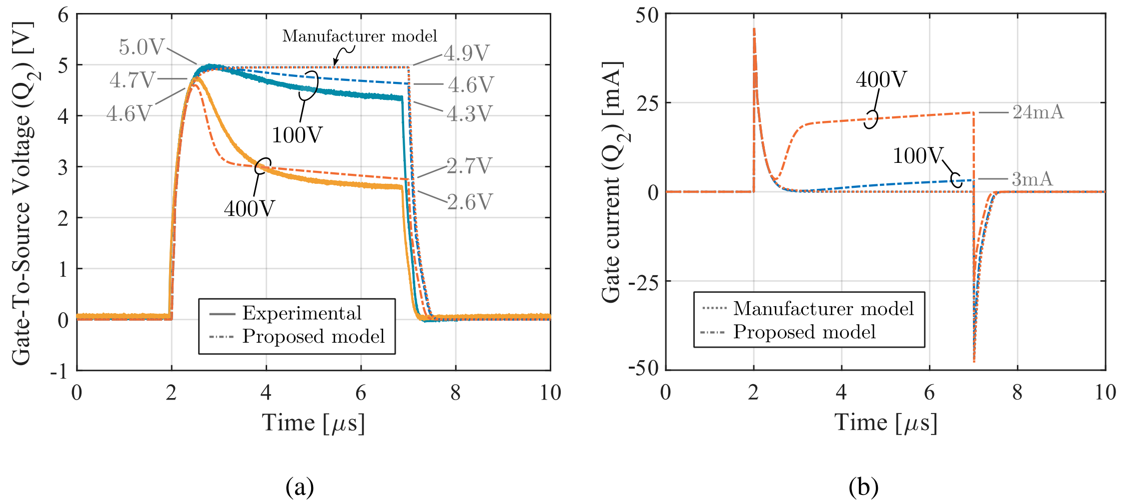


Fig. 5.14 Comparison between experimental and simulated waveforms of the gate-source voltage (a) and simulated gate current (b) for V_{dc} equal to 100- and 400- V, in the condition V_G = 5 V, R_g = 100 Ω.

the correspondence with the experimental results confirms that the dependence of $I_{G,Lk}$ with V_{GS} and T_j has been correctly derived.

Looking at Fig. 5.13 it can be noted that the rise time of the current is lower in simulations in comparison with the experimental results. This fact is not related to the improper definition of the input capacitance model, as can be verified considering the gate-source voltage of Fig. 5.14 (a), where the simulation results follow the same time evolution of the experimental ones. The faster current rise of the model among other possible causes can be also attributed to a higher threshold voltage of the real device tested compared with the one typical one considered in the manufacturer's model.

To provide an overall indication about the goodness of the proposed model also for other values of V_{dc}, the experimental and simulated SC energy of both devices are compared in Fig. 5.15. It can be noted that the manufacturer model overestimates the SC energy for device Q_2, while it underestimates the SC energy of device Q_1. The maximum absolute errors in the SC energy computation for Q_1 and Q_2 are 0.9 mJ (-34%, at 400 V) and 19 mJ (+38%, at 100 V) respectively. The proposed model reduces the error in the estimation of the SC energy in the whole range of V_{dc}, but still overestimates the energy dissipated by Q_2 and underestimates the one of Q_1. As an average, the proposed model provides a 5% overestimation for SC energy of device Q_2 and a 10% underestimation for device Q_1.

The model has also been validated in the conditions $V_G = 5$ V and $R_g = 22\ \Omega$, where the SC behavior of the two devices has proven to be strongly different from the previous

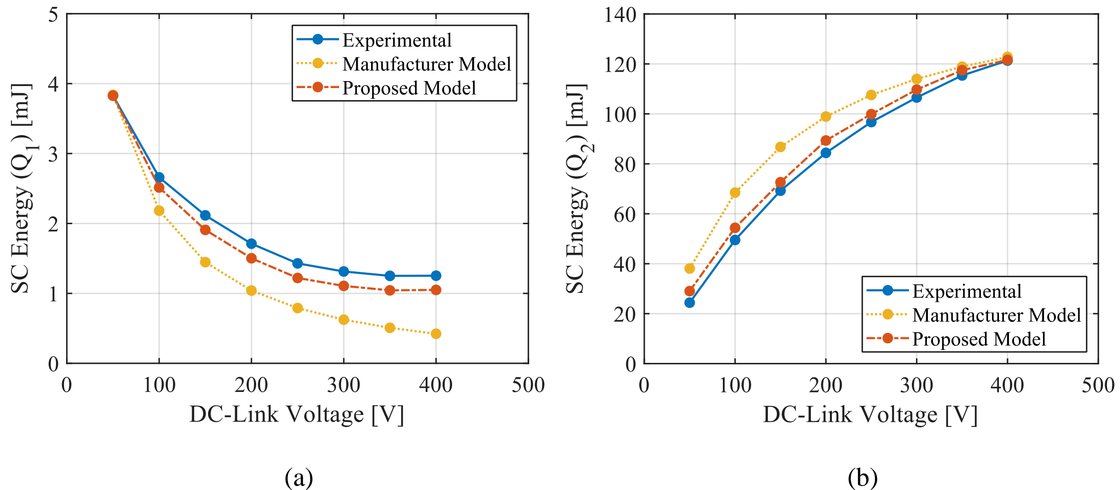


Fig. 5.15 Comparison between experimental and simulated SC energy of device Q_1 (a) and Q_2 (b) in the condition $V_G = 5$ V, $R_g = 100\ \Omega$.

case. In this condition, the SC stress involves device Q_1 for V_{dc} lower than 200 V, while Q_2 bears the electro-thermal stress for higher V_{dc}. Therefore, to provide a comprehensive evaluation of the model, both devices are considered in the following discussion.

The comparison between the experimental and the simulated waveforms is provided for the drain current and the gate-source voltages, while the gate leakage current involves the comparison between the simulation results of the manufacturer model and the proposed one. The SC energy is also evaluated for both devices, as in the previous case.

The experimental waveforms of the drain current are compared with the simulation results of the manufacturer model and the proposed one in Fig. 5.16 (a) and (b), respectively. The manufacturer model overestimates the drain current at both 100 V and 400 V. The peak values of the simulated I_D are 196 A and 182 A at 100 V and 400 V respectively, while the real measured values are 176 A and 170 A. The final value of I_D is also overestimated by about 10 A at 400 V, while it is correctly determined at 100 V, where it is equal to 102 A. The drain current obtained with the proposed model is correctly determined both at the peak and the final value at both V_{dc} values considered in this case. However, it must be noted that the reduction of I_D during the SC is not accurately represented neither by the manufacturer model nor by the proposed one. As for the previous case, this can be related to the thermal model used for the simulations and the different thermal response of the GaN HEMT during the SC tests, while the different rise time of the simulated drain current with respect the experimental one can be at least in part attributed to the higher threshold voltage of the real GaN device.

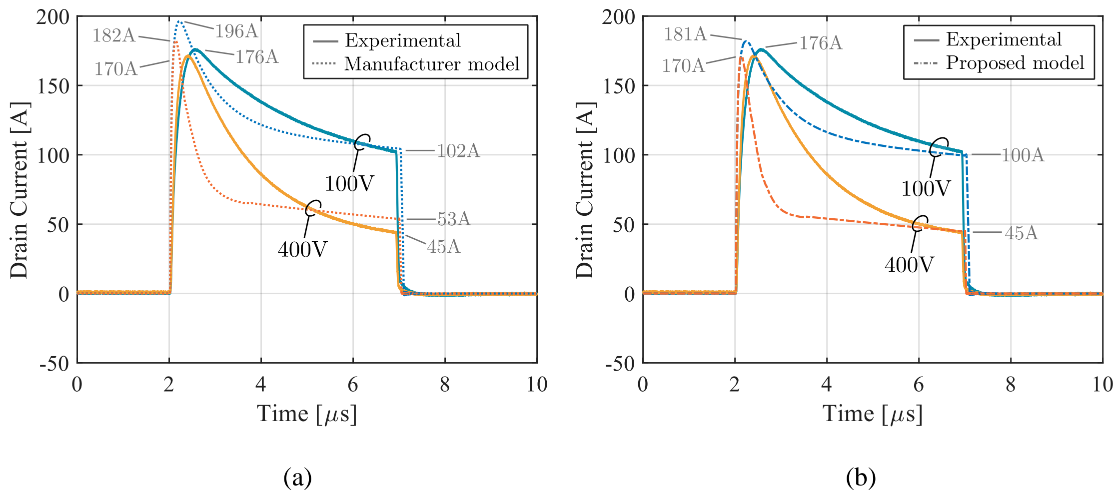


Fig. 5.16 Comparison between experimental and simulated waveforms of the drain current with (a) manufacturer model and (b) proposed model for V_{dc} equal to 100- and 400- V, in the condition $V_G = 5$ V, $R_g = 22\ \Omega$.

The model was able to follow the drain current variation in the previous condition with $R_g = 100\ \Omega$ (cf. Fig. 5.13), but other devices of the same ratings were used for the tests with $R_g = 22\ \Omega$. So, it is possible that not all the 650 V – 60 A GaN HEMTs used for the experimental tests show the same identical thermal response, affecting in a different way the drain current reduction during the SC event. Even if the peak and final values of I_D are correctly determined by the proposed model, this fact can lead to higher error in evaluating the mean power dissipation and the SC energy, because of the underestimation of the mean SC current.

Although better results could be reached by modifying the thermal model of the device in the LTSpice library, the accuracy of the proposed model can still be evaluated considering the differences with the manufacturer model in determining the peak values and the final values of the current. In fact, besides the higher accuracy reached in determining the peak values thanks to the proposed drain current model, the gate leakage current effect is responsible of the further reduction of I_D at the end of the SC, going from 53 A (manufacturer model) to 45 A (proposed model) at $V_{dc} = 400$ V. The difference is lower at $V_{dc} = 100$ V since the increment of $I_{G,Lk}$ is lower.

The considerations on the gate leakage current can be better understood looking at Fig. 5.17 and Fig. 5.18, that show the gate-source voltage of the two devices and their simulated gate leakage current.

At $V_{dc} = 100$ V the experimental and the simulated waveforms show some differences related to the mismatch between devices Q_1 and Q_2. During the experimental tests at

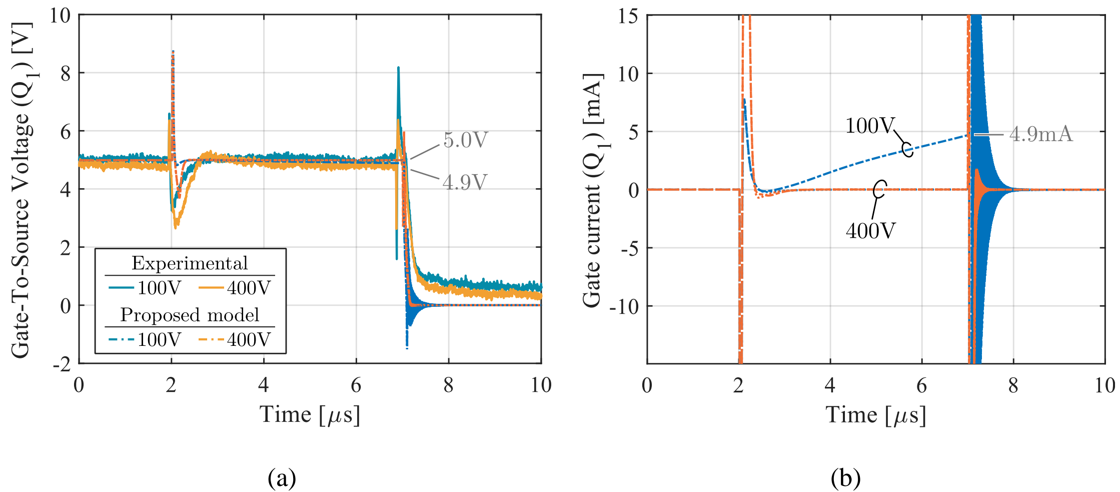


Fig. 5.17 Comparison between experimental and simulated waveforms of the gate-source voltage (a) and simulated gate current (b) of device Q_1 for V_{dc} equal to 100- and 400- V, in the condition $V_G = 5$ V, $R_g = 22\ \Omega$.

$R_g = 22\ \Omega$, device Q_1 suffers from a higher thermal stress for V_{dc} equal to 50-, 150- and 200- V, while the trend is stopped at $V_{dc} = 100$ V, where Q_2 undergoes the highest electro-thermal stress. This inverted trend at 100 V could not be approximated in the simulations, leading to a difference in the experimental and the simulated waveforms. In fact, the experimental waveforms of V_{GS1} in Fig. 5.17 show that a low thermal stress is caused by Q_1 and its leakage current is very low, since V_{GS1} remains at about 5.0 V. However, the simulated gate current shows a noticeable increase at 100 V up to 4.9 mA, indicating that the SC stress is borne by Q_1 in this condition. As a consequence, the simulated V_{GS1} slightly decreases to 4.9 V. On the contrary, the gate-source voltage V_{GS2} of device Q_2 decreases at $V_{dc} = 100$ V in the experimental tests, but the simulated one remains constant at 5.0 V, as shown in Fig. 5.18.

At $V_{dc} = 400$ V both V_{GS1} and V_{GS2} are simulated correctly by the proposed model. In fact, Fig. 5.17 shows that V_{GS1} remains practically constant and $I_{G,Lk}$ of device Q_1 is negligible, as the thermal stress is mainly on device Q_2. In Fig. 5.18 V_{GS2} in fact decreases from 5.2 V to 3.3 V at the end of the SC and is correctly represented by the simulated V_{GS} with the proposed model, while it remains constant at 5.0 V with the manufacturer model. The difference in the trend of V_{GS} during the SC is again related to the thermal response of the device, which affects both drain current, as discussed above, and the gate leakage current. The leakage current of device Q_2, estimated from the measured voltage drop on the experimental waveform of V_{GS}, is 84 mA and $I_{G,Lk}$ with the proposed model reaches 80 mA and therefore predicts the real increase of the gate leakage current with an error of about 7%.

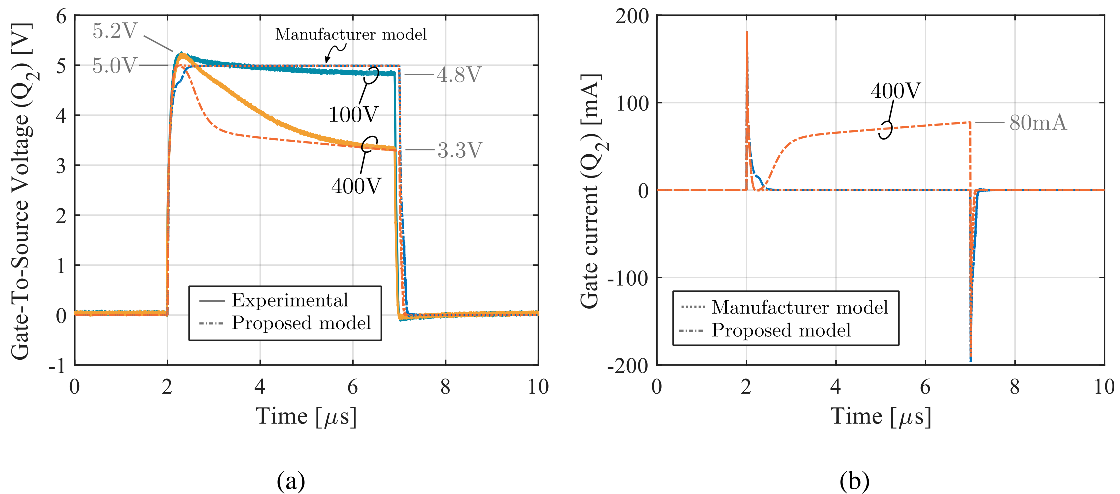


Fig. 5.18 Comparison between experimental and simulated waveforms of the gate-source voltage (a) and simulated gate current (b) of device Q_2 for V_{dc} equal to 100- and 400- V, in the condition $V_G = 5$ V, $R_g = 22\ \Omega$.

To conclude the analysis, the SC energy computed from the experimental results and the simulations is compared for both devices in Fig. 5.19, as it represents an overall parameter that can be used to evaluate the performance of the proposed model.

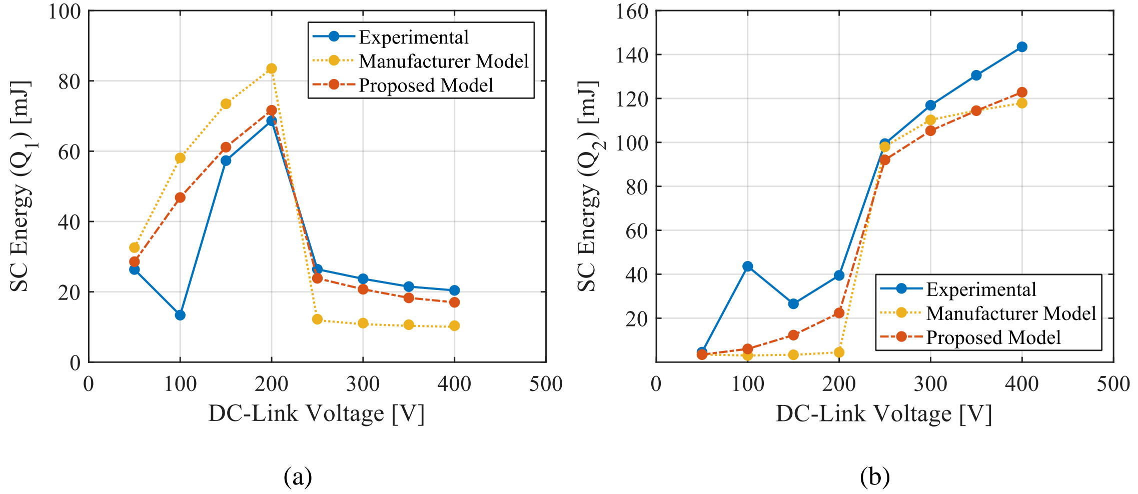


Fig. 5.19 Comparison between experimental and simulated SC energy of device Q_1 (a) and Q_2 (b) in the condition $V_G = 5$ V, $R_g = 22\ \Omega$.

It can be noted that the manufacturer model causes a larger error in computing the SC energy of device Q_1, overestimating the SC energy for $V_{dc} \leq 200$ V and underestimating it for higher V_{dc}. The error is reduced in all the range of V_{dc} with the proposed model, with an average error of -10% in the region $V_{dc} > 200$ V and +5% in the region $V_{dc} \leq 200$ V, excluding $V_{dc} = 100$ V where neither the manufacturer and the proposed model are able to represent the real behavior of the HB, leading to a large error in computing the SC energy. This happens because at $V_{dc} = 100$ V the HB shows an unstable behavior during the SC, and the device suffering the highest stress depends on the variation of V_{GS} and T_j and is also influenced by the parasitic components in the circuits. For device Q_2 the results obtained with the manufacturer model and the proposed one are quite close, even if the proposed model achieves lower errors in the region $V_{dc} \leq 200$ V and at $V_{dc} = 400$ V.

5.4.1 Impact of thermal model

As introduced above, the thermal model of the GaN HEMT is responsible of the main differences between the simulation and the experimental results. The thermal model used for the simulations is a Cauer equivalent model with four RC networks with constant parameters [50], already presented in 1.4.5. The equivalent circuit representing the thermal model is reported here in Fig. 5.20 for completeness and its parameters are listed

in Table 5.2. In the network, the cell that mainly determines the temperature evolution during the SC event is the one with the lowest time constant, that actually consists of the RC cell connecting the junction and the GaN substrate, also highlighted in Fig. 5.20.

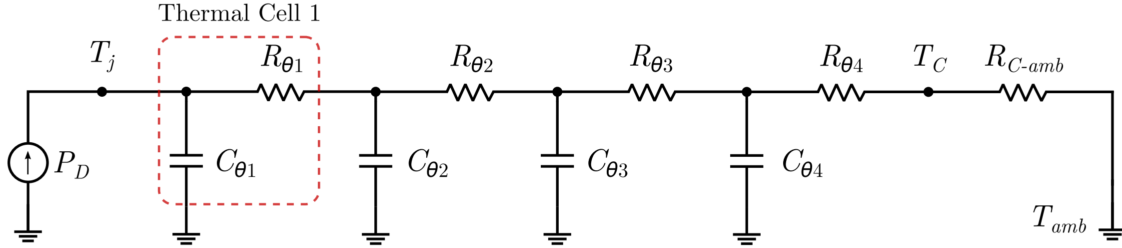


Fig. 5.20 Cauer thermal model of the GaN HEMT used for the LTSpice simulations.

Table 5.2 Parameters for the Cauer thermal model of GS66516T.

Thermal Model					
Thermal Capacitance [Ws/°C]		***Thermal Resistance*** [°C/W]		***Time Constant*** [s]	
Symbol	***Value***	***Symbol***	***Value***	***Symbol***	***Value***
$C_{\theta 1}$	$1.4 \cdot 10^{-4}$	$R_{\theta 1}$	0.01	τ_1	$1.40 \cdot 10^{-6}$
$C_{\theta 2}$	$1.23 \cdot 10^{-3}$	$R_{\theta 2}$	0.14	τ_2	$172 \cdot 10^{-6}$
$C_{\theta 3}$	$10.8 \cdot 10^{-3}$	$R_{\theta 3}$	0.14	τ_3	$1.5 \cdot 10^{-3}$
$C_{\theta 4}$	$3.3 \cdot 10^{-3}$	$R_{\theta 4}$	0.01	τ_4	$33 \cdot 10^{-6}$

In order to compensate the different thermal response of the GaN device, the first RC cell of the manufacturer thermal model was modified and, after a fitting procedure, the new values adopted in the thermal network are $C_{\theta 1} = 5.6 \cdot 10^{-4}$ Ws/°C and $R_{\theta 1} = 0.008$ °C/W. The thermal capacitance has been increased by 4 times compared with its original value, while the thermal resistance has been decreased by 20%.

The comparison between the simulated and the experimental waveforms of the drain current and the gate voltage of device Q_2 are reported in Fig. 5.21 in the conditions $V_G = 5$ V, $R_g = 22\ \Omega$. The gate current model also needed to be modified to correctly represent the gate leakage current increase and the value of parameter m (cf. 4.4) was set to 0.07 °C^{-1}.

After the modification of the thermal model, both the current and the gate voltage evolution are better approximated by the proposed model during the SC, indicating that

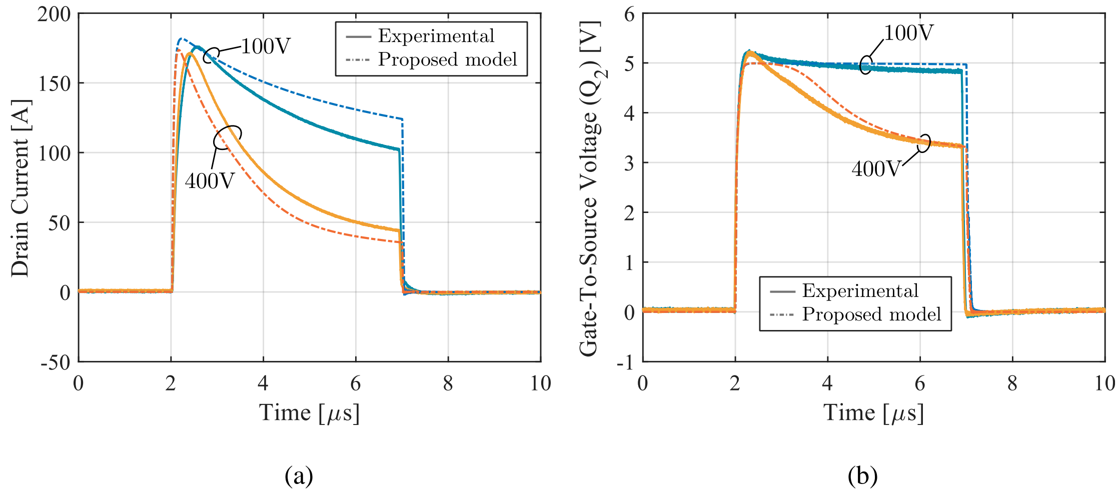


Fig. 5.21 Comparison between experimental and simulated waveforms of the drain current (a) and gate voltage of device Q_2 (b) with the modified thermal model. The test conditions are $V_G = 5$ V, $R_g = 22$ Ω.

the derived electrical model for the drain and gate current is in good agreement with the experimental results and can be used to evaluate the SC behavior of the GaN-based HB. On the other hand, an improvement of the GaN HEMT's thermal model is necessary to increase the accuracy of the simulation.

The manufacturer thermal model is derived from 3D finite element simulations considering a constant power dissipation on the device operating in normal conditions, as described in [76]. With this assumption, the heat transfer mainly involves the surface of the GaN layer, with a quite homogeneous temperature distribution along the channel. The equivalent thermal impedance is determined in this condition, but different works have demonstrated that during the SC the power density is mainly focused in a small area of the channel, under the gate towards the drain side [35], [41]. Moreover, during the SC the high power dissipation causes the heat transfer to involve a larger thickness of the GaN substrate, as also shown in [41]. Therefore, the volume involved in the heat transfer is increased, leading to a larger thermal capacitance. On the other hand, the larger thickness of the thermal power distribution reduces the effective length between the center of the heat generation and the substrate, leading to a lower thermal resistance. This explanation is consistent with the new values of thermal capacitance and resistance used for the first cell of the Cauer thermal model.

Considering the modifications of the thermal model and its impact on the simulated drain current waveforms, that better represent the real current evolution during the SC, the SC energy dissipated by the two GaN devices was computed again, performing the simulations with the proposed model for V_{dc} varying from 50 V to 400 V in 50 V steps

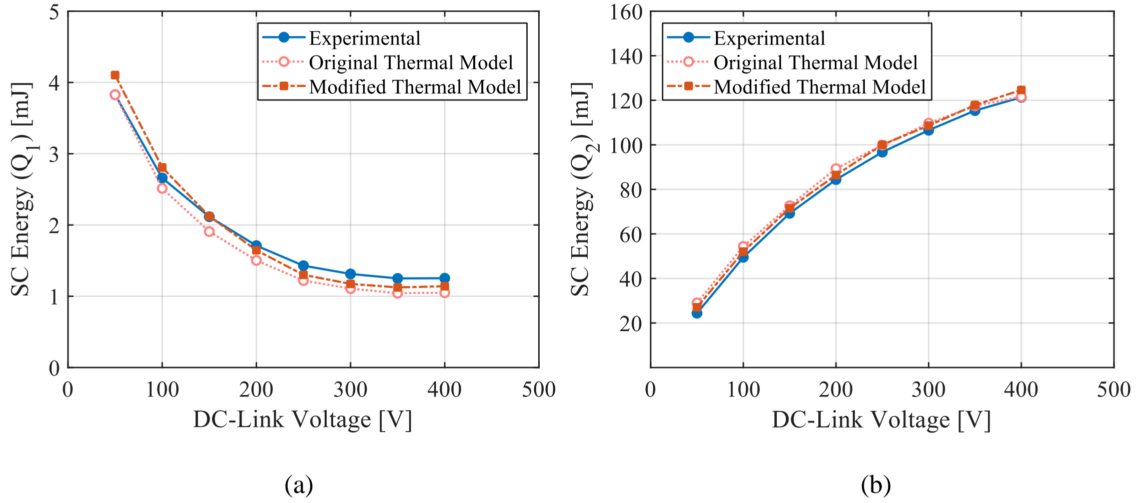


Fig. 5.22 Comparison between experimental and simulated SC energy of device Q_1 (a) and Q_2 (b) in the condition $V_G = 5$ V, $R_g = 100\ \Omega$ before and after the modification of the thermal model.

and $V_G = 5$ V. The SC energy computation was performed with the modified thermal model both with $R_g = 100\ \Omega$ and $R_g = 22\ \Omega$. Fig. 5.22 and Fig. 5.23 show the SC energy computed using the proposed model with the modified thermal model for the latter two cases. It can be noted that the modification of the thermal model strongly improved the accuracy of the SC energy computation, reducing the error in all the range of V_{dc} for both devices and for both R_g conditions.

Looking at Fig. 5.22, the use of the modified thermal model for $R_g = 100\ \Omega$ determines the reduction of the maximum error in underestimating the SC energy for device Q_1, that goes from -20% to -10% at $V_{dc} = 400$ V. Moreover, the average error in overestimating the SC energy of device Q_2 also decreased from +5% to +3.5%.

The improvement of accuracy is mainly visible for $R_g = 22\ \Omega$, where the original thermal model caused a major underestimation of the drain current during the SC (cf. Fig. 5.16 (b)). In fact, as visible in Fig. 5.23, the SC energy computed with the modified thermal model shows a lower deviation with respect the experimental results. The SC energy of device Q_1 is overestimated by 4% for $V_{dc} \leq 200$ V, except for the case $V_{dc} = 100$ V, and underestimated by 2% for higher V_{dc}, improving the accuracy of the proposed model. Instead, excluding the case $V_{dc} = 100$ V, the SC energy of device Q_2 is underestimated in all V_{dc} range, but the accuracy in determining its value is strongly increased, with a maximum error of 7% occurring at $V_{dc} = 400$ V where it was 18% for the previous thermal model.

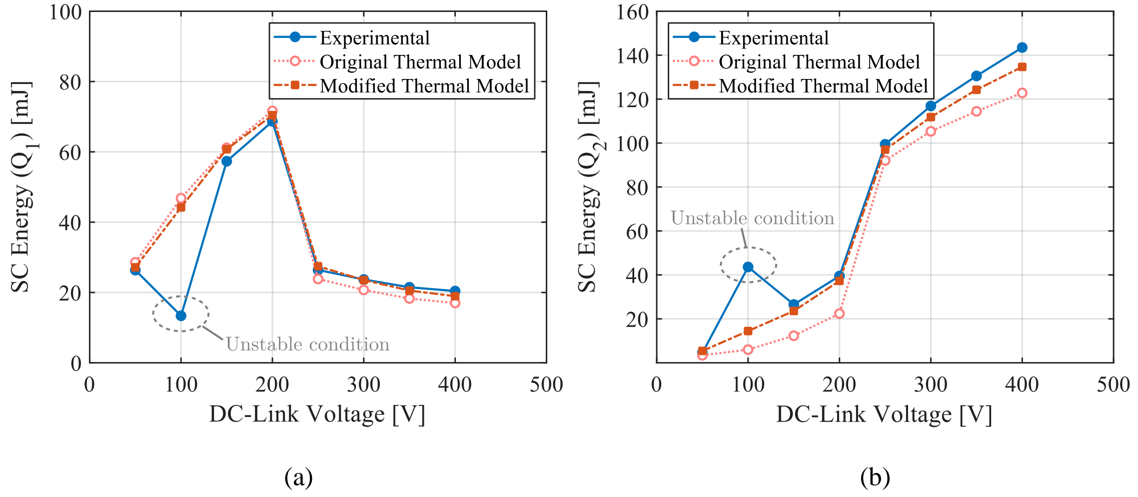


Fig. 5.23 Comparison between experimental and simulated SC energy of device Q_1 (a) and Q_2 (b) in the condition $V_G = 5$ V, $R_g = 22\ \Omega$ before and after the modification of the thermal model.

5.5 Temperature estimation through the gate leakage model

The close and simple equation found for the gate leakage current of the 650 V – 60 A was presented in section 4.4 and it is dependent on V_{GS} and T_j. The derived equation can be used to predict the junction temperature of the GaN HEMT both in SC conditions and in normal operating conditions, as first proposed in [122]. The equation, reported here for clarity, is expressed by

$$I_{G,Lk} = I_{G0} \cdot e^{mT_j + q(V_{GS})} \tag{5.3}$$

where m and I_{G0} are constant parameters and $q(V_{GS})$ is a rational function of V_{GS}. This equation can be inverted and used to derive the expression of T_j as a function of the gate leakage current, leading to

$$T_j = \frac{1}{m}\left[ln\left(\frac{I_{G,Lk}}{I_{G0}}\right) - q(V_{GS})\right] \tag{5.4}$$

The SC experimental results presented in the previous sections can be used to evaluate the capability of the model to estimate the junction temperature from the gate leakage measurement. Considering the test condition $V_G = 5$ V, $R_g = 100\ \Omega$, the gate leakage current of device Q_2 can be extracted from the experimental waveforms of the gate-source voltage V_{GS} at the end of the SC event by computing the value according to

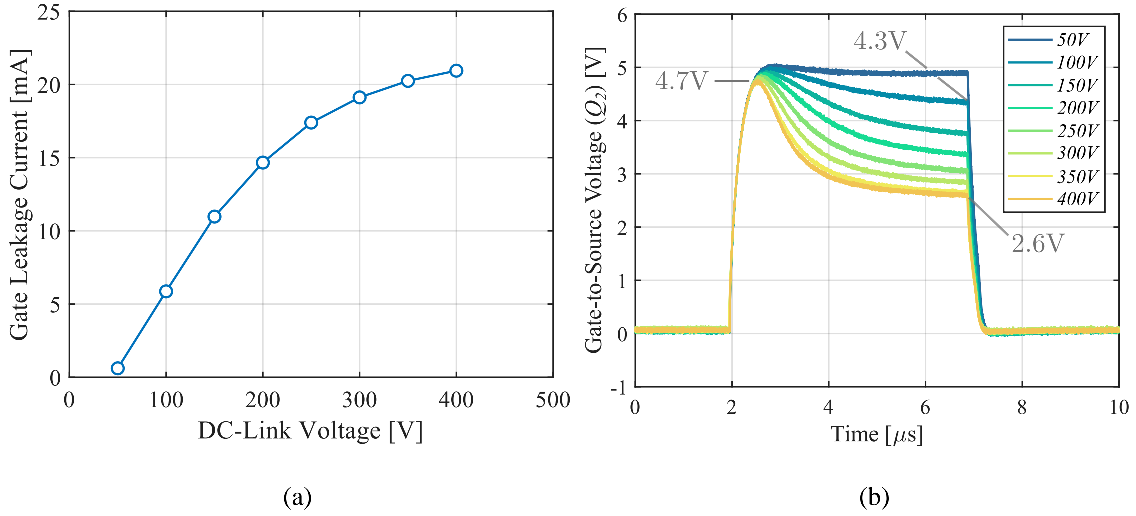


Fig. 5.24 Values of $I_{G,Lk}$ for device Q_2 extracted from experimental waveforms at different V_{dc} in the test condition $V_G = 5$ V, $R_g = 100\ \Omega$ (a) and gate-source voltage waveforms of device Q_2 used to compute $I_{G,Lk}$ (b).

$$I_{G,Lk} = \frac{\Delta V_{GS}}{R_g} - \frac{V_{GS}}{R_{gs}} \tag{5.5}$$

Where ΔV_{GS} is the voltage drop evaluated on the V_{GS} waveforms from the beginning to the end of the SC and R_{gs} is the pull-down resistance between the gate and source and it is equal to 10 kΩ. Even if small, a fraction of the whole gate current is sink by R_{gs}, equal to 0.5 mA at $V_{GS} = 5$ V, and if it is neglected a major error can be made especially in estimating low temperatures, when the gate leakage current is in the order of hundreds of μA or few mA. The extracted values of $I_{G,Lk}$ are plotted versus V_{dc} in Fig. 5.24 (a), where it is shown that $I_{G,Lk}$ varies from 600 μA to 21 mA as V_{dc} increases. The waveforms of V_{GS} used to compute $I_{G,Lk}$, already presented in 5.2, are reported in Fig. 5.24 (b) for completeness.

The values of $I_{G,Lk}$extracted from experimental data are used as inputs in (5.4) to obtain the estimation of T_j. The computed values of the couples $I_{GLk} - T_j$ are plotted in Fig. 5.25 (a), where the solid lines represent the function expressed by (5.4) for different values of V_{GS} varying from 2 V to 6 V in 1 V steps. The locations of the red circles in the $I_{GLk} - T_j$ plane are determined considering the value of V_{GS} at the end of the SC, which was used to calculate ΔV_{GS} and $I_{G,Lk}$. Therefore, the obtained values of T_j represent an estimation of the junction temperature at the end of the SC event.

The obtained values of T_j are then plotted in Fig. 5.25 (b) as a function of V_{dc}. For a comparison, Fig. 5.25 (b) also shows the temperature at the end of the SC at each V_{dc} obtained with the Simulink simulations using the thermal model of the GaN HEMT and the experimental power dissipation as input. As visible, the values estimated through the gate leakage equation are very close to the simulated data and therefore the proposed gate leakage equation represents a suitable instrument for the junction temperature estimation and its real-time monitoring.

The same procedure can be applied to estimate T_j of devices Q_1 and Q_2 at the end of the SC in the conditions $V_G = 5$ V, $R_g = 22$ Ω. However, for low temperatures the value of $I_{G,Lk}$ cannot be calculated with precision from the V_{GS} waveforms, because of the much lower voltage drop on R_g and the presence of unavoidable noise. This fact brings to large errors in the computation of very low gate leakage currents and a consequent error in estimating the corresponding junction temperature. This issue can be easily overcome with a custom circuit for the sensing of the gate current directly on the gate resistor, achieving higher precision. Besides this, it has been possible to obtain more accurate results in estimating the temperature for higher T_j and $I_{G,Lk}$ and they are shown in Fig. 5.26. In this figure the simulated and estimated temperatures of both GaN HEMTs are compared, showing a good agreement among the results for temperature higher than 100 °C, while the estimated data at lower temperatures are not reported because affected by large errors for the reason explained above.

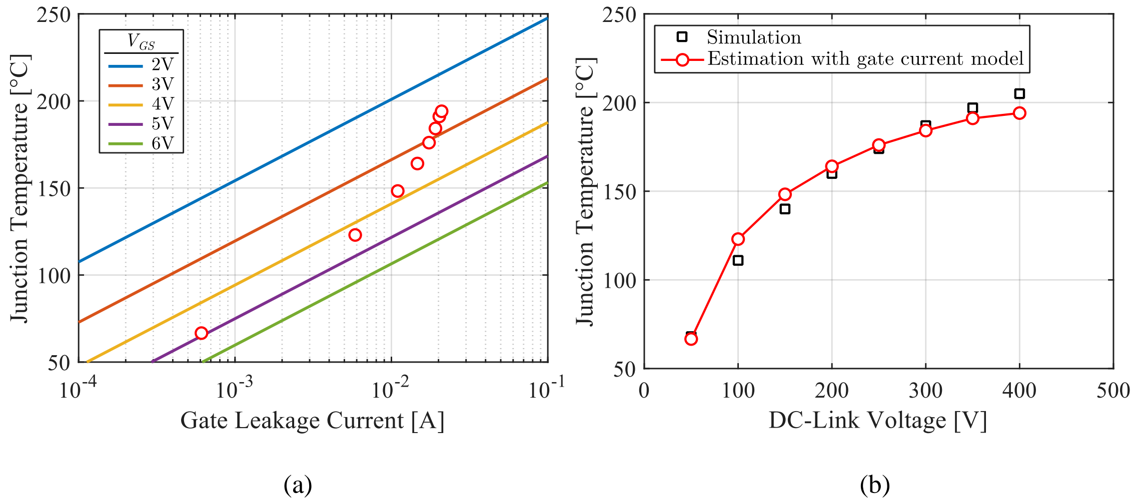
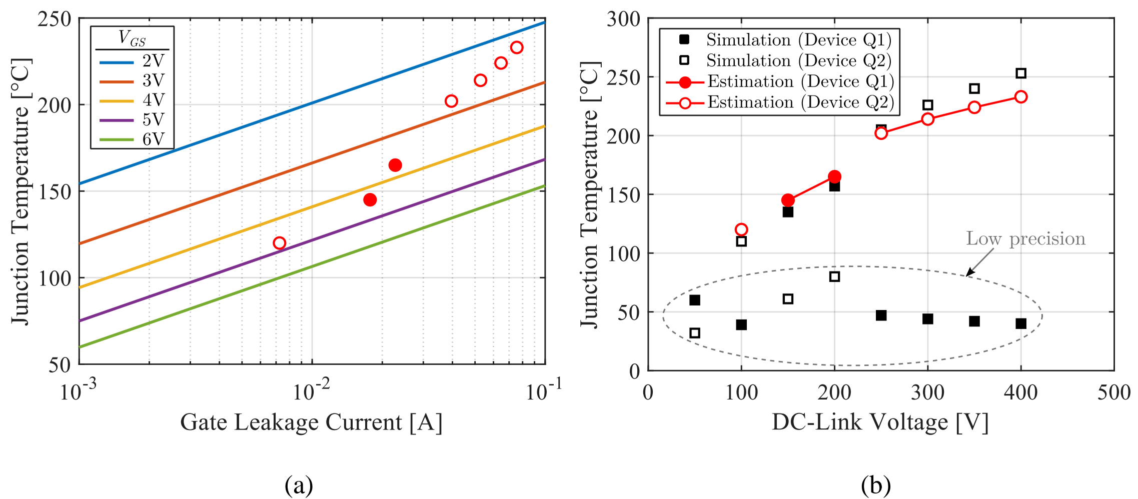


Fig. 5.25 Estimated T_j in the $I_{GLk} - T_j$ plane (a) and comparison between estimated and simulated T_j versus V_{dc} (b) in the test condition $V_G = 5$ V, $R_g = 100$ Ω.

Anyway, the results of Fig. 5.25 and Fig. 5.26 show the capability of the model to predict the junction temperature of the GaN HEMT during the SC through the gate leakage current. If the measurement of the gate leakage current is implemented in a custom sensing circuit, the model can also be used for the real-time measurement of the junction temperature both in normal operating conditions and during the SC [122]. Moreover, the direct relationship between the gate leakage current and the junction temperature can be exploited in the detection of the SC event, linking the fast temperature increase with the corresponding increase of the gate current. Thus, according to the proposed gate current model, it is possible to design a sensing and protection circuit for the SC of a GaN-based HB by defining a maximum threshold for the gate leakage current, corresponding to the maximum temperature in the device, to not exceed during the SC occurrence.



(a) (b)

Fig. 5.26 Estimated T_j in the $I_{GLk} - T_j$ plane (a) and comparison between estimated and simulated T_j versus V_{dc} (b) of both GaN HEMTs in the test condition $V_G = 5$ V, $R_g = 22\ \Omega$.

6
Conclusions and Outlooks

6.1 Conclusions

This thesis has focused on the analysis of the Short Circuit (SC) behavior of a GaN-based Half Bridge (HB) and the development of a behavioral model for a 650 V – 60 A GaN HEMT. The SC robustness is one of the crucial aspects for power devices and still represents a limitation factor for the widespread use of GaN HEMTs in power electronics applications. The SC ruggedness of medium voltage (600/650 V) GaN HEMTs has been widely investigated in the literature and it has been proven to be lower than SiC and Si MOSFETs of the same rating, showing a withstand time that collapses to few hundreds of nanoseconds at 400 V DC-link voltage, that is a common value used in many power applications.

This thesis tried to extend the common procedure of testing GaN HEMTs under SC conditions, studying the simultaneous impact of the SC on two identical GaN devices in HB configuration. In fact, in the literature the SC characterization is presented focusing on a single device, that however is not representative of the real conditions during which a SC can take place, i.e. in HB-based converters.

A preliminary theoretical and simulative analysis performed on a 650 V – 60 A GaN-based HB has investigated the behavior of the two devices during the SC. Neglecting any mismatch between the two devices, the SC event causes a strong electro-thermal stress on the device that turns on after its blocking phase, so with the whole DC-link voltage applied across it. In fact, it operates in the saturation region with high drain current and voltage, dissipating a huge instantaneous power that makes the junction temperature increase far beyond the maximum operating temperature limit. On the other hand, the other device

experiences a type II SC, starting with zero drain voltage and current. This fact reduces its electro-thermal stress and, after a transient region where it can operate in the saturation region, its working point returns in the linear region, where the device behaves like a variable resistor and dissipates much lower power.

The influence of various circuit parameters has been investigated, such as the DC-link voltage, the gate driver voltage, the gate resistance and the parasitic inductances. The DC-link voltage plays a major role in determining the entity of the SC stress on the GaN HEMTs, as the electro-thermal stress increases with its value and it can bring the devices to failure for voltages higher than 300 V. The gate driver voltage has a relevant impact on the SC current, determining its peak value and so the related peak power dissipation. Therefore, using reduced gate driver voltages with respect the recommended driving conditions can help in preventing the failure of the devices for high voltage operations, where the failure is related to the high local current density. However, the reduction of the gate driving voltage is less helpful for long SC events at lower DC-link voltages, where the temperature determines the reduction of the current independently of the gate voltage and the failure is associated with the excessive temperature along the structure of the device. Large gate resistors are beneficial during the SC event, reducing the *di/dt*, turn-off oscillations and preventing instabilities on the devices, but they can also lead to unrealistic results on the SC behavior of the HB, underestimating the involved energy dissipation, as proven with the experimental results provided in the thesis. The simulation analysis shows that the peak SC current can be reduced with large gate resistor because of the slowing down of the current dynamics with respect the thermal one. Therefore, using large gate resistance seems to be beneficial for the SC, though it has little practical use in normal operating conditions.

When a mismatch between the devices is present in the circuit and, in particular, on the common-source path, leading to different stray inductances, the two devices undergo strongly different behaviors with respect the ideal case, depending in particular on the applied DC-link voltage. In this case, the two devices can swap their behavior and the GaN HEMT that should bear a type II SC, with lower electro-thermal stress, actually experiences a type I SC, dissipating a high power. A behavioral interpretation of this phenomenon has been provided using the output characteristic of the two devices and showing the trajectories of their operating points under various DC-link voltage operations.

The increase of temperature is responsible of all the main mechanisms acting during the SC operation of GaN HEMTs, such as the drain current reduction and the gate leakage current increase. However, the comparison of experimental results of SC tests and simulations using the manufacturer model for the 650 V – 60 A device shows significant differences in both the drain and gate currents. In this perspective, an experimental I – V

characterization of both drain and gate currents is performed in the thesis with the goal of developing an improved simulation model, that can be used as a reliable instrument to evaluate the real SC operation of the GaN HEMT under study.

A custom test board has been designed to perform the pulsed I – V characterization and SC tests, but it is suitable also for Double Pulse Tests and as a primary stage of a converter. The prototype is made of two 650 V – 60 A GaN HEMTs with the corresponding driver circuits, auxiliary power supply and DC-link capacitors, and it was constructed on a four-layers 14 x 16 cm PCB.

A pulsed gate I – V characterization has been performed to determine the drain current at different gate-source voltages and constant temperature. The results were used to derive a behavioral model for the drain current that gathers together the manufacturer model and a proposed fitting equation that only uses six parameters. The accuracy of the proposed drain current model has been evaluated for all the tested gate-source voltages, showing an overall error less than 6 A. The parameter analyzer 4200A-SCS was used to perform the gate characterization at different voltages and temperatures, obtaining the gate leakage current dependence with V_{GS} and T_j. An exponential regression was applied to the data of gate leakage current versus temperature to extract a simple behavioral model that expresses the gate leakage current as a closed function of junction temperature and gate-source voltage. The proposed gate current model showed a high accuracy for temperatures lower than 150 °C, with an error lower than 500 μA, while it becomes less accurate for higher temperatures, due to a simplification made in the exponential regression. Finally, the proposed models of drain and gate currents have been integrated in LTSpice and a Simulink implementation has been also proposed.

The results of non-destructive experimental SC tests on the realized prototype have been presented, with the capability of evaluating both type I and type II SC on the GaN devices. In the thesis, a type I SC was performed on the low-side device and a type II SC on the high-side one. The effect of DC-link voltage was evaluated and two values of gate resistance have been used, namely 100 Ω and 22 Ω. The experimental results have confirmed the theoretical analysis and were used to derive some crucial parameters of the SC, such as the power dissipation, the SC energy and an estimation of the junction temperature of both devices. With 100 Ω gate resistance, the low-side GaN HEMT endured the highest electro-thermal stress, with a peak power dissipation of 60 kW and a peak junction temperature of 267 °C, while the high-side device showed a 2.5 kW peak power dissipation and a neglectable temperature increase.

Two virgin GaN devices of the same ratings were used to perform the SC tests with 22 Ω gate resistance. In this condition, the behavior of the two devices changed, due to the mismatch between the common-source stray inductance of the transistors and the

higher *di/dt* imposed by the lower gate resistor. This condition leads the HB to be like a bistable system, where the electro-thermal stress of the devices is strongly dependent on the stray inductance and the operating conditions. A higher electro-thermal stress was endured by the high-side device for DC-link voltages lower than 200 V, with a peak power dissipation of 25 kW and a temperature of 156 °C. For higher DC-link voltages, the low-side device returns to bear the SC stress, reaching a 53 kW peak power dissipation and a temperature of almost 300 °C. However, also the high-side device suffered from a huge transient power dissipation, with a peak of 44 kW at 400 V that quickly decreases to zero in less than 2 μs. Moreover, in the tests with 22 Ω gate resistor the SC energy of the two devices became comparable and significantly higher in comparison with the results with 100 Ω gate resistor, indicating how the SC behavior of the HB can be strongly influenced by the *di/dt* and the presence of differences in the circuit layout of the devices. Using a large gate resistor can lead to an underestimation of the real impact of the SC on the two devices in terms of energy and electro-thermal stress.

The experimental results of the SC tests have been used to validate the proposed drain and gate current models and evaluate the impact of the gate leakage on the SC for two values of DC-link voltage. With 100 Ω gate resistor the model is able to accurately simulate the real SC behavior of the devices, in terms of both drain and gate currents. The influence of the gate leakage current was clearly shown, highlighting that at the end of the SC a further drain current reduction of about 10 A is present when the gate leakage current is considered, because of the gate voltage reduction from 5.0 V to 2.6 V. The comparison of the SC energy computed with the manufacturer model, the proposed one and the experimental results showed an improvement of the SC modeling achieved with the proposed model. With 22 Ω gate resistor the model showed less accuracy, mainly due to the different behavior of the two devices because of the effects of the stray inductance, which is difficult to incorporate. The gate leakage current was correctly simulated by the model, reaching about 80 mA at 400 V. However, because of the lower gate resistance, the impact of this leakage current was reduced and the gate-source voltage decreased from 5.0 V to 3.3 V at 400 V. The peak and final values of the drain current were correctly determined, but a difference in the thermal response of the devices was noted when comparing the simulation and the experimental results, indicating that also the thermal model of the GaN HEMT should be improved to accurately simulate the SC behavior.

The manufacturer's thermal model was modified to highlight its impact on the simulation results and prove the accuracy of the proposed model. Changing one thermal cell of the model led to a valuable improvement of the SC current evolution and decreased the error in estimating the SC energy of the two GaN devices for both values of R_g.

The gate leakage current equation, since incorporating a simple and direct relationship with the temperature, was used to show the possibility to estimate the junction temperature

of the GaN HEMT during the SC. The gate leakage current at the end of the SC was computed measuring the voltage drop on the gate resistance and used to determine the junction temperature according to the inverted equation of the gate leakage current model. For the SC tests with 100 Ω gate resistor the estimated temperature was very close to the simulated one, whereas with a 22 Ω gate resistor the lower voltage drop results in a much lower resolution in determining the leakage current and, therefore, the temperature. Nevertheless, the estimation of the junction temperatures for values higher than 100 °C showed a good agreement with the simulated values.

6.2 Outlooks

The results presented in this thesis are a starting point for further analysis on the SC behavior of GaN HEMTs in Half Bridge-based power converters and provide an overview of the main critical mechanisms that can affect the SC operation of GaN-based converter.

The model developed for the 650 V – 60 A GaN HEMT can be used to predict with high accuracy the SC operation of the single device and of the HB, representing an useful instrument also to design a protection circuit against the SC for half bridges-based topologies. However, the thermal model of the GaN HEMT, which is supplied by the manufacturer in static power dissipation conditions, needs to be further improved to correctly simulate the SC evolution of drain and gate currents, taking into account the different thermal impedance involved during the SC.

The derived gate leakage current equation has been proven to be capable of estimating the junction temperature from the sensing of the gate leakage current. This capability can be exploited in real-time operation of GaN-based power converters for the monitoring of the temperature if a proper circuit for the gate current sensing is designed. Moreover, it could be used to detect the SC event on a HB by defining a threshold leakage current representative of the maximum admissible temperature that must not be exceeded to avoid the failure of the GaN HEMTs.

Moreover, the scalability of the proposed model can be evaluated, analyzing the possibility to extend the drain and gate models to other GaN HEMTs of the same family by defining an appropriate scaling method. In this way, the SC behavior of GaN HEMTs with different ratings could be analyzed and characterized without exclusively performing experimental tests, that are time- and cost- expensive.

The model can also be extended to simulate the failure of GaN HEMTs under various operating conditions and define the safe operating boundaries, trying to represent both the failure mechanism due to the extreme temperature rise in events with long SC times and

that related to the high current density that can lead the device to destruction within a few hundred nanoseconds.

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