UNIVERSITY OF MONASTIR
FACULTY OF SCIENCES OF MONASTIR

UNIVERSITÀ DEGLI STUDI DI
CASSINO E DEL LAZIO MERIDIONALE

Doctoral Thesis:

Electrothermal Analysis of Memristors and Thermistors

by

Khitem Lahbacha

joint PhD degree in

"Metodi, modelli e tecnologie per l'ingegneria" (Ciclo XXXIV)
University of Cassino and Southern Lazio (Italy)
Dip. di Ingegneria Elettrica e dell'Informazione (DIEI)
and
"Electronics & Microelectronics"
University of Monastir (Tunisia)
Lab. of Electronics and Microelectronics (Code: LR99ES30h)

Prof. Antonio Maffucci	Supervisor
Prof. Hamdi Belgacem	Supervisor
Prof. Wael Dghais	Supervisor

Defended on .....,2022 in Università Degli Studi di Cassino e Del Lazio Meridionale.

"Dream, Dream, Dream
Dreams transform into thoughts
And thoughts result in action.
Dream is not that which you see white sleeping,
It is something that does not let you sleep"

A.P. J. Abdul Kalam

ACKNOWLEDGEMENTS

These research works were carried out at the dipartimento di ingegneria elettrica e dell'informazione (DIEI), Università degli Studi di Cassino e del Lazio Meridionale and at the lab of electronics and microelectronics, Faculty of Sciences of Monastir. This work was also partially supported by the program “Dipartimenti di Eccellenza 2018-2022”, MIUR, Italian Ministry of University.

‘‘Let us be grateful to people who make us happy”

Sometimes, life brings a lot of surprises and things that we did not expect. When I started my thesis, I never imagined that along the way I would work with a special person daily for more than 3 years of my thesis. I am certainly talking about my Italian supervisor **Prof. Antonio Maffucci**, who gives me the opportunity to work with him and be a member of the University of Cassino and Southern Lazio. From the start to the end, he was as involved in the thesis as me and was always present and looking for new ways, methods, and directions in order to progress as much as we could in the research. I learned a lot from him, from his professional nature and his understanding, he always inspired me. In addition to the scientific discussions and exchanges that would last for hours in his office or elsewhere, I also enjoyed being with him because on a personal level he was a very good person. This will always remain special moments in my memory. I am extremely grateful to him not only for never letting me down or losing the track but also for his continuous support, for being always helpful, for his solidarity in the difficult times, and for doing his best to provide me with better conditions during my stay in Italy. I must say I was fortunate enough to be under his guidance. This thesis would not have been possible without you, *Grazie Mille Prof!*

I express my gratitude also to my Tunisian supervisor **Prof. Wael Dghais** for his close follow-up of this thesis, the scientific support he gave me during this work, his patience, and his constant encouragement. His expert advice, discussions, and knowledgeable perspectives on the issues of my doctoral research have been very important to me. Thank you very much.

I also would like to express my sincere gratitude to my Tunisian supervisor **Prof. Hamdi Belgacem** who gave me the opportunity to work in this field, for his encouragement, and trust, and also for helping me solve administrative problems. Finally, I am thankful for his listening, his scientific and unconditional support, and his human qualities.

I express my gratitude to **the Members of the Jury** for having done me the honor of agreeing to evaluate my thesis.

The past three years have been sometimes joyful, sometimes difficult, but in each of these moments, I could count on the unwavering support of many individuals, colleagues and friends. This research has been conducted in parallel with the PhD work of my friend Fakhreddine Zayer, I thank him for the pleasant collaboration. I owe a big thanks to my colleagues at the EμE laboratory of the FSM for the good time and memories in the laboratory and also for their useful support. My sincere thanks to all Professors and friends of the LEMNDE and LAMI of the DIEI Department of the University of Cassino, for many aspects and kind friendship. I am extremely grateful to my besties Sarah Sibilia, Gennaro Di Mambro, Gianmarco Trezza, and Guilia Di Capua for their love, and for being part of my life also outside of work, you have made this period one of my best memories that I will never forget. Thank you all for your sympathy and simply for the pleasure I had in dealing with all of you on a daily basis.

I am so grateful to my Tunisian friends, thank you for being so close to me and sharing an amazing time together in Italy.

Finally, from the bottom of my heart, I would like to thank my parents. Mum and dad, everything I am and everything I have achieved in my life is due to you. I am grateful for your love, support, and all the sacrifices you have made for me. To my dear brothers and sisters, a big thanks for their good humour, endless love and encouragement. My life is more beautiful with all of you! My deep thanks to my dear friend Chiheb for his constant encouragement and kindness and for his persistence in being close to me.

Thank you to all the people I didn’t mention who were directly or indirectly involved in this work.

ABSTRACT

The high demands of reducing power consumption for electronic applications and decreasing the current and voltage range have increased the technological development of the non-volatile Resistive Random Access Memory (RRAM) based on Memristive devices. In this thesis, a full 3D electrothermal model is adopted to study the thermal and signal integrity of a 1Diode-1Resistor RRAM crossbar array. In fact, the 3D integration suffers from two main issues which are the voltage drop along the interconnects and thermal crosstalk between the memory cells. Several solutions are investigated based either on new biasing schemes, new materials (Nickel (Ni), Copper (Cu), and Carbon nanotubes (CNT)), and new architectures integrations (reverse architecture (1D1R-1R1D) and complementary resistive switching (CRS)). Based on these proposed structures with the choice of the new materials and the bias management, the electrothermal performances show the benefits of solving the issues related to the large-scale monolithic 3D RRAM integration. All the results are compared with the reference architecture (1D1R) and also the physical model is validated against other models in the literature. Indeed, the second approach of the thesis is to study the electrothermal behavior of macroscopic graphene strips (Graphene Nano-Platelets (GNPs)) as a heater element which is the Thermistor. Where an equivalent electrical resistivity is studied, by means of models and experimental characterization based on three different materials with different percentages of graphene nanoplatelets. To this end, the electrical resistivity shows a negative temperature coefficient in a wide temperature range [-40, +60] °C, which allowed these materials to be used for thermistor and temperature sensor applications.

Keywords: 3D RRAM crossbar, electrothermal modelling, signal and thermal integrity, 1D1R-1R1D, CRS, CNT, Thermistor, Electrical conductivity, Graphene Nano-platelets, NTC materials.

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER I

CHAPTER II

CHAPTER III

CHAPTER IV

CHAPTER V

LIST OF TABLES

INTRODUCTION

The semiconductor industry is a high-tech hub. For the past fifty years, microelectronic products have invaded our lives, with massive penetration into health, safety and identification, communications, education and virtually every aspect of human life.

Since the emergence of the CMOS industry in the 1960s, the microelectronics industry has been continuously evolving, seeking to remain attractive in the personal and corporate markets. The size and technology node of the transistors has drastically shrunk to nanometer scale in order to increase the density on a chip to reach a robust a low power computing. Where the increase in power, predicted by Intel co-founder Gordon Moore in 1965 (Moore, 2006), has created many challenges such as the need to dissipate high heat densities and is today limited by both technological tools and processes and by physical phenomena becoming predominant when small dimensions are considered (quantum phenomena).

Thermal control then became a key point in the design of electronic equipment. The operating characteristics of the components and the reliability of the systems depend heavily on temperature. Miniaturization and increased switching frequencies lead to increasingly high dissipated power densities. These now reach values in the order of 400 Wcm^{-2} in power electronics: the thermal behavior has therefore become one of the main factors limiting the switchable power. A fine and fast modeling tool of heat transfer in electronic power components would therefore be very useful for optimizing their structure from a thermal point of view, minimizing their operating temperature for a given dissipated power. Indeed, when developing and designing integrated circuits, the thermal aspect is crucial for their proper operation.

This Thesis deals with the electro-thermal modelling of innovative devices whose operating principles rely on the interaction between their electrical and thermal responses.

The first application is a memristive memory, a new technology consisting of a combination of memory and resistance, that has set as a promising candidate for future “beyond CMOS” high integration density memory devices and low power consumption. Specifically, the Thesis analyzes the Resistive Random-Access Memory (RRAM) device, consisting of an oxide layer of a few nanometers deposited between two metal electrodes and which may have two non-volatile states depending on the voltage applied to its terminals: the highly resistive or HRS state and the low resistive or LRS state.

The second application analyzed in this Thesis is an innovative thermistor, and specifically a novel resistive element realized by commercial graphene material, the so-called Graphene Nano-Platelets (GNPs). The final application foreseen for such a device is the heating systems for de-icing and anti-icing purpose for aircraft wings.

In both cases, the general goal has been that of assessing a reliable and accurate electrothermal model, and using it to characterize their performance, optimize their design and investigate alternative solutions.

The Thesis is organized as follows.

- The first chapter presents the context of the study, the problems and objectives and discusses the main generalities related to the thermal management of electronic devices, in particular the effect of temperature on electronic fields. Heat dissipation and heat transfer are discussed. A general overview on the proposed applications is also provided: Memristors and Thermistors are presented, by explaining their characteristics and modes of operation.
- The second chapter is a review of current and emerging memory technologies. In this context, RRAM memories are presented as a potential candidate and the first applications of the memristor concept to memory. This chapter presents the operating principle of such a type of resistive memories such as complementary resistive switching. The issues related to signal and thermal integrity associated to RRAM integration into crossbar architectures are discussed, with reference to a first case-study.
- The third chapter presents the electrothermal model formulation and the main techniques proposed for its solution. The numerical implementation of the

model by using a Finite Element solver is discussed, with reference to the memristor application. In particular, the physical models for the material properties are discussed, as for instance the electrothermal model of the conductive filament of the memristor in the high and the low states of the memory (SET and RESET).

- The fourth chapter presents the results of a signal and thermal integrity analysis carried out on arrays of RRAM memories, comparing different architectures (conventional 1D1R, inverted 1D1R-1R1D, and complementary CRS), different material choice (nickel, copper, and carbon nanotubes) and different biasing schemes. The best design solutions are highlighted, to mitigate and even resolve the signal and thermal integrity issues, such as voltage drop and thermal crosstalk.
- The fifth chapter is devoted to the analysis of a new class of thermistor, realized by means of macroscopic Graphene Nanoplatelets (GNP) strips. These commercial films are proposed as heating elements via Joule effect. Three different types of materials have been analyzed, with different percentage of graphene nanoplatelets. The equivalent electrical resistivity model is derived from the joint use of experimental data and of simulation results obtained by means of a full-3D numerical electrothermal model in a wide temperature range (-40, +60) °C. The model of the thermistor is experimentally validated.

Main novel contributions of the Thesis.

- This work provides an answer to many open questions about the accurate modeling of the oxide-based RRAM devices. Indeed, an improved model of the conductive filament reversible formation and dissolution is derived and implemented in the global electrothermal model.
- A detailed electrothermal analysis of the RRAM crossbar structures highlights the sources of signal and thermal integrity issues (voltage drop along the interconnects and thermal crosstalk between the memory cells) and quantifies the impact of such issues. Possible solutions to these problems are here

thoroughly investigated, based either on new biasing schemes, novel architectures, and novel materials, including innovative nanomaterials.

- A procedure to identify the main parameters of the graphene heater (thermistor) is here assessed, which provides the temperature-dependent electrical resistivity by jointly using the results of experimental characterization and numerical modeling. Experimental validation of the resistivity model is provided, where the Joule effect is used as the mechanism of heat source.
- A negative temperature coefficient of the electrical resistivity is demonstrated, as a result of using graphene-based materials for realizing the thermistor.

The main results of the electrothermal analysis of the RRAM memory devices are published in the following paper:

- Lahbacha K, Zayer F, Belgacem H, Dghais W, Maffucci A. "Performance Enhancement of Large Crossbar Resistive Memories with Complementary and 1D1R-1R1D RRAM Structures," *IEEE Open Journal of Nanotechnology*. 2021; Vol. 2:111-9. https://doi.org/10.1109/OJNANO.2021.3124846.

The main results of the electrothermal analysis of the GNP thermistor are published in the following paper:

- Lahbacha K, Sibilia S, Trezza G, Giovinco G, Bertocchi F, Chiodini S, Cristiano F, Maffucci A., "Electro-Thermal Parameters of Graphene Nano-Platelets Films for De-Icing Applications," *Aerospace*, 2022; Vol.9(2):107. https://doi.org/10.3390/aerospace902010.

Chapter I : Electrothermal Behavior of Electronic Systems

Chapter I

I.1 Introduction and context

This chapter aims to set the context for this work and to present in detail the issues in order to support the interest of the studies carried out and to clearly define the research to be carried out.

First of all, the microelectronic context is dictated by the guidelines derived from the famous “Moore’s Law”: miniaturization and diversification. The evolution of this market requiring the addition and discovery of new features. Indeed, it becomes necessary to integrate passive components in circuits and more and more new materials such as Memristors and Thermistors devices. Next, these new applications that use more and more integrated materials in the components such as Carbon Nanotubes and Graphene will be also described. The integrated dielectrics and their properties will also be presented. Finally, the issues, including the need to characterize and present these new components and their characteristics. Once these issues have been defined, the objectives of this thesis work can be set out as well as the material resources made available or to be developed.

The “roadmap” is the general outline of the future of a selected area which is made up of the collective knowledge of researchers in that area. In high-tech sectors such as nanoelectronics, roadmaps are very useful and have an advantage in improving the relationship between theoretical and practical research, providing alternative drivers for future research patterns, and coordinating efforts to address key technical challenges. In this context, we will describe the Moore's Law which was expressed in 1965 in "Electronics Magazine" by Gordon Moore, an engineer from Fairchild Semiconductor, one of the three founders of Intel. Noting that the complexity of electronic circuits doubled every year at constant cost since 1959, the date of there he predicted that this growth would continue. This exponential increase was quickly named Moore's Law or, considering the later adjustment, first Moore's Law. Then, in 1975, Moore re-evaluated his prediction by indicating that the number of transistors in microprocessors on a silicon chip doubles every two years (It’s the “More Moore” aspect). Although this is not a physical law but just an empirical extrapolation, this prediction turned out to be surprisingly accurate. Between 1971

and 2001, the density of transistors doubled every 1.96 years. As a result, electronic machines became cheaper and more powerful. Figure I.1 shows the evolution of Intel® processors as a function of time and in comparison, with Moore's statements.

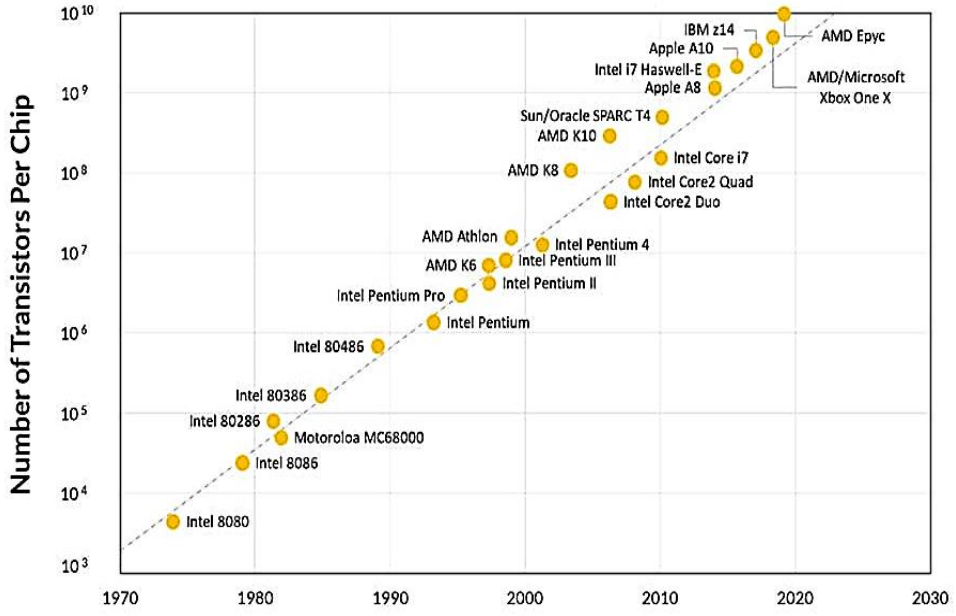


Figure I-1 Chart: Moore's Law: The number of transistors packed into microchips.

Moreover, as shown in Figure I.1, Moore's Law also dictates the cross-functional evolution of the microelectronics industry through a diversification of functionalities: "More Than Moore". By integrating passive components, sensors or biochips in the "Back End Of Line" (BEOL), electronic, medical or complete instrumentations functions can be realized within the same circuit. The space saving obtained thanks to the miniaturization of transistors makes it possible to increase the computing power for the same surface area and thus to use these computing possibilities to integrate these new functions (image sensors, pressure sensors, accelerometers, etc.). Figure I.2 summarizes the two aspects of Moore’s Law.

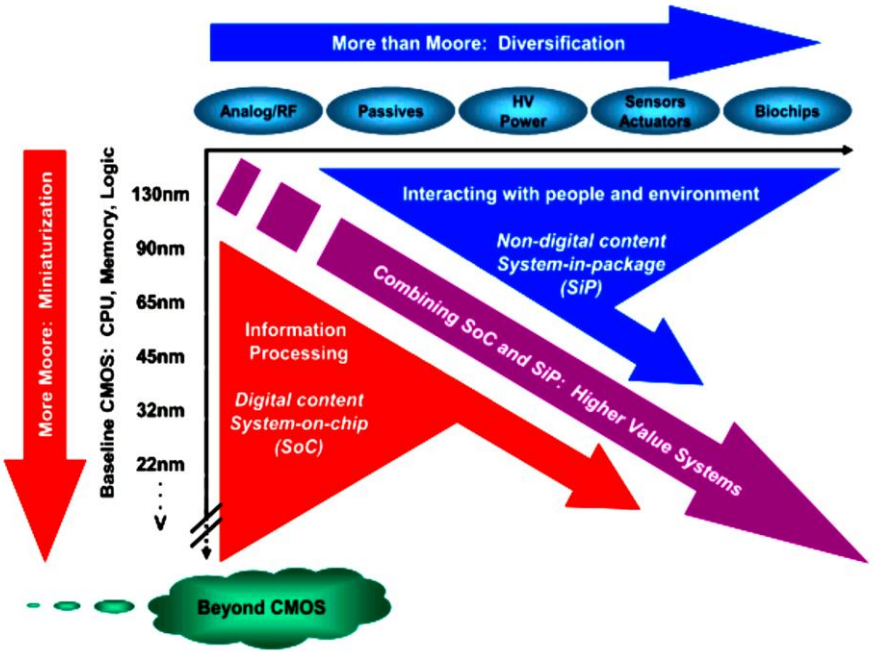


Figure I-2 Trends and challenges towards miniaturization and diversification of circuits.

It seems that the first roadmap for semiconductors was born out of Moore's principle that the computing power of chips was increasing exponentially over time (Moore,1965; Moore,2006). This means that semiconductor manufacturers need to schedule regular upgrades to improve chip performance. The main performance is focused on decreasing the size of the integrated circuits by improving and optimizing the existing circuits.

As the transistor is one of the basic components of electronic devices and the basic design of integrated circuits (ICs), its reduction has increased the performance of ICs and the cost per device function has decreased accordingly. Physical and technological limitations such as undesirable small current behavior, quantum effects, design complexity and power dissipation are presented as drawbacks for further development of microelectronics based on conventional circuit scaling. Indeed, the high investment costs for conventional CMOS and technological design issues can reduce the barriers to entry for alternative device concepts.

Over the past few years, Moore's low has slowed down, particularly as miniaturization approaches physical limits. This is evidenced by the growing

difficulties of the manufacturer who best embodies it, Intel, the world's number one chip company, to respect it. Its generation of 14 nm chips was launched one year late on the initial schedule and 10 nm late by more than 3 years. And his next generation of 7 nm is about to experience the same setbacks. This has motivated researchers to study new devices for logic and memory, new integration processes, such as three-dimensional monolithic integration, and much more energy-efficient new computer architectures to perpetuate the trends of Moore's Law (Hoefflinger,2011; Theis,2017). Indeed, the following section presents the basic concepts related to memristive devices and provides the basic operating characteristics of this new electronic device. These concepts include a review of new non-volatile memory technologies and their basic definitions.

I.2 Thermal management of electronic devices

All areas of electronics to varying degrees are affected by thermal problems. Electrical machines, motors and alternators, given the power involved and the heating due to losses, were the first devices studied from a thermal point of view. For many years, similar studies have been carried out on microelectronic components, and in particular on semiconductor components. Some more specific works concern high temperature electronics for applications such as oil research for example. The first works relating to the thermal phenomena used in microelectronics are rather old and few (Wójciak,1997). In recent years, with the development of simulation tools, the need for modeling has increased significantly. We are witnessing a very significant increase in work in this field.

During the development and design of integrated circuits, the thermal aspect is crucial for their proper functioning. The problem of overheating of the junction remains a major obstacle in front of the most sought-after performance of the electronic systems: the increase of the speed of operation and the miniaturization of the components. In both cases, this results in an increase in the temperature of the electronic components caused respectively by the accumulation of a thermal residue from one cycle to another and the increase in the dissipated power density. Heat is an inevitable consequence of each electronic device and it must be minimized or

managed. Several research projects have been carried out to overcome thermal problems in electronic components. The first research work focused on the choice of materials and geometry and on the dimensions of radiators (i.e., thermal dissipator) on which the electronic power components must be attached depending on the power dissipated in these components and the surrounding environment.

The challenges tied in finding the heat-optimal positions lie in the complexity of solving the heat transfer equation with boundary conditions applied to several contours and surfaces and in the precise evaluation of dissipated power in semiconductors. To overcome the second difficulty, the model chosen to represent each semiconductor component involved must describe its behavior according to the current and its temperature. An adequate modelling of each component is then necessary.

The analytical solution of the heat transfer equation, which is reduced to the permanent Poisson equation requires considerable computational resource (e.g., CPU and memory). This is often done by numerical solution or by reducing the resolution of the thermal problem to that of an electrical problem. However, the assimilation of the thermal problem to that of an electrical network gives, in general, erroneous results since in such a network each element ensures the transfer of heat in a certain direction which does not really reflect the propagation of heat which is done naturally in all three dimensions.

Numerical solution of thermal problems reported in several publications are based on the finite difference method or finite element method. Some thermal optimization algorithms, in this case, the simulated sound annealing method and that of partial networks which are based on the use of the Monte-Carlo method, were established and applied on electronic boards and hybrid circuits.

A thermal optimization algorithm shall, at each iteration corresponding to a given configuration of component positions, take into account the variation in heat sources due to variations in component parameters due to changes in temperature and the change in boundary conditions due to changes in the geometry of the heat transfer medium. Indeed, components whose characteristics depend on temperature interact and the behavior of the circuit can be greatly influenced by thermal couplings up to

the sometimes malfunction. Thermal analysis at the same time as electrical analysis is, therefore, essential. In these approaches, this work is based on two applications, the Memristor and the Thermistor in which are based on electrothermal modeling and the effect of the temperature and the overheating is studied in the next chapters.

I.2.1 Effects of temperature on IC operating conditions

Increasing the temperature of an active device typically changes its electrical parameters such as gain, leakage and compensation. These parameter variations with temperature are well documented and incorporated into most circuit simulators. Most circuit designers are aware that the leakage current in active devices (diode, MOS transistor) approximately doubles each increase by 10°C. This reduces the effect of leakage currents. If the temperature of an active device increases too much, it will exceed the manufacturer's specifications and impair the normal operation of the integrated circuit.

The change in temperature of passive devices typically changes their values. For example, film resistors have temperature coefficients ranging from the range of several parts per million per degree °C of difference to several hundred. In practice, these changes in electrical parameters are not typically desired. If the temperature increase is high enough, the active or passive device being heated can permanently degrade, even break completely or deform in a plastic way. Therefore, a good thermal design should minimize any temperature increases and especially the local thermal gradient. As a designer one cannot have control of changes in the environment of the integrated circuit, but we have control of the device's spatial auto heating (distribution of the dissipated power density).

I.2.2 Heat dissipation and heat transfer mechanisms

In recent years, microelectronic heat dissipation analysis has become increasingly important due to the ever-increasing density of components on substrates whose dimensions are progressing in reverse. Thermal dissipation problems are of great importance in the IC enclosure. Not to consider them and not to control them is to manufacture modules that do not offer all the guarantees of operation and reliability.

Poor or insufficient heat removal can adversely affect the proper functioning of the system. Heat is the result of an electrical power developed by active and passive elements. The thermal effects may be manifested in different ways, by temperature drift of the components leading to significant variations in electrical performance, or by a weld failure connecting the component to the substrate due to different dimensional variations for each of them, resulting in either partial failure or total failure.

In electronics, power dissipation is the process by which an electronic or electrical device produces heat (energy loss or waste) as an undesirable derivative of its primary action. In other words, it is usually a measure of how much heat is being released due to inefficiencies in the circuits. Furthermore, the power dissipation in resistors for example is considered a naturally occurring phenomenon. The fact remains that all resistors that are part of a circuit and have a voltage drop across it will dissipate electrical power. In addition, this electrical power converts into heat energy, and therefore all resistors have a nominal (power) rating. Also, the rated power of a resistor is a classification that sets the maximum power that it can dissipate before reaching a critical failure.

In addition, heat transfer within a system occurs only if there are temperature gradients between the different parts of the system, which implies that the system is not at thermodynamic equilibrium (the temperature is not uniform throughout the system). During the transformation of the system to a state of final equilibrium, the temperature will change in both time and space.

Conduction is defined as the mode of heat transmission (or internal energy exchange) caused by the temperature difference between two regions of a solid, liquid or gaseous medium or between two media in physical contact (temperature gradient in a medium). In most cases, conduction is studied in solid media, since in fluid media (i.e., liquid or gaseous), there is often coupling with a displacement of material and thus convection mechanism. Conduction is the only mechanism involved in heat transfer in a homogeneous, opaque and compact solid.

Conduction is carried out from near to far:

- If one heats the end of a solid there is progressive heat transfer.

- If we cut the solid, we stop the transfer.

The conduction theory is based on the Fourier's law where the flux $q\ (W/m^2)$ is proportional to the magnitude of the temperature gradient and opposite to it in sign.

$$q = -k\nabla T \qquad (I.1)$$

Where $k\ (W/m.K)$ is thermal conductivity of the medium.

Convection is the mode of transmission that involves the displacement of a gaseous or liquid fluid (flux) and exchange with a surface that is at a different temperature. There are two types of convection, forced convection due to external mechanical actions (pump, fan, etc…) and natural convection (or free convection) in which the movement of the fluid is created by differences in density, themselves caused by differences in temperature. Indeed, convective heat transfer is done in two steps:

- Fluid movement: the faster the fluid moves, the more efficient the heat transfer.
- Diffusion, which is the energy transfer due to the random movement of molecules.

The convective exchange between a hot surface (at temperature T_s) and a fluid (at temperature T_∞) is given by the following Newton law:

$$q = h(T_s - T_\infty) \qquad (I.2)$$

Where q is the convective flux density and h is the convective heat transfer coefficient.

Heat transmission by radiation is the exchange of heat by the radiation of a hot body on a cold body. The simplest example is solar radiation. Thermal radiation is the mode of transmission through which heat passes from one high temperature body to another colder body without the need for material support. It is therefore the only mode of heat transfer that can be propagated in the vacuum. Thermal radiation differs from other electromagnetic waves, such as microwave waves for example, only in its origin temperature. Indeed, each body radiates as long as its temperature is different from 0K. Thermal radiation is a surface phenomenon where the maximum

flux density q emitted by a surface is given by Stephan-Boltzmann's law at absolute temperature T_s :

$$q = \sigma(T_s^4 - T_\infty^4) \quad \text{(I.3)}$$

Where $\sigma = 5.6704.10^{-8}\ W/m^2K^4$ is the Stefan-Boltzmann constant.

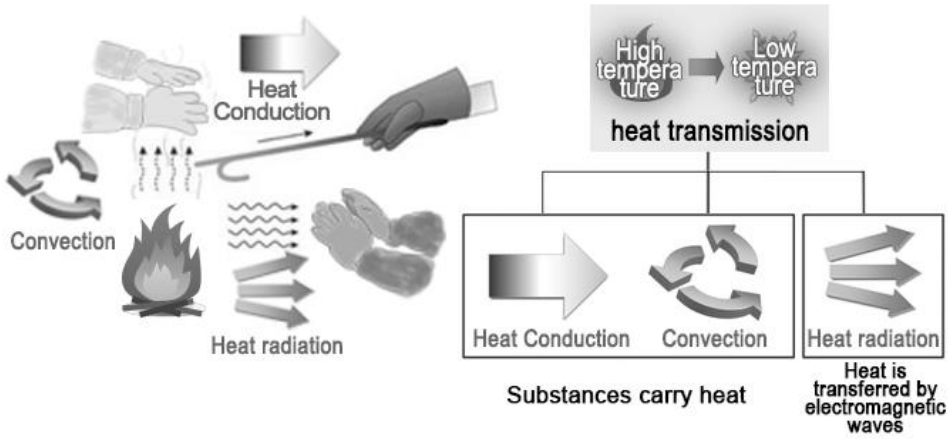


Figure I-3 Different modes of heat transmission.

I.2.3 Cooling system

The cooling or thermal management issues are facing critical challenges with the continuous miniaturization and rapid increase of heat flux of electronic devices. In order to solve the thermal problems that can affect the proper functioning of the electronic circuits, effective cooling is used. On the one hand, the cooling system must be compatible with the environment in which it will be used. On the other hand, cooling systems must be subject to certain limitations such as thermal and mechanical limitations.

The cooling solutions of the electronic systems constitute a very varied and heterogeneous toolbox. Different options are available depending on the characteristics of the system, the power to be dissipated and the cost of implementation. All these thermal optimization options on the design and architecture side are also necessary and complement the technological solutions. In the new thermal design approach, these solutions will be implemented from the start of product development.

I.2.4 Thermal resistance

An analogy between heat conduction and electrical conduction simplifies the analysis. In stationary mode, it is based on the concept of thermal resistance. In this analogy, the heat flow q is represented by the electric current. A temperature difference ΔT is analogous to a voltage drop. We can then define a thermal resistance R as:

$$R = \frac{\Delta T}{q} \qquad \text{(I.4)}$$

Although this analogy applies only to conduction transfer, this definition can be generalized to all modes of transport. In the same way as for electrical systems, the thermal resistors corresponding to the elements on the heat removal path can be set in series or in parallel in order to calculate the overall thermal resistance of the assembly. This total resistance (I.4) is often defined according to the maximum temperature of the device T_{jmax} (maximum junction temperature) and the ambient temperature Ta:

$$R_{th} = \frac{T_j - T_a}{q} \qquad \text{(I.5)}$$

I.3 Thermo-electrical applications: memristors and thermistors

I.3.1 Memristors: fundamentals

The term «memristor» for memory resistor (memory resistance) refers to a 2-terminal passive introduced in 1971 by Leon Chua in his article (Chua,1971), where it is described as the fourth basic element of an electronic circuit (Figure I.4). To affirm this, Chua lists the achievable doublets with the two sizes used for electronics: the voltage (v), the current (i), as well as their temporal integral, the flow (φ), and the charge (q). He notes that doublets (φ, v) and (q, i) form two of the laws of electromagnetism and that doublets (v, i), (q, v) and (φ, i) respectively define resistance, capacitance, and inductance. The last doublet (φ, q) has no

correspondence. It is this doublet that generates the definition of the memristor which it separates into two cases. The case of the controlled memristor in charge gives:

$$V(t) = M(q(t)) \cdot i(t) \tag{I.6}$$

Where

$$M(q) = \frac{d\varphi}{dq} \tag{I.7}$$

The case of the flux-controlled memristor:

$$i(t) = W(\varphi(t)) \cdot v(t) \tag{I.8}$$

Where

$$W(\varphi) = \frac{dq(\varphi)}{d\varphi} \tag{I.9}$$

Here, the parameters M(q) and W(φ) are indicated as incremental memristance and incremental memductance, respectively, they have thus, similar units to resistance and conductance.

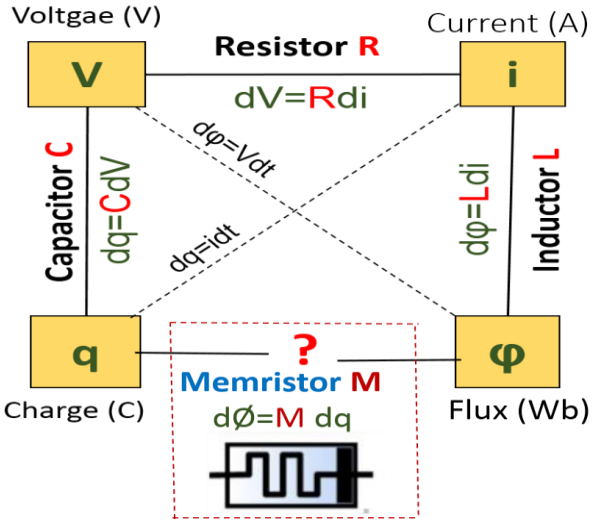


Figure I-4 The relationships between the four elementary passive components: resistance, capacitor, inductance and memristor.

In 2008, the HP laboratory published an article on a memristor manufactured by inserting a TiO_2 layer between two layers of Pt (Strukov,2008). In this article, a physical model for the memristor is presented. This consists of two distinct zones, a doped and a non-doped, which, when they occupy the total length of the device, correspond to the two extreme resistances R_{OFF} and R_{ON} of a memristor. The variation in the size of the doped zone w changes the total resistance of the device by weighting the importance of each zone (Figure I.5). The following equations are derived from these assumptions:

$$M(q) = R_{OFF}\left(1 - \frac{\mu_v R_{ON}}{D^2} q(t)\right) \tag{I.10}$$

$$w(t) = \mu_v \frac{R_{ON}}{D} q(t) \tag{I.11}$$

with w the length of the doped area, D the total length of the device between the two metal contacts and μ_v the average mobility of ions in the active layer.

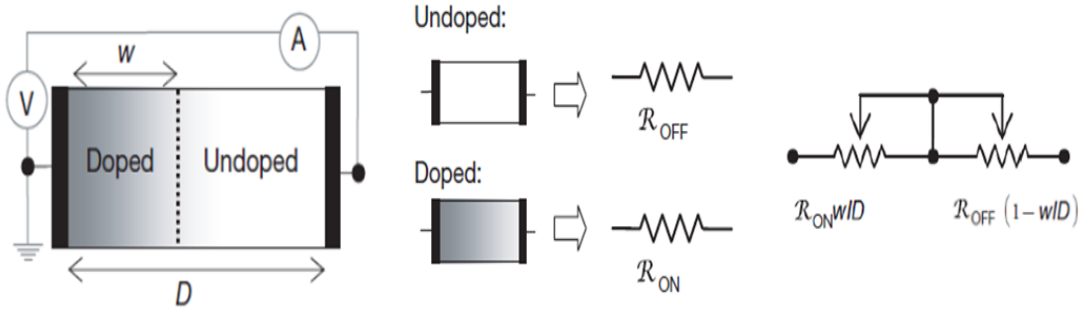


Figure I-5 Physical model of a memristor obtained by varying the length of a doped zone in a doped/non-doped type device. Varying the length of the doped region w is equivalent to weighting the importance of R_{OFF} and R_{ON} resistors (Strukov,2008).

This first model will be criticized mainly for its simplification which ignores certain physical properties. However, it makes it possible to obtain the first simulations of this phenomenon and to gather under the same name quite different non-linear effects such as resistive memories or negative differential resistance effects (NDR) (Figure I.6).

In nanoscale devices, small voltages can produce a huge electric field, which in turn can produce significant nonlinearities in ionic transport. The right side of equation (I.10) is multiplied by a window function $w(1-w)/D^2$, which corresponds to a non-linear drift when w is close to zero or D as shown in Figure I.5. In this case, the switching event requires a much higher charge (or even a threshold voltage) for w to approach either of the limits. Thus, switching behavior is basically binary because the on and off states can be kept much longer if the voltage does not exceed a specific threshold.

The nonlinearity can also be expected in electronic transport, which may be due, to tunnelling at interfaces for example. Indeed, the hysteresis behavior defined above remains basically the same, but the I-V characteristic becomes non-linear.

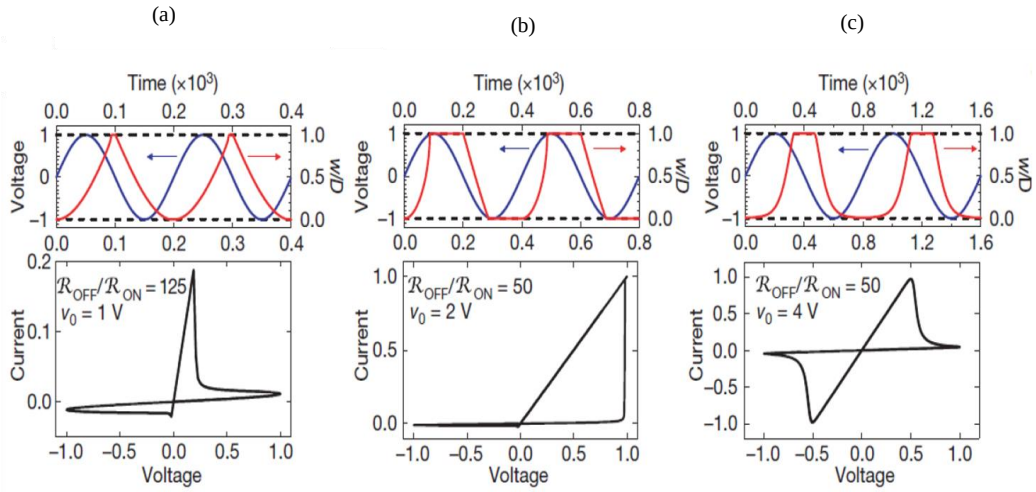


Figure I-6 Simulation of memristive devices using equations I.5 and I.6 (Strukov,2008). The blue curve corresponds to the voltage stimuli and the red to the corresponding normalized variation of w/D. a) For a "dynamic" negative differential resistance. b) For resistance switching. c) For a phenomenon governed by a non-linear displacement of ions.

Williams and Chua assumed that all memory resistive devices are classified as memristors, regardless of the physical and physical operating mechanisms (Chua,2019; Kim,2012). These devices have a distinctive “footprint”, characterized by a pinched hysteresis loop. This hysteresis loop is limited to the first and third quadrants of the V-I plane, as shown in Figure I.6c, which changes its contour shape

according to the amplitude and frequency of the input voltage/periodic current source of the sinusoidal type (Chua,2019).

The discovery of the memristor and the originality of the production of resistive memories based on TiO_2 is one of the major arguments presented in 1968 (Argall,1968), in which the possibility of creating a thin anodized titanium dioxide film with three distinct conductivity levels is described. Several types of resistive memories existed in the literature long before the 2008 HP article. Examples include nano-ionic resistive memories (Waser,2009) or those using phase change materials (Raoux,2008).

It should also be noted that, at present, the difference in the use of the terms "memristors" and "resistive memories" depends on the application. The term resistive memory is generally used to refer to digital memory applications. The word memristor is rather used when the dynamic and analogical aspects are important.

I.3.2 Thermistors: fundamentals

The thermal sensor refers to the number of devices most frequently used. Its main purpose is to perceive the temperature and convert it to the signal. There are many different types of sensors. The most common of these are thermocouples and thermistors. A thermistor is a temperature-sensitive element consisting of sintered semiconductor material with large resistance variations proportional to small temperature variations. Thermistors generally have a positive or negative temperature coefficient, PTC and NTC, respectively (the symbol is shown in Figure I.7), which means that the resistance of the thermistor decreases as the temperature increases in the case of NTC.

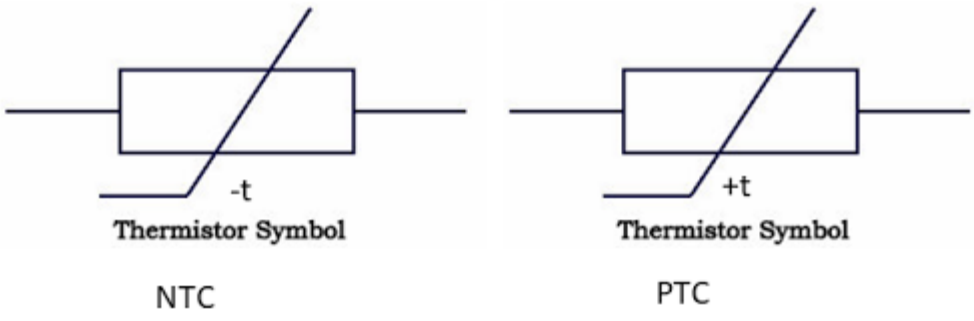


Figure I-7 NTC & PTC thermistors Symbol.

It found great use in electrical engineering, since it has a special control over the temperature regime. It is very important to have their presence inexpensive equipment, computer, and industrial techniques. Used to effectively limit the starting current, it is limited to the thermistor. This changes its resistance depending on the resistance of the current passing it, due to the heating of the device.

Thermistors are generally sensitive and have different thermal resistance. In the poor conductor, the atoms that make up the material tend to be located in the right order, forming long rows. When the semiconductor is heated, the number of active loads supports increases. The most available load supports, the greatest conductivity is the material. The resistance and temperature curve always shows a non-linear characteristic as shown in Figure I.8, in other words the thermistor temperature characteristic curve shows the temperature response to the change in resistance which is the thermal sensitivity offered by the change in resistance as the temperature changes (NTC and PTC). The thermistor works best in the temperature range of -90 to 130 °C.

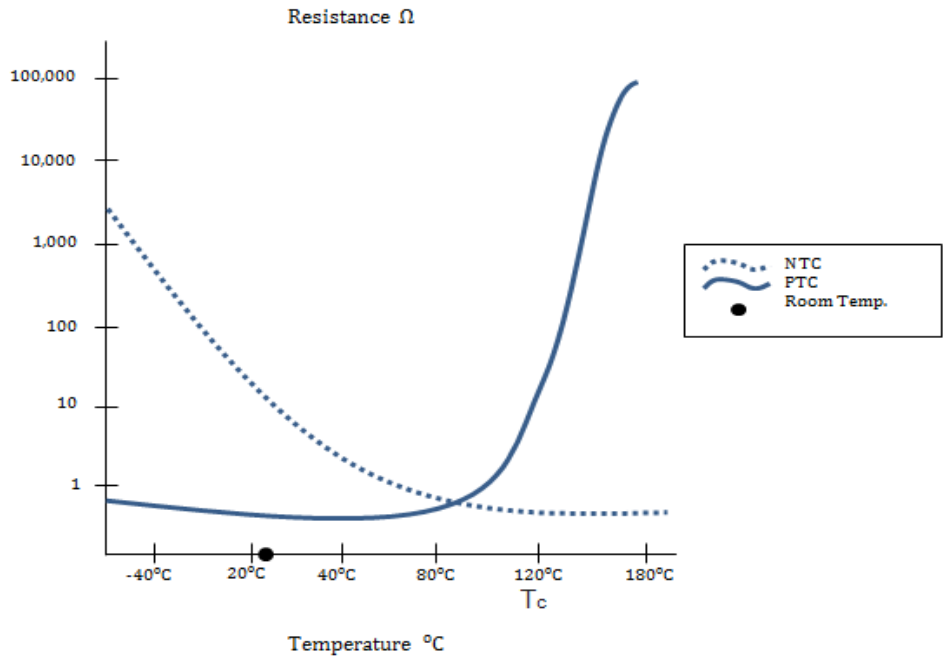


Figure I-8 The thermistor temperature characteristic curve, for NTC and PTC.

The electron, pushed by the applied electric field, can be moved to relatively long distances before colliding with an atom. The collision slows its movement, so that

the electric "resistance" will decline. At a higher temperature, the atoms are moved more and when a specific atom is somewhat deviated from its usual 'parked' position, it is very likely to face a passing electron. This "deceleration" is manifested in the form of an increase in electrical resistance.

When the material is cooled, the electrons settle on the lowest valence shells, become susceptible and, as a result, move less. At the same time, resistance to the movement of electrons from one potential drop to another. When the temperature of the metal increases, the resistance to metals in the flow of electrons increases.

NTC thermistors are widely used as starting current limiters, self-driving cornering protection and self-regulating heaters. Typically, these devices are installed parallel to the AC circuit. They can be found everywhere: in cars, aircraft, air conditioning, computers, medical equipment, incubators, hair dryers, electrical outlets, digital thermostats, portable heaters, refrigerators, ovens, stoves and other kinds of peripherals.

There are thermistors with a resistance (at 25°C - temperatures at which the resistance of the thermistor is generally determined) of one ohm to ten meg and more. The resistance depends on the size and shape of the thermistor, however, for each specific type the resistance rates may differ from 5 to 6 orders of magnitude, obtained by a simple change in the oxide mixture. When the mixture is replaced, the type of resistance temperature dependence (R-T curve) is also changed and the stability changes at high temperatures. Fortunately, thermistors with a high enough strength to use them at high temperatures also have a higher stability. Cheap thermistors generally have fairly large parameter tolerances. For example, allowable resistance values at 25°C range from ±20% to ±5%. At higher or lower temperatures, the variation in parameters increases even more. For a typical thermistor with a sensitivity of 4% per degree Celsius, the corresponding tolerances of the measured temperature range from approximately ±5°C to ±1.25°C to 25°C.

All thermistors are made from a combination of metals and materials based on metal oxide with a popular and well-known high-temperature resistance coefficient. This coefficient is much, several times higher than that of other metals. The principle of thermistor operation is based on the basic correlation between metals and

temperature. They are made from semiconductor compounds, such as oxides, silicates, nickel, manganese, iron, copper, etc., can even feel a small change in temperature. Our study is based on Graphene Nanoplatelets, which is detailed in chapter V.

The design of the thermistor is quite simple. A piece of semiconductor fixes the shape of a thread, bar, rectangular plate, ball or other shape. On opposite parts of the thermistor, two exits are mounted. The magnitude of the ohmic resistance of the thermistor, as a rule, is substantially more than the amount of resistance of other circuit elements and, above all, depends considerably on the temperature. Therefore, when the current flows, its value is mainly determined by the size of the ohmic resistance of the thermistor or finally its temperature. With an increase in the temperature of the thermistor, the current in the diagram increases and, on the contrary, decreases with a decrease in temperature. Heating the thermostat can be carried out by heat transfer from the environment, heat release in the thermistor itself when the electric current is passed or, finally, by using special heated windings. The heating method of the thermistor is directly associated with its practical use.

I.4 Conclusions

- The chapter presents the introductive part of the thesis where mentioned the roadmap of the semiconductors and Moore’s law and the context of our electrothermal applications.
- This chapter has allowed us to highlight many issues related to the thermal management of electronic devices such as the effects of temperature on the integrated circuits, the heat dissipation effects, and the cooling system.
- The heat transfer mechanisms (conduction, conductive, and radiation) are described as well as the thermal resistance.
- The criteria on the characteristics of a unipolar memristor are defined to allow its integration in crossbar arrays. We then developed the details of the thermistor device, its operation, and its physical properties.

- This chapter has also contributed to the understanding of switching mechanisms through a physical modeling approach of phenomena during SET and RESET operations of memory cells.

Chapter II : Memristor As A Memory

Chapter II

II.1 Introduction

In order to improve digital systems, the issue of non-volatile memory presents the main topic. Given the current need to manage and store more and more information and the difficulty of continuing to miniaturize the CMOS technology (Iwai,2015), research is focusing on new technologies for the future such as the memristor. Among its applications, which are called emerging memories, are the resistive memories, which are the subject of a great deal of research in the literature. Different paths are studied in order to find the component of tomorrow and in particular, the one that will interest us, the Resistive Random-Access Memory that we find under the name in the literature is RRAM. This abbreviation will be used in this thesis to qualify resistive memories in general, but we will see that under this name a multitude of different devices is hidden depending on their structures.

This second chapter explores the state of the art in non-volatile memory technologies. It then includes a brief history of the memristors detailing the history and detailing the different types of current and emerging memory devices. We will then focus on the RRAM in particular the current knowledge in terms of operation, the performance of these memories, and modes of operation. We will observe their architecture, their composition, and the type of operation they can adopt, as well as the issues and the limits of the arrangement of memory devices in crossbar matrices. In addition, complementary memory devices (CRS) are presented and positioned as a solution to the leakage currents limiting the development of crossbar matrices, and in the end, the case study of our devices are presented.

II.2 Classification of memories

Over the past 40 years, the integrated circuits market has experienced exceptional growth. In 2007, this market represented $256 billion (Chang,2007). Memory technologies share a significant part of this market (~30%). Ideally, the memory technology should be non-volatile and meet the 10-year retention criteria. In addition, it must offer high capacity (Gb), fast access time (a few ns), good endurance (~ 10^9-10^{12} write/erase cycles), energy consumption (100 mW in

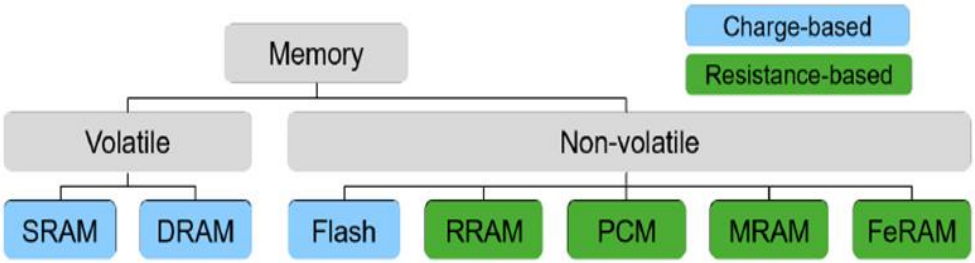


Figure II-1 Classification of current and emerging memory technologies. (a) Overview of established charge-based memories (blue) and new resistance-based non-volatile memories (green).

operation), and competitive manufacturing costs ($5/Gb) (Burr,2008). It must also be compatible with the CMOS manufacturing technology used in microelectronics.

The ideal memory technology has not yet been developed. Thus, several technologies have developed in parallel, to address different applications. Figure II.1 presents the classification of memory technologies (De Salvo,2011), traditionally classified according to their volatility and operating principle. The market for memory technologies is shared between hard drives, where access to information is sequential along tracks written on the surface of the media, and random-access memory (RAM), which consist of individual data bits arranged within a two-dimensional array. Currently, there are three types of complementary RAM memory technologies on the market: SRAM, DRAM and Flash (Nozières,2010). Dynamic memories (DRAM, for Dynamic RAM) and static memories (SRAM, for Static RAM) have the disadvantage of being volatile. On the other hand, they offer a high access time and good endurance. Thus, the computer places the temporary data in these two types of memories. Flash memories dominate the non-volatile memory market, due to their high integration density and low production costs. However, access time is long and endurance is limited and they are used for data storage.

Thus, current memory technologies are complementary and address different applications. It is not uncommon for them to be combined, for example, a computer combines a hard drive, SRAM, DRAM and Flash memories.

Due to their low energy consumption, Flash non-volatile memories are particularly interesting for portable electronics. That market is exploding right now.

The demand for Flash memory, which is in petabits (~ 10^{15} bits), is constantly increasing. Capacity demand doubles every two years starting in 2010. Memory cards for cameras, digital cameras, USB sticks, MP3 players and mobile phones are the engines of the market. Computer hard drives and the automotive industry are high potential markets. Flash technology is being improved.

In order to further develop microelectronics technologies, an industrial consortium meets every two years to establish the roadmap and coordinate research investments. The document entitled "International Technology Road Map for Semiconductor" (ITRS) provides the broad guidelines for future R&D investment (Hoefflinger, 2020). For example, the traditional tunnel oxide (SiO_2) is replaced by an oxide with a high dielectric constant (HfO_2, HfAlO, etc.), which allows the use of higher thicknesses when miniaturizing devices. Leakage currents are reduced and information retention is improved. In parallel, innovative materials and architectures are developed, these are emerging memories.

II.3 Emerging non-volatile memories

The following technologies are considered to be emerging according to the ITRS, in which information storage is not based on the trapping of electronic charges, which makes it possible to continue the reduction of dimensions. They are studied according to their ability to meet the following requirements: surface per cell (F^2), operating speeds (ns), retention time (s), endurance (number of cycles), and consumption (J/bit).

These memoirs are based on the change of polarization or state of resistance of an active material integrated between two metal electrodes and forming a capacity. Several types of innovative memories are currently under development: FRAM, MRAM, PRAM and RRAM. Here we compare their function and properties.

Figure II.2 presents the principle operating of emerging memories. Ferroelectric memories (FRAM for Ferroelectric RAM) use the permanent polarization of a perovskite (generally PZT, Pb (Zr, Ti) O_3) (Vorotilov, 2012). An electric dipole exists naturally, without the application of an electric field, because the barycenter of positive and negative ionic charges is not identical. The memory effect is obtained

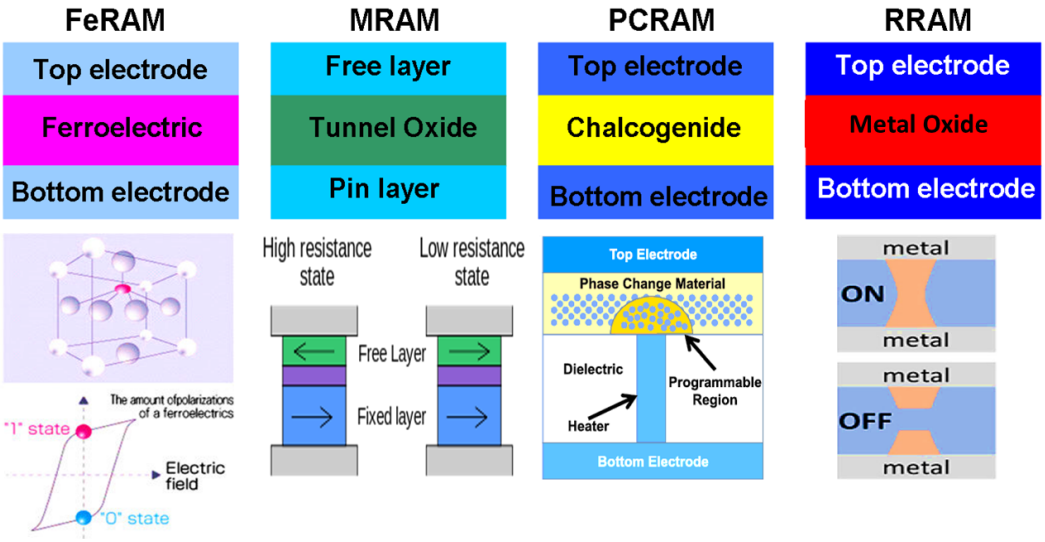


Figure II-2 Operating principle of emerging memories: a) FRAM; b) MRAM; c) PRAM; and d) RRAM.

thanks to two stable polarization states, by the application of an electric field in two opposite directions. The two polarization states are obtained by changing the position of zirconia or titanium atoms. Magnetic memories (MRAM for Magnetic RAM), phase change memories (PRAM for Phase change RAM) and resistive memories (RRAM for Resistive RAM) are based on the change in resistance of the active material. The memory cell is alternately switched between two stable resistance states. In MRAM, two layers of ferromagnetic material separated by a thin layer of oxide form a tunnel magnetic junction (Reohr,2002). The orientation of the magnetic fields determines the strength state of the junction. The magnetic orientation of one of the two layers is fixed, while that of the second can be modulated with the application of a magnetic field. The electron spin aligns with the polarization of the ferromagnetic material which acts as a filter. If the polarizations of the two ferromagnetic materials are parallel (same direction), the resistance is low, if the polarizations are antiparallel (opposite directions), the resistance is higher. In PRAM, the active material is a chalcogenide (generally GeSbTe). Resistance is modulated by a phase change between the crystalline state (low resistance) and the amorphous state (high resistance) (Waser,2010). The phase change is caused by the modulation of the temperature by dissipation of Joule energy in the active material when it is crossed by the electric current. The amorphous phase is obtained by locally heating the

crystalline material with a short, high-intensity current pulse in order to heat the material above its melting point. The phase is stabilized by the sudden shutdown of the electric current. The temperature drops abruptly, which has the effect of a tempering. The crystalline phase is obtained by heating the amorphous phase above its crystallization temperature, using a moderate current intensity. The mobility of the amorphous phase atoms increases and the crystalline phase stabilizes. Finally, the term RRAM is generic and refers to the set of memories based on a change in resistance of the active material by chemical or electrical effects. This phenomenon is observed for a wide variety of materials (binary or complex oxides, organic compounds, solid electrolytes of the selenide or sulfide type, etc.), which presupposes different resistance switching mechanisms. The following section aims to present the characteristics of RRAM memories.

II.4 RRAM memory cell: basics and materials

The operating principle of RRAM is based on a phenomenon of controlled variation of the resistance of a sandwich insulation between two electrodes. This variation in resistance may be due to several phenomena depending on the composition of the MIM structure (Figure II.3 a). The first of these phenomena occurring in the majority of resistive memories in the literature is the reversible formation of a conduction filament at the core of the dielectric that will connect the two electrodes. This filament can be of several types, for example metallic or formed of oxygen deficiency.

Other observed phenomena are current passages by charge effect or by Mott transition. To change the logical state of these memories it is necessary to know the voltage needed to switch from the high resistive state (HRS) to the low resistive state (LRS), this is called the step of SET. The voltage to perform the reverse switching is naturally called the RESET step. Depending on the phenomenon taking place in the component, two types of operation of the memories with very different characteristics I-V can be observed, as can be seen in the graphs Figure II.3 (Wong,2012).

The first type of operation is called unipolar or non-polar Resistive Switching (URS). These memories require voltages of different magnitudes to switch resistive state. If the switching does not depend on the polarity these memories are said to be non-polar; if the polarities of the voltages needed for the SET and RESET steps are identical (the same sign), they are said to be unipolar. Figure II.3b shows that a V_{SET} voltage is applied in order to change from the state from HRS to LRS. The cell then behaves as a resistance until the $V_{RESET} > V_{SET}$ voltage is reached which puts it back in a state of high HRS resistivity.

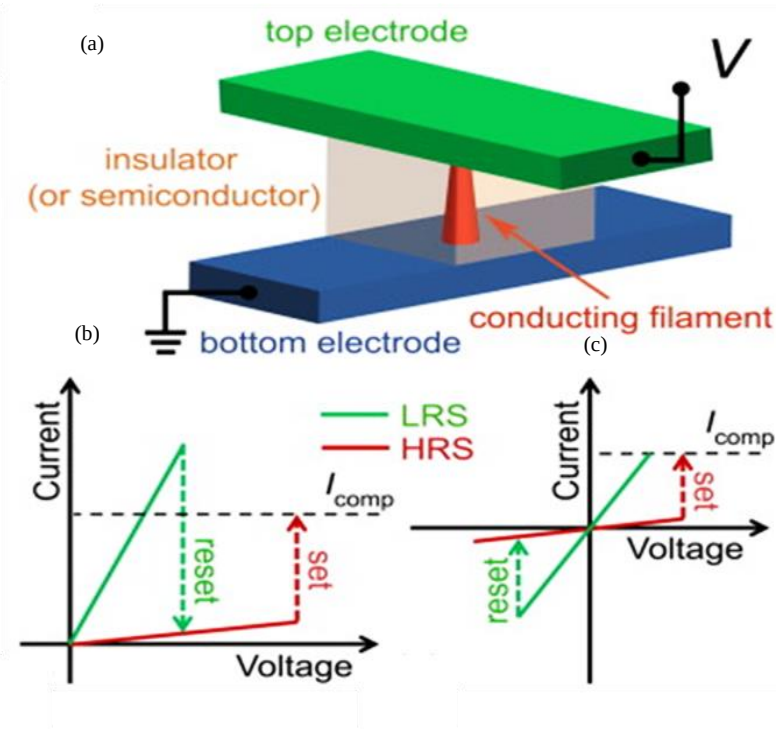


Figure II-3 a) Diagram of the structure of a RRAM cell. I-V electrical characteristics of the b) unipolar and c) bipolar modes.

The second type of operation known as bipolar Resistive Switching (BRS). These memory cells require voltages of the opposite polarity to switch the resistance state.

If the memory is in an HRS state must be polarized in reverse to a V_{SET} voltage in order to switch to an LRS. The electrical response of the cell is then resistive until the V_{RESET} voltage of positive polarity is reached in order to regain a state of high

resistance. In other words, the SET for the ON state takes place at one polarity and the RESET for the OFF state takes place at the opposite polarity (Zahoor,2020).

To obtain either of these operations (URS, BRS) is also depends on the materials used for the dielectric and for the electrodes. The same dielectric may have unipolar or bipolar types of operation depending on the nature of the electrodes. Indeed, the composition of the MIM structure will lead to various phenomena leading to resistive switching (Lanza,2014).

Three different types of operation can be distinguished concerning the physics of the electrical resistance change in RRAM cells. The first concerns bipolar electrochemical metallization (ECM) with a memory effect. The operation is based on the presence of an electrochemically active electrode whose derivation of cations leads to metallic growth. The second refers to the memory effects related to the change of electrons in the valence band (VCM) of metal ions of oxide (Yang,2012), characterized by the migration of oxygen deficiencies. Finally, thermochemical memory (TCM) effects refer to the unipolar behavior. In this case the current induces an increase in temperature and causes a change in the stoichiometry of the insulation. This later is the type of RRAM studying here.

The choice of materials is a priority in the design of MIMs. The selected materials must respect several characteristics including good electrical properties, low cost, and tolerance at the mechanical-chemical planarization (CMP) stage. Following these main selection criteria, the materials are then chosen according to their characteristics. RRAM memories are usually based on a binary oxide of a transition metal (M_xO_y). These are M-O-M (Metal-Oxide-Metal) structures. They have been studied intensively by laboratories and industrialists since the 2000s. More than 2,400 publications were published after this date. The change in resistance of many oxides is being studied. After a short history, we present the most studied and used binary oxides in this work.

The change in resistance of SiO_2, $Al2O_3$, $Ta2O_5$, ZrO_2 and TiO_2 oxides was discovered by Hickmott in the 1960s (Hickmott,1961). A few years later, Simmons proposed the use of resistance-changing oxides to manufacture memory devices (Simmons,1971). However, the development of this technology only began in the

2000s, probably because of the massive development of Flash memories. As the physical limits of this technology approach, the interest in RRAM memory increases. In 2004, the Samsung Group demonstrated the feasibility of integrating RRAM memory with CMOS manufacturing processes (Baek,2004). The first results obtained are encouraging in terms of operating time (10 ns), endurance (10^6 write/erase cycles) and energy consumption (<3V, 2mA). Figure II.4 compares the erasure current intensities (RESET) of the CMOS-compatible oxides (NiO, TiO_2, HfO_2, ZrO_2) studied by Samsung. Nickel oxide offers the lowest energy consumption, so it is the first binary oxide studied intensively (Baek,2004).

There are a large number of binary oxides with the ability to change resistance in

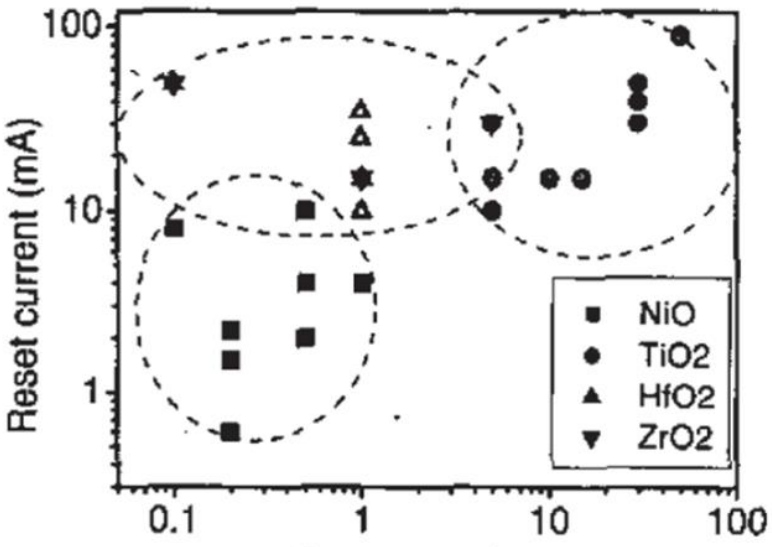


Figure II-4 Comparison of electrical properties of different oxides compatible with CMOS (Baek,2004).

a reversible manner. The set of feasible devices is exhaustive, more than 1500 combinations are possible. The periodic table of the elements below (Figure II.5) is adapted to present the materials available for the design of RRAM (oxides, electrodes). In the following, we compare the performance of the most promising oxides and discuss the impact of the materials that make up the electrodes.

For example, the TiO_2 used so far is suitable for RRAM design in academic settings but is not supported by industry. One of the most common replacements is HfO_2 hafnium dioxide, this oxide is frequently encountered in RRAM design. Its high-k behavior (Baek,2004) allowed the realization of RRAM of 1kbits by Sheu and al (Sheu,2009). The retention time obtained is 10 years with endurance exceeding 10^6 cycles. The efficiency is excellent (~100%), meaning that the majority of the devices change resistance in a reversible way (Lee,2008). The same group also demonstrated that endurance and operating time can be optimized (10^{10} cycles, 300 ps) (Lee,2010). Hafnium oxide is a technologically mature material, although it has recently been studied for RRAM applications. Indeed, it has been studied intensively for years in place of SiO_2 as a grid oxide in advanced CMOS transistors. There are other oxides available for a RRAM application. Table II.1 shows some characteristics obtained for various oxides.

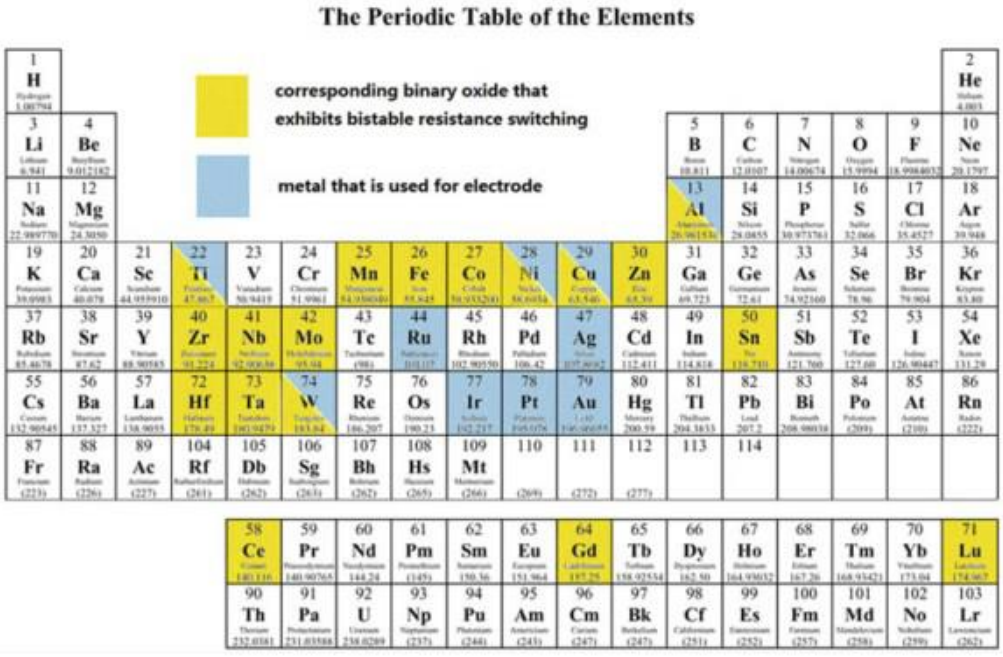


Figure II-5 Periodic Element Table Representation for Materials Used in RRAM Design (Wong,2012).

In electrodes, tungsten, copper, titanium, nickel and platinum are widely used. Titanium and tantalum compounds (TiN, TaN) are also interesting. The material chosen for the electrode controls the resistance change mechanism of the oxide

(Bertaud,2012; Chen,2010; Cagli, 2011) and its performance (retention, cycling) (Goux,2010; Gonon,2010; Vallée,2011). When the electrode oxidizes a little (noble metal: Ni, Pt…), the unipolar mechanism is preferred. For an oxidized electrode (Ti, TiN, Al, etc.), the bipolar mechanism is predominant. The porosity of the electrode and its thickness must be checked to improve performance. Indeed, the mechanism of resistance change could involve the formation of conductive regions in the oxide following the migration of oxygen atoms. When the electrode is fine or porous, the oxygen atoms leak and are no longer available to repair the conductive region (no RESET). However, if the electrode is too thick, the oxygen atoms accumulate at the oxide/electrode interface. Electrode deformation and hole formation are observed, probably due to gas retention (O_2). Therefore, electrodes play a decisive role in the operation of RRAM, that is why we are studying new materials to be used for RRAM electrodes, such as Carbon Nanotubes (CNT) and Copper (Cu). These materials will be discussed in details in the next chapters.

Table II-1 Performance of different binary oxides embedded in RRAM devices (Wong,2012).

Identifier	W_{ox}	HfO_x/AlO_x	Hf/HfO_x	Ni/HfO_x	HfO_x	TaON	HfO_x	HfO_2/CuGeS
Publication & year	IEDM 2010	VLSI 2011	IEDM 2011	IEDM 2012	IEDM 2012	IEDM 2013	VLSI 2014	IEDM 2015
2D/3D Geometry	2D Transversale	2D Transversale	2D Transversale	2D Transversale	3D Verticale	2D Transversale	3D Vertical	3D Vertical
Type of switching	Bi	Uni	Bi	Bi	Bi	Uni	Bi	Bi
Structure	1R	1R	1T-1R	1T-1R	1R	1R	1R	1R
TE/material/BE	TiON/WO_x/W	Ni/HfO_x/AlO_y/p-Si	TiN/Hf/HfO_x/TiN	TiN/Ni/HfO_2/n+-Si	TiN/HfO_x/Pt	Cu/Ta/TaN/TaON/Cu	TiN/HfO_2/TiN	W/CuGeS/HfO_2/TiN
Cell area (µm2)	0.000081 (9nm)	~6000	0.0001 (10nm)	0,0014	~4	0.0009 (30nm)	0,000003	60nm (électrode)
Switching time [ns]	~1000	~30	~10	~50	~100	~100	50	500
DC voltage [V]	<4	<2.5	<1.5	<4.5	<3.5	<5	<3	4
DC current [uA]	~1	~1000	~50	~0.0002	~50	~800	~500	<0.001
HRS/LRS Ratio	>10	>1000	>10	>10	>10	>100	100	100
R high[Ω]	$5x10^8$	10^8	10^7	10^9	10^7	$5x10^8$	10^6	10^{12}
R low[Ω]	$5x10^7$	10^3	10^6	10^7	10^5	$5x10^5$	10^4	10^{10}
Endurance	200	10^6	$5x10^7$	10^5	10^8	15	10^4	$>10^7$
Retention	280h à 200°c	28h à 150°C	30h à 250°C	10 An à 85°C	28h à 125°C	300h à 300°C	2000h à 250°C	10^4s à 85°c

II.5 RRAM cell arrays: crossbar architecture

The memory devices to be used, are arranged into array architecture, and the address or the access to a memory point is done through the application of specific voltages on the desired rows and columns. The RRAM memory cells have two terminals, so their matrix architecture layout requires only two addressing lines (denoted as Word Lines (WL) and Bit Lines (BL) which is a big advantage in terms of integration density. Moreover, the production of such cells is not very complex because it requires only a layer of oxide between two metal electrodes: passive crossbar 3D matrices consisting of perpendicular metal lines separated by a switching oxide are thus low-cost and very dense solutions to achieve an array of RRAM memory devices (see Figure II.6) (Nauenheim,2008). Indeed, if we consider F (smaller dimension achievable in a technological node) as the width and spacing between two metal lines then the minimum surface area of a memory point is $4F^2$.

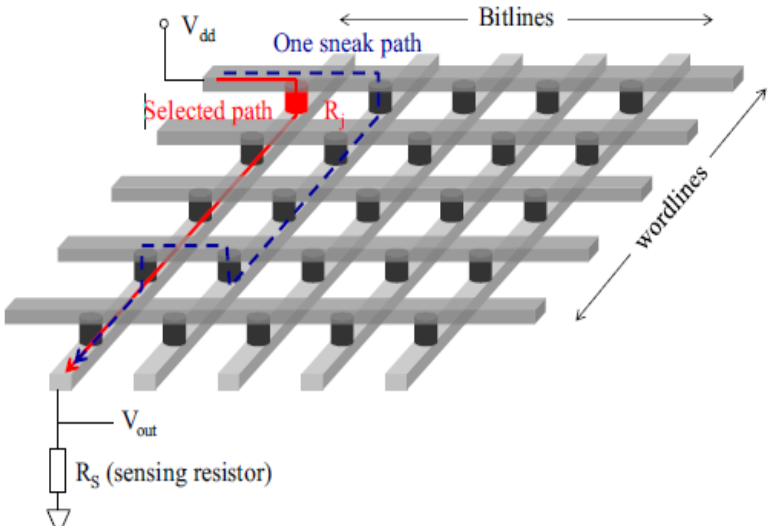


Figure II-6 Crossbar architecture of resistive memory. The current path corresponding to the selected cell is represented by a red line while one of the possible leakage current paths is represented by a blue dotted line (Chen,2013).

II.6 RRAM Integration Challenges: signal and thermal integrity

In fact, regardless of the architecture considered, the commercialization of these types of crossbars is hampered by the presence of significant leakage currents or

sneak paths. These leakage currents are undesired “current paths” that could disrupt the reading of the selected cell and/or result in the writing of non-selected cells, as shown in Figure II.6. These currents depend primarily on the resistance of the interconnection between two memory cells, the status of the non-selected cells in the crossbar, the status of the selected cell, and the size of the crossbar. The most important condition however is that each memory point has a strong non-linearity in its two states LRS and HRS in order to always be strongly resistive in a state of «RESET», that is, it must not allow power to pass when it is half selected or not selected.

For example, if one considers reading a memory point with a Vdd voltage, the memory points on the same line and those on the same column as this memory point will have potential at their Vdd/2 or Vdd/3 terminals depending on the configurations used (Gül,2019). It is important that the sum of the leakage currents through all these «half-selected» memory points (Vdd/2 or Vdd/3) is much less than the current of the read memory point.

The leakage currents can lead to several drawbacks where during the write phase, the unselected cells are exposed to a voltage drop causing a drift in their internal state. Another issue is during the reading phase, these paths cause a degradation in the sense margin leading to false estimation of the state of the selected device. In addition, more power is dissipated in the crossbar.

The main causes of electronic failures are high temperature, humidity, vibration, and dust, as shown in Figure II.7 (Khattak,2019). About 55% of electronic challenges are caused by thermal management failure (Bailey,2008). In addition, a large portion of thermal management failures are due to non-uniform temperature distribution on the chip surface. The non-uniform temperature distribution is mainly caused by the following reasons. One is the temperature increase along the flux path, due to the gradual increase in the temperature of the coolant along the flux path and the decrease in the heat transfer coefficient as the boundary layer thickens, resulting in the creation of a temperature gradient along the flux path. Another problem is hot spots due to non-uniform heat flux from the heat generating components which is known as the thermal crosstalk phenomena.

A major issue related to such crossbar architecture is the high temperatures reached during operating conditions, which introduce thermal crosstalk between the layers.

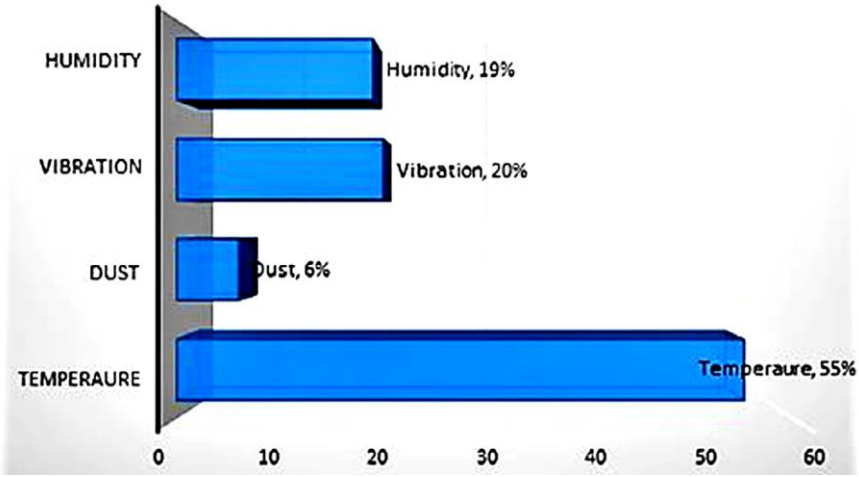


Figure II-7 Major causes of failure of electronics.

Therefore, a cooling system is required to guarantee smooth operations, which increases the energy consumption and lowers reliability. Thermal is the field of physics that deals with heat exchanges or heat transfers in a system or between two systems. The thermal properties of the materials govern these exchanges and thus characterize the behavior of the materials in the presence of one or more types of heat exchange. These properties are thermal conductivity, thermal diffusivity and thermal effusivity. Note that generally the thermal properties depend on the nature of the material and its temperature.

II.6.1 Novel Architectures: 1S1R, 1D1R or 1T1R

The simplest method adopted to solve or mitigate these problems is to prevent the current from passing through the non-selected cells by coupling them to a selector component such as a diode or a transistor (as shown Figure II.8). The diode is achievable with the same materials as the memory and can therefore be integrated vertically without loss of space, however it only works for unipolar memories. The transistor is more efficient but requires much more space, which greatly decreases the interest of these memories. The integration in 3D could minimize this problem by

offering a 1TnR architecture with n the number of memory layers. Finally, research has focused on selectors that can act as diodes for unipolar and bipolar cells. An example of this type of breeder is a Mott insulation (Akinaga,2010).

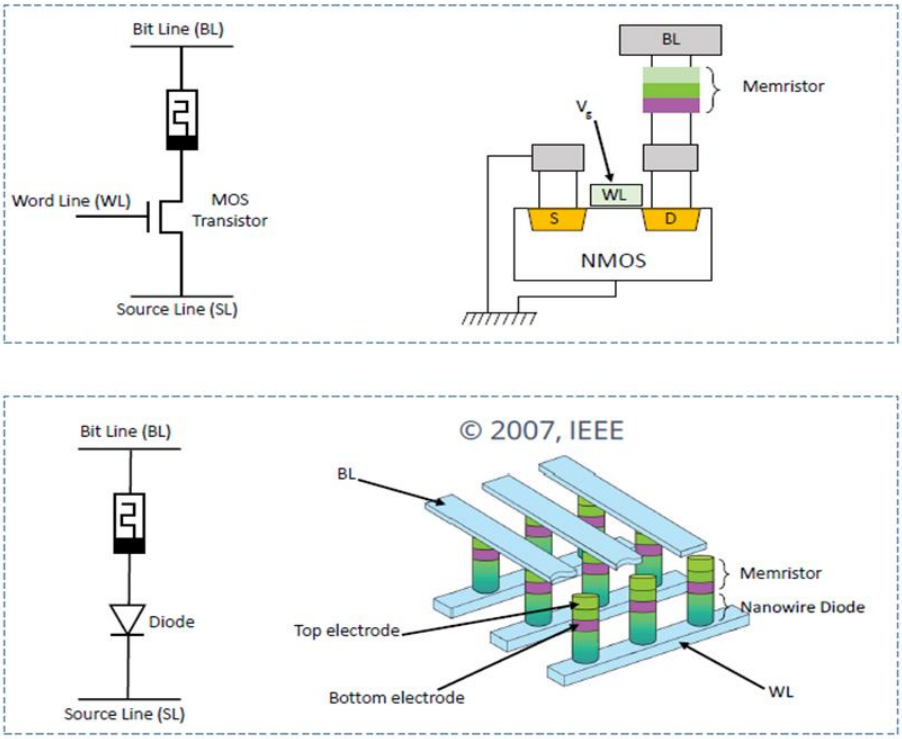


Figure II-8 Selector devices: a) Transistor type b) Diode type.

II.6.2 Alternative bias schemes

Among the intuitive solution to tackle the signal integrity problem is to RESET the farthest cell in a cross-point array by applying a high bias voltage to the word-line (Amer,2019). However, this idea induces a permanent breakdown stuck of near cells; increase both the joule power and RRAM operating temperature due to high voltage stress. Advanced bias schemes are instead proposed to improve power consumption and read margin, by subdividing the crossbar array into multiple sub arrays, selected by nonlinear devices (i.e., transistor, diode). For instance, the 1/3 bias scheme enables a larger read margin due to the reduced IR voltage drop of the selected cell, while 1/2 write scheme is preferred, due to a much lower power consumption (Sun,2016). Other method attempts to overcome these issues is the

management of the applied bias between the word and bit lines of the crossbar which is demonstrated in details in chapter III.

II.6.3 Complementary Resistive Switching structure (CRS)

The Complementary Resistive Switch or CRS is a 2R type memory consisting of putting two RRAM around the active electrode (Yang,2012). The resistive state of the low voltage CRS is necessarily HRS because this resistive state is the result of the serial association of a RRAM in HRS and a RRAM in LRS. This association prevents current leakage, because in a memory crossbar, the passage of the current through a CRS not selected will always be less profitable since it will be in a state of high resistivity. This effect is shown in Figure II.9, which shows the filament status of the two RRAM that make up the CRS at each point of its I-V characteristic. At a lower voltage in absolute value at V_1 or V_3, the memory point always appears in HRS because one of the two RRAM is necessarily in the HRS state.

The logical state of the CRS is determined based on which RRAM cell is in HRS by reading at a V_{Read} voltage between V_1 and V_2. The CRS is considered to be in an ON state if the upper RRAM is in the LRS state and the lower RRAM is in the HRS state, case 1 shown schematically in Figure II.9. If, on the opposite, the upper RRAM is in HRS and the lower RRAM is in the LRS state then we consider the memory in the OFF state, this is the case diagram 3. To switch from HRS to LRS, a positive voltage greater than V_2 will be applied to switch from an ON state (state 1) to an OFF state (state 3). To perform the reverse switching, a negative voltage lower than V_4 is applied. Since the CRS, made up of two resistors, acts as a voltage divider bridge, if voltage is applied to the CRS, it is the RRAM in the HRS state that will have most of the voltage across these terminals. If the polarity of the voltage allows it, this RRAM in the HRS state will switch to the LRS state schematized as the transition a) for a SET and c) for a RESET in the diagram. At this time both RRAMs are in the LRS state, state #2 in the figure. Finally, one of the RRAM cells will switch to the LRS state depending on the polarity of the voltage so that the CRS reaches the desired ON or OFF state according to the transition b) for a SET and d) for the RESET. To read the state of the CRS is applied a voltage V_{Read} between V_1

and V_2. If the CRS was in an ON state, the voltage V_{Read} being greater than the voltage V_1, the CRS will be in its transition state 2 and a large current will be read.

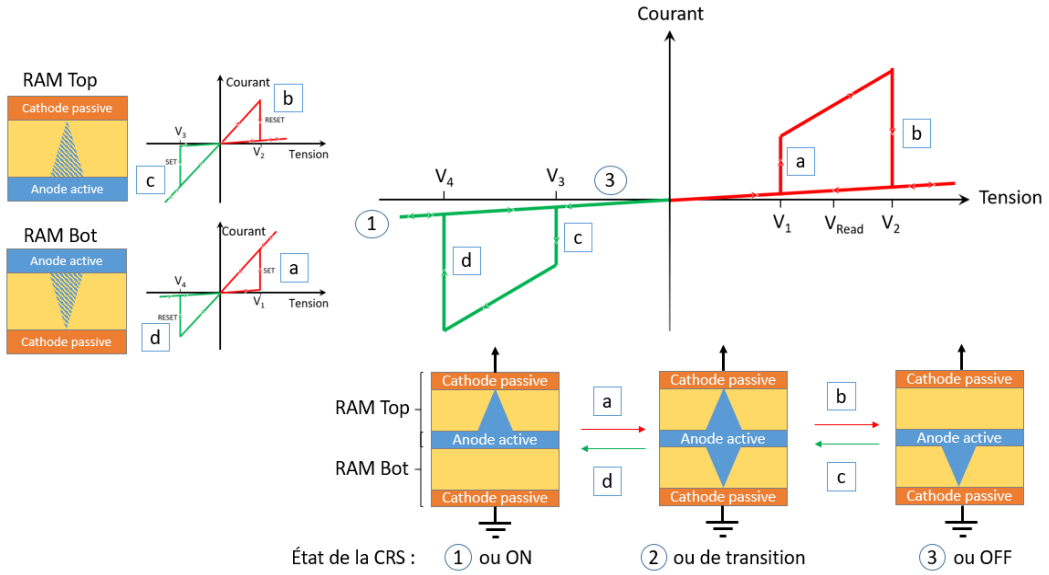


Figure II-9 Diagram of a CRS structure in its three states and the corresponding characteristic I(V). The circles show the three possible logical states of the CRS and the squares show the possible transitions between these states. State 1 is an ON state of the CRS when the RRAM top is in LRS and the lower RRAM in HRS. The reverse state 3 is the OFF state of the CRS. State 2 is a transition state accessible only under voltage between V1 and V2 or between V3 and V4.

Note that this reading is destructive and a rewrite is therefore necessary. If the CRS was in an OFF state, there will be no resistive switching and a low current will be read.

II.6.4 Impact of signal and thermal integrity: a case study

The main scope of the RRAM case study is to address signal and thermal integrity issues and improve the read/write margin, then new architectures are proposed, such as those named in this thesis as inverse and complementary resistive switching, for realizing large arrays of RRAMs, comparing their performance in terms of signal and thermal integrity, to the conventional 1D-1R crossbar structure. For all the considered architectures, the elementary memory unit (also denoted as the “X-point”) is the 1D-1R cell depicted in Figure II.10b, made by the series of a Ni / HfO_2 / Pt

resistor and a Pt / TiO_2 / Ti diode. The reference crossbar structure (see for instance (Zayer,2020)) is obtained by sandwiching planar arrays of 1D-1R between the two sets of conducting bars (WL and BL). In the reference structures, these lines are made by Ni, so to realize the active electrode and to create a Ni conductive filament (see Figure II.10b).

In absence of the CF, the RRAM is at the High Resistive State (HRS), whereas once the CF is formed, it switches to the Low Resistive State (LRS). The RESET current is 1.7×10^{-4} A. Indeed, the diode is added to limit the sneaky current during its read/write process, as pointed out before.

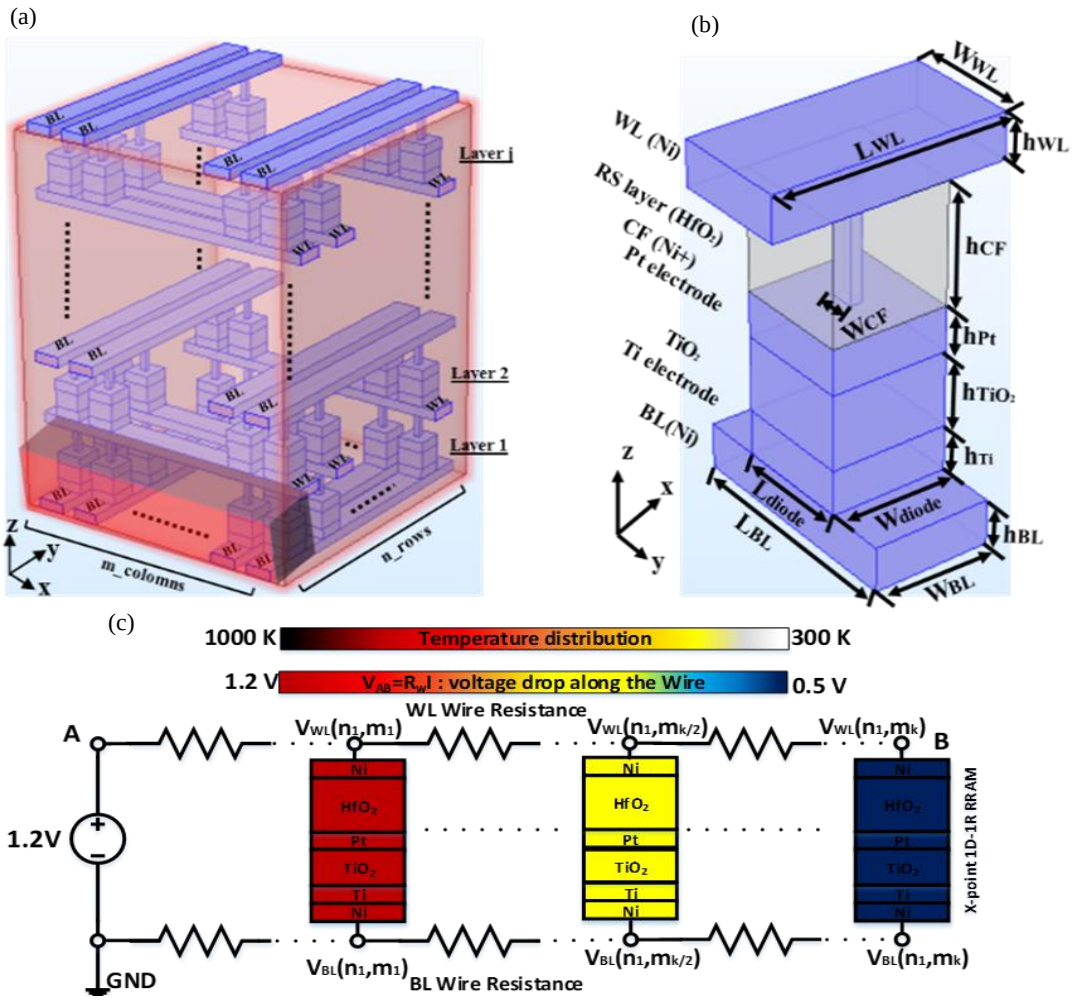


Figure II-10 a) 3D 1D-1R crossbar RRAM structure. b) 1D-1R cell as the X-point RRAM building block. c) Signal and thermal integrity issues: voltage and temperature distribution along the WL and BL wires.

The 3D architecture in Figure II.10a has been devoted a large interest in literature, since it naturally enables monolithic integration (Li,2017). It was reported that the crosstalk effect in integrated RRAMs is more sensitive to the feature size spacing, interconnects and CF widths, rather than type/mode of device operation (Chen,2018). A larger spacing can suppress the crosstalk. However, this results in smaller storage density. Hence, it should be there a trade-off between scalability and stability of the RRAM integration. On the other hand, the aggressive downscaling of the whole array dimensions and of the wire widths result in major issues. For instance, the resistance of the WL and BL interconnects brings extra latency and energy consumption, and causes voltage drop along the line (Tseng,2017). The voltage drop significantly affects the signal integrity, by altering the requested level of voltage for reliable SET and RESET switching. For instance, the 1D-1R ideally requires low voltage values for the SET and RESET processes, thus improving the overall power efficiency. Nevertheless, the voltage drop in the 1D-1R RRAM crossbar is associated to the CE resistivity (e.g., IR drop). Therefore, the assumed step RESET voltage amplitude at the X-point memristive elements may decrease to a lower value inhibiting the OFF switching, see Figure II.10c). The same considerations for thermal integrity apply, since the distribution of temperature along the bar follows a similar trend as the voltage. To face this issue, the bias voltage applied to the word-line could be increased, but this results in increasing power demand and in increasing Joule dissipation, hence increasing temperature. Other proposed solutions are based on advanced bias schemes, such as for instance the 1/3 bias scheme that enables a larger read margin, or the 1/2 one that leads to a lower power consumption (Long,2013; Liu,2013). However, the signal integrity analysis disregarded the coupled electro-thermal effects. Indeed, studying the thermal behavior of the RRAM structure is important not only for studying the thermal integrity but also for its impact on electrical performance (Sun,2015; Luo,2016).

II.7 Conclusion

Electronics dedicated to the storage of information is a strategic point in the current IT environment. Many memory technologies that have been in use for

decades are now reaching their technological limits, including Flash memory preferred for long-term storage. The rise of emerging memories is directly linked to the coupling between the growing need for information storage and the difficulty encountered in improving current semiconductor memories. The literature shows several innovative technologies at different maturity running in parallel with attempts to extend current technology. We can cite MRAM, PCRAM, FERAM and finally the subject of this report, RRAM.

- RRAMs are a potential answer to these growing needs, because they equal or even surpass current memories in terms of performance. They consist of a two-electrode MIM-type structure and store information in resistive form using various phenomena of controlled resistive switching.
- The signal and thermal issues as well as the problems of the current leakage in the crossbars of RRAM remain today the two main obstacles to the massive development of such a technology.
- Several solutions are being studied to address these issues. The use of new structures could improve the performance of RRAMs, 3D architectures including selectors would prevent leakage currents in memory arrays, and the management of the bias schemas could decrease the IR drops and the thermal crosstalk in the crossbar architectures.

Chapter III : Electrothermal Modelling

Chapter IV

III.1 Introduction

This chapter introduces the main methods used in recent decades to improve the consideration of thermal aspects in the design of electronic components and circuits. The operating temperature fundamentally determines the electrical behavior of the electronic components, the design of heat removal devices is crucial for modern components with high density. Thermal models have been continuously improved in recent years, however, not all are suitable for all stages of design. Thus, to address the different needs of engineers, several types of models are developed (numerical mesh, analytical, behavioral, compact, etc.).

The physical phenomena that condition the electrical behavior of electronic devices are intimately related to the temperature of the component. Meanwhile, the component temperature is strongly related to the power dissipation that is given by the forms of electric waves. There is therefore a real coupling between the electrical behavior of the electronic components and the thermal impact of the entire structure.

Thus, in the design of electrical engineering, particularly in power electronics components and systems, the thermal evolution during the operating cycles must be taken into account in order to increase the reliability of power systems.

The purpose of this chapter is to present the numerical resolution of our models. We present electrothermal coupling, COMSOL Multiphysics software and mesh sensitivity, parameters and numerical procedures used to solve our models which are analyzed in the following chapters.

III.2 Generalities on electrothermal modelling approaches

The modeling of electrothermal systems is typically composed of two parts, “heat” (thermal behavior) and “power” (electrical behavior) (Wunsche,1999). This electrothermal system is strongly coupled, where the schematic description of the complete interaction between the thermal and electrical network is shown in Figure III.1. The electrical and thermal model is connected through estimation on self-heat dissipation, which is achieved by electrical behavior simulation. In fact, the thermal issue cannot be neglected since most of the parameters of the device are strongly

dependent on the temperature and then the heat is dissipated by the Joule effect. On the other hand, this dissipation changes the temperature of the charge and acts on the electrical parameters.

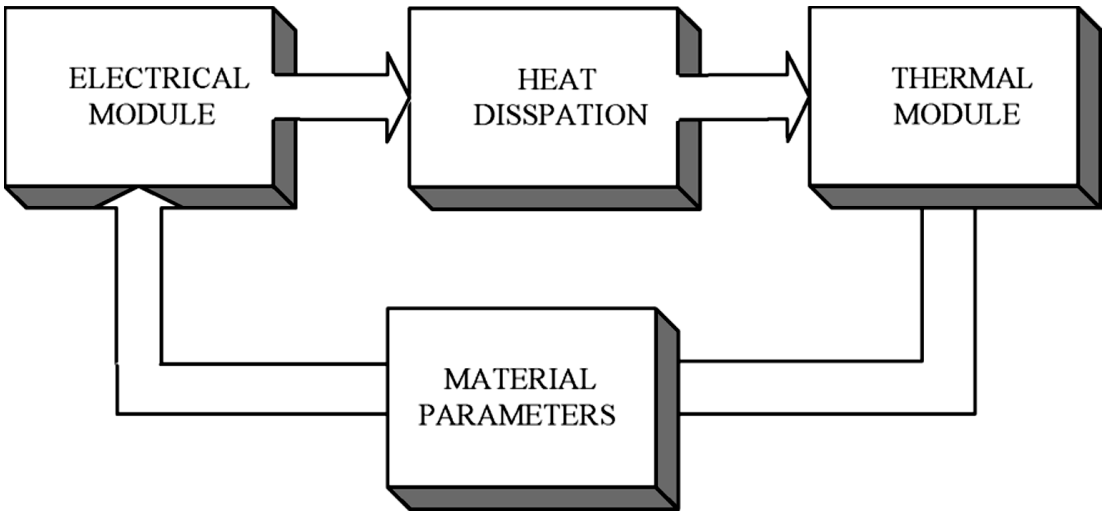


Figure III-1 Diagram of the complete electrothermal model (Du,2009).

Thus, in order to increase the reliability of electronic systems and to optimize their thermal design (enclosures, operating conditions, location of components on the printed circuits, etc.), it is necessary to have a good estimate of the electrothermal behavior of circuits and components.

The steps necessary for the electrothermal coupling of the electronic components are defined by two main approaches (Türkes,1998): The first step is to define all parameters of the electrical model that are affected by the temperature (mobility, carrier concentration, conductivity, etc.), as illustrated in the Figure III.2, the device model is fed with the instantaneous temperature of the device by the thermal network (from this temperature value the component model calculates temperature-dependent parameters of the device). The second step is to create an electrical model of the electronic component (MOS, IGBT, Diode, etc.), where the electrical parameters will be the operating conditions such as the voltage drop through the device and the current to be pinched from the circuit in which the device plays a given role. The last step then is in the device model, the part of the power loss calculation, collects all this information to calculate the power dissipation in the device. The dissipated power is supplied again to the thermal network for the temperature calculation. These

steps complete one cycle of electrothermal simulation and establish the communication between the two models (Figure III.2).

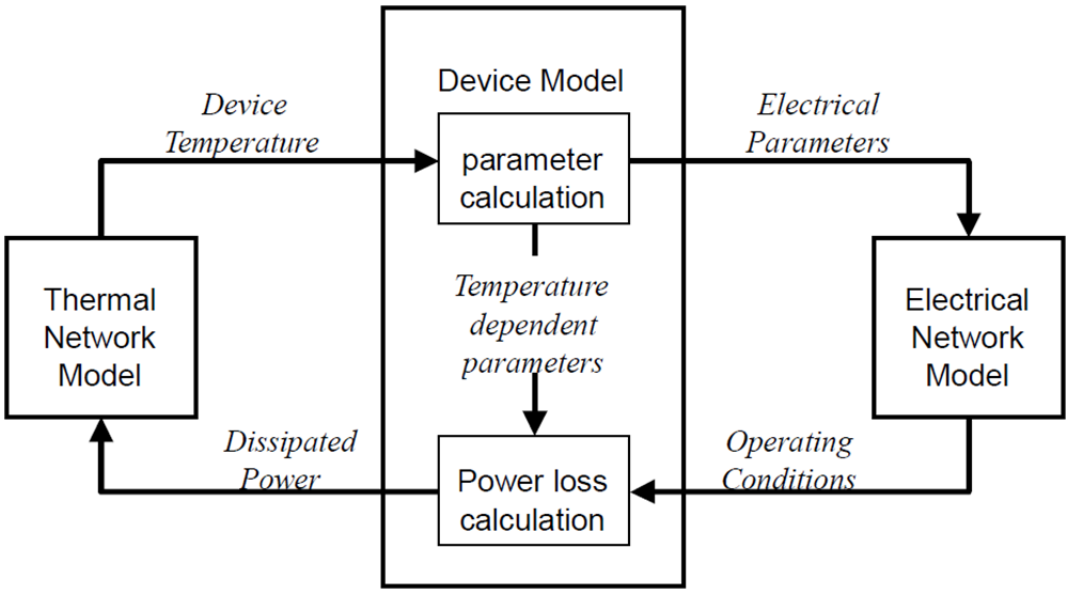


Figure III-2 Operating cycle of the electrothermal model configuration (Lee,2003).

Several methods have been explored to achieve this coupling and they can be classified into two main types are the relaxation method the direct method.

III.2.1 Relaxation Method

The relaxation method is based on an alternating resolution of the two systems of associated equations. This method is carried out considering the temporal coupling between the electrical simulator and the thermal simulator (Gutierrez,1999; Van,1994), and using an interface software (API: Application Programming Interface) to control the flow of information between the two simulators and their activation according to time. This software pauses the electrical solver after each time step and transmits the dissipated power to the thermal solver which calculates the temperature which will be sent back to the electrical simulator. More specifically, this method consists of adopting an iterative scheme in which the electric equations and the FEM equations are separated and updated alternately. However, this approach may suffer from a lack of robustness (instability).

The relaxation method can be as precise as desired and provides temperature maps at the interfaces between layers giving gradients that can induce thermomechanical stresses. However, the increased precision and the strategy adopted for reliable convergence control make the calculation time very long (Gutierrez,1999). This method is schematized in Figure II.3a below.

III.2.2 Direct Method

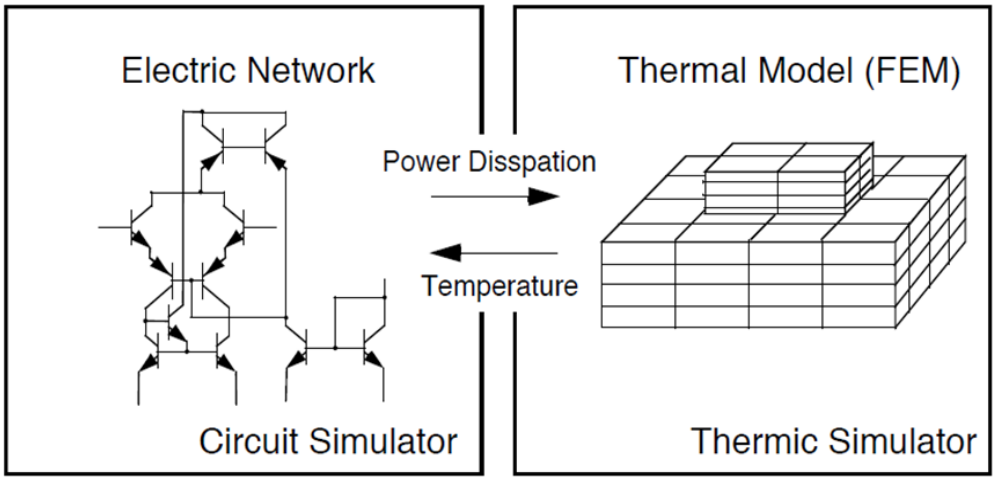
The direct method or fully coupled solution is based on a modeling of the module's thermal and electrical behavior by integrating into the same system of equations within a single simulator (Gutierrez,1999; Jakopović,2001). This approach requires prior thermal and electrical modeling of the component. For example, thermal modeling can be performed using an analog behavioral language such as C^{++} and the electrical problem could be described using a SPICE network list. Thermal modeling presents the major challenge in several simulations, which can be described by finite element, finite differences, Fourier series and, thermal ladder networks. The thermal simulator, which takes into account the thermal parameters of the entire structure, will have all the information to calculate the electrothermal behavior. Indeed, the direct method is characterized by the simulation where the electrical and thermal models are strictly connected through real-time return, a change in electrical quantities instantaneously involves temperature adjustments and vice versa.

The main advantage of this coupling approach is given by the relatively low computational effort (the computation time is low compared to the "relaxation" method), making this method suitable for simulators used in commercial or industrial environments. This method is shown in the following Figure III.3b.

In this work, a complete 3D electrothermal coupling exploiting the finite element method is simulated. This coupling is considered as a kind of hybrid method since it uses one single simulator as the direct method for the implementation and follows a typical relaxation scheme. This feature makes it possible to exploit the advantages of the two methods discussed and, at the same time, it avoids their respective disadvantages. Where there is the possibility of carrying out simulations using a

single simulator which at the same time avoids all the programming effort required to implement the numerical method from scratch. Indeed, these days commercial software such as COMSOL Multiphysics® or ANSYS® provides several ways to solve the electrical and thermal problems by FEM analysis. Thus, the main effort implementation lies in the geometrical modeling of the device, which is in any case required by both the direct and the relaxation method.

(a)



(b)

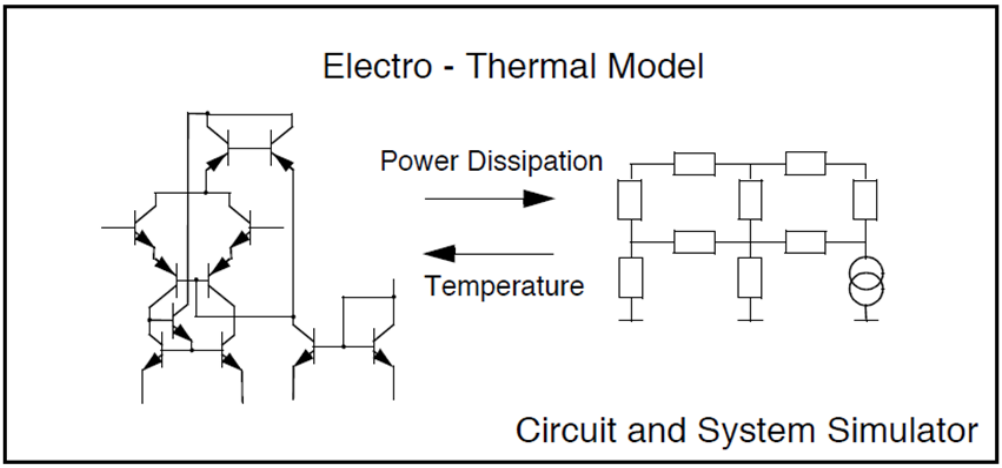


Figure III-3 Schematization of the two main electro-thermal coupling methods used for electronic system: a) relaxation method, b) direct method (Vellvehi,2006).

III.3 Electrothermal model formulation

For solving the electrothermal modeling in this work, the 3D Fourier heat flow equation is coupled to the Poisson electrical equation:

$$\rho(T)\, C_P(T) \frac{\partial T(\vec{r}, t)}{\partial t} - \nabla\kappa(T)\nabla T(\vec{r}, t) = F(T) \qquad \text{(III.1)}$$

where $\kappa(T)$, $\rho(T)$, and $C_P(T)$ are the Temperature (T) dependent thermal conductivity, mass density, and specific heat of the material in the considered region, respectively, which means that those quantities define nonlinear material properties. Finally, the right-hand side of the equation (III.1), namely $F(T)$ describes the heat production which is assumed to be only related to the Joule dissipation in the conducting regions and usually called generation term of the heat equation. Therefore, $F(T)$ depends on the solution of the electrical problem (Poisson equation), that provides the potential distribution, v, in the same region (III.2), being $\sigma(T)$ the temperature-dependent electrical conductivity:

$$F(T) = \sigma(T)|\nabla v(t)|^2 \qquad \text{(III.2)}$$

Before describing the boundary conditions of the heat equation, it is necessary to explore the conduction of heat in this work defended by Fourier's law. This model is known as the most common constituent relationship for heat transfer in various engineering materials. For thermal conduction, this law has a linear relationship between heat flux density q and temperature gradient:

$$q(\vec{r}, t) = -k\, \overrightarrow{\text{grad}}\, T(\vec{r}, t) = -k\nabla\, T(\vec{r}, t) \qquad \text{(III.3)}$$

Indeed, the heat equation identifies the variation of the temperature field $T(\vec{r}, t)$ in space and in time. Therefore, to determine the solution in a partial differential equation (PDE), the definition of an initial condition and a Boundary Condition (BC) are required. There are a large number of boundary conditions, depending on the formulation of the problem, the number of variables involved, and the nature of equation (Zhang,2007).

The conditions imposed at time t=0 are the initial conditions and we can also impose conditions on the limits for example in the limit for t =>∞.

For the definition of boundary conditions of such a domain (Ω) governed by the differential equation, as shown in figure III.4, the component of q is orthogonal to the Γ domain boundary which is called the external normal heat flux q_n is useful as follows:

$$q_n = q(\vec{r}, t).n = -k\nabla T(\vec{r}, t).n \qquad \text{(III.4)}$$

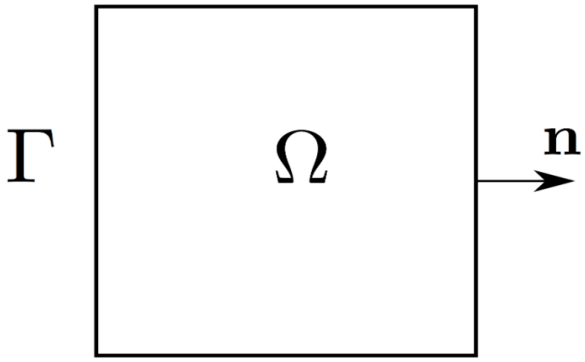


Figure III-4 Geometry and external boundary of a square domain with the normal vector at the boundary.

Here n presents the external normal to Γ. The domain can exchange heat with the external environment through three different heat transfer mechanisms, i.e., conduction, convection, and radiation.

This work focuses on conduction heat transfer, where there are two types of possible boundary conditions definitions, Dirichlet and Neumann boundary conditions.

On an interface or boundary, it is imposed the value of the solution of a conservation equation such as temperature or electrical potentials. In other words, it is a fixed value specifying the value of the function on the surface, in our case, it defines the temperature values along the domain boundary Γ.

$$T(x) = \overline{T} \quad \forall x \in \Gamma \tag{III.5}$$

On an interface or boundary, it is imposed with the value of a flow such as heat flux or current density. Thus, the flux is bound by a gradient to the variable, so the Neumann condition is to impose a value to the gradient of the variable. Indeed, it is to specify the normal derivative of the function on a surface, which here defines the value of the outward normal heat flux in (III.4):

$$q_n(x) = -k\frac{\partial T}{\partial n} = \bar{q} \quad \forall x \in \Gamma \tag{III.6}$$

This condition determines the orthogonal thermal flux along the boundary. Thus, the condition in (III.6) is named non-homogeneous Neumann BC which is opposed to homogeneous Neumann BC, defined by:

$$q_n(x) = -k\frac{\partial T}{\partial n} = 0 \quad \forall x \in \Gamma \tag{III.7}$$

Indeed, the boundary condition of (III.7) defines the case where there is no exchange between the domain (Ω) and the external environment (case study). This is the case of an adiabatic wall, which means that the domain is thermally insulated.

For the electrical part, it's necessary to define the electrical potential for electronic devices where the general differential form of Faraday's law is:

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{III.8}$$

This condition indicates that the loop of the electric field E is given by the rate of change of the magnetic field B over time. For the solution of the electro-thermal problem, it is sufficient to consider the stationary case, so that the temporal dependencies of the electromagnetic quantities involved can be neglected. Thus, the condition in (III.8) can be rewritten as follows:

$$\nabla \times E = 0 \tag{III.9}$$

According to equation (III.9), it is noted that the electric field E is irrotational, and consequently, an electric scalar potential V can prove in order to express E as the gradient of V:

$$\mathrm{E} = -\nabla \mathrm{V} \tag{III.10}$$

The distribution of electrical quantities can be defined by the current continuity equation additionally to (III.10):

$$\nabla . \mathrm{J} + \frac{\partial \varphi_e}{\partial t} = 0 \tag{III.11}$$

Here φ_e is the density of charge per unit volume per unit time. In the stationary case, the capacitive effects are neglecting and the vector of the current density field J is solenoidal, so the equation (III.11) is given by:

$$\nabla . \mathrm{J} = 0 \tag{III.12}$$

The current density J can be linked to the electrical potential V by the equivalent differential form of the Ohm law:

$$\mathrm{J} = \sigma E \tag{III.13}$$

When replacing conditions (III.12) in (III.13), and then the equation (II.10) is given by:

$$\nabla \sigma . \nabla \mathrm{V} = 0 \tag{III.14}$$

This condition then describes the distribution of the potential V in the field in the stationary case. Equation (III.14) presents a form of the partial differential equation such as the heat equation (III.1), so its solution requires definitions of boundary conditions and is defined by:

$$\mathrm{V} = \overline{\mathrm{V}} \quad \forall \mathrm{x} \in \Gamma \tag{III.15}$$

$$\frac{\partial \mathrm{V}}{\partial \mathrm{n}} = 0 \ \ \forall \mathrm{x} \in \Gamma \tag{III.16}$$

In this case, the solution of equation (III.12) did not require any initial condition since the time variable is not involved.

The electrothermal model must be solved by imposing proper interface and boundary conditions. In our case, the computation domain is given by a box including the structure under study and the thermal and electrical flux exchange is

only possible through the electrodes. In the electrical problem, Dirichlet-type boundary conditions are assumed: the WL electrodes can be fed at one side or at both sides with a given bias voltage, whereas the BL bars are grounded. For the thermal problem, the electrodes are assumed to be in contact with an ideal heat sink, imposing constant temperature $T = 300K$ on the boundary surfaces of the closing box corresponding to non-conducting thermal and electrical materials, thermal adiabatic and dielectric electrical conditions are imposed.

Note that in cases of practical interest, an electrothermal model must be formulated and solved numerically. Indeed, an analytical solution can be found only in the case of relatively simple structures. For instance, the thermal model can be solved by using series of transformations and mathematical functions (Fourier, Heinkel, Kirchhoff, Green… (Sabry,1999; Pesare,2001; Janicki,2002)) on the heat transfer equation. Among the different analytical methods, we can cite the method whose mathematical solution is in the form of a Fourier series which has found an interesting application to solve 3D thermal problems in relatively simple structures. The considerable advantage of this method is its speed of calculation.

III.4 Example of numerical implementation: memristor application

The electrothermal model presented in the previous Section can been numerically implemented by using three main methods: finite element, finite difference and finite volume methods. In this work, we adopted the finite element (FE) method, since we implemented the model by using COMSOL Multiphysics software (Luo,2016).

The FE method consists of discretizing the space using simple geometric elements (triangles, rectangles in 2D and tetrahedrons, hexahedrons in 3D). It is suitable for modeling very complex geometries. Then, partial differential equations and boundary conditions are replaced by the so-called weak form (or integral form) in which the unknowns are calculated using linear combinations of basic functions (Hermite polynomials) whose support is one of the elements (Ciarlet,2002). The FE method is therefore based on a decoupling of the space according to a mesh. Usually, we choose a square or triangular mesh but nothing forbids to choose more complex

meshes. It is also not necessary for the mesh to be regular and there is a tendency to tighten the mesh close to the places of interest (for example, where the solution is thought to vary greatly). The tighter this mesh is, the more accurate the solution obtained by the finite element method will be and will be close to the "true" solution of the partial differential equation.

With such a Finite Element analysis simulator (Thomas,2013), the geometric configurations of the elementary device and of the global structure for our applications (RRAM and Thermistor) can be designed with a specific material property of the structure to be simulated under electrical and thermal excitation and boundary conditions. Several partial differential equations have been solved in COMSOL to obtain the necessary behavior of temperature and electric field, which are listed in the previous section. The electric currents, heat transfer in solids, and multiphysics equations are mathematically formulated as follows and included in COMSOL modules to be used in the electrothermal model.

In the following, we discuss in details the implementation in COMSOL of the problem related to the memristors, with results validated against experimental and simulation results available in the literature. The first validation refers to 1R-RRAM structure, while the second one refers to 1D-1RRAM structure.

III.4.1 Modelling a single RRAM cell, standard configuration

The thermal conductivity κ(T) of the Ni^+ CF can be modeled as formulated in (López,2013), by means of an Arrhenius dependence on temperature. Here we adopt the approach described in (Chiariello,2010), where the model considers Wiedemann–Franz (WF) contribution in mesoscopic conductors:

$$\kappa_{CF}(T) = \sigma_{CF}(T) \cdot L \cdot T, \tag{III.17}$$

where $L = 2.44\ 10^{-8}\ \mathrm{W} \cdot \Omega \cdot \mathrm{K}^{-2}$ is the WF Lorenz constant value, and $\sigma_{CF}(T)$ is the electrical conductivity of the Ni^+ CF, which can be modeled as (Kim,2014),

$$\sigma_{CF}(T) = \frac{\sigma_{CF0}}{1 + \alpha_{CF}(T - T_0)}, \tag{III.18}$$

where σ_{CF0} is the electrical conductivity at $T_0 = 300K$ and α_{CF} is the temperature coefficient, with values in Table III.1. Besides, the electrical conductivity for Nickel bars is assumed to be temperature-independent (e.g., $\sigma_{Ni}(T) = \sigma_{Ni}$), whereas for copper it can be again expressed as in (III.2), which α_{Cu}value is listed in Table III.1 at T_0. Note that such values take into account the size effects of the sub-micron dimension of the conductors, e.g. (Wilhite,2014). All the other parameters are almost constant with the temperature and are given in Table III.1, taken from (Kim,2014) and (Luo,2016).

Table III-1 RRAM Geometry and Parameter Values at T=300 K.

Material	CF	diode			BL/WL			HfO_2
		TiO_2	Pt	Ti	Ni	Cu	CNT	
Width (nm)	16	80			80			80
Height (nm)	80	50	30	30	30			80
κ $Wm^{-1}K^{-1}$	22	33.8	8.31	21.9	22	380	200	0.9
c $Jkg^{-1}K^{-1}$	445	133	710	523	455	400	700	286
σ $(S.m^{-1})$	0.12M	3.07k (ON) 50m (OFF)	9.65M	2.5M	0.12M	33.5M		0.7u
α (K^{-1})	1.4m	--------			2.7m (Cu)			----
ρ $(kg.m^{-3})$	8.9m	19.8K	4.2K	4.5K	8.9k	8.9k	1.6k	9.7k

As for the other materials, the experimental behavior of κ(T) is provided in (Panzer,2009) for the metal oxide TiO_2 film, and in (Hui,2017) for that in HfO_2. In both cases, it can be fitted as follows (Russo,2009):

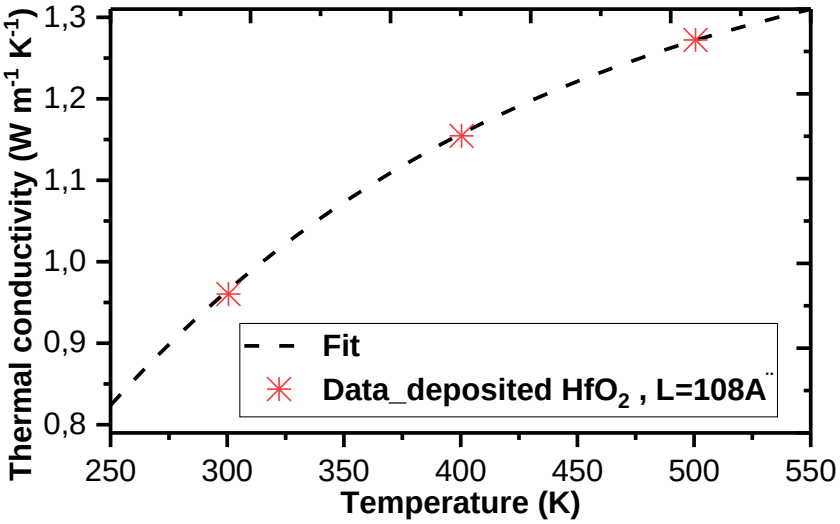
$$\kappa(T) = a_1 \exp(-b_1 T) + a_2 \exp(-b_2 T) + c, \qquad \text{(III.19)}$$

whose fitting coefficients $a_i, b_i; i \in \{1,2\}$ and c are in Table III.2. The thermal conductivity for all the other materials is almost constant with *T*, with the values given in Table III.2.

Table III-2 Fitting Coefficients of the Thermal Conductivity.

Parameters	a_1 $W.m^{-1}K^{-1}$	a_2 $W.m^{-1}K^{-1}$	b_1 K^{-1}	b_2 $10^{-3}K^{-1}$	c $W.m^{-1}K^{-1}$
TiO_2	230.2	22.3	0.037	6.5	5.1
HfO_2	0.14	-2.2	10.6	5.2	1.4

(a)



(b)

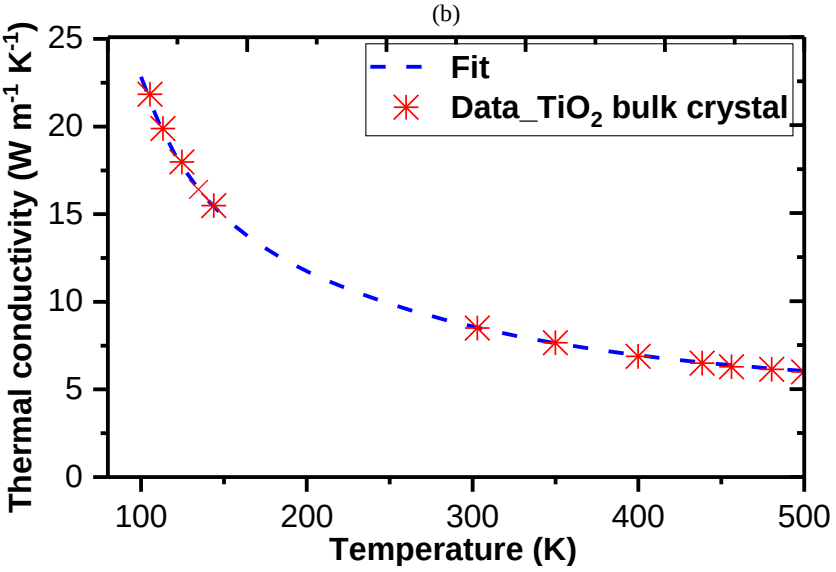


Figure III-5 Temperature-dependent thermal conductivity of: (a) TiO_2 (Ahn,2018) (b) HfO_2 (Liang,2019).

It should be mentioned that $\kappa(T)$ is measured up to 500 K, while the maximum temperature in our simulation exceeds this range. However, the bi-exponential equation given by (III.3) can be still effective, because the metal-oxide thermal conductivity tends to saturate at higher temperature.

The experimental results refer to the 1R RRAM studied in (López,2013). Here we use the proposed model to reproduce the behavior of the temperature of the CF as a function of the RESET voltage applied to the electrodes. In the 1R structure, the application of the RESET voltage produces a CF temperature increase until a critical value T_{crit} is reached, at which the filament dissolution occurs, resetting the device. The geometrical parameters and the sweep voltage have been set according to the data provided in (Luo,2016; López,2013). The only parameters that have been here tuned to fit the experiment are: the filament width and the resistive temperature coefficient α_{CF} appearing in expression (III.2). Their values are reported in Table III.1. In Figure III.6 the numerical solution obtained by the COMSOL model (dashed line) is successfully compared to the experimental ones (dots), provided in (López,2013).

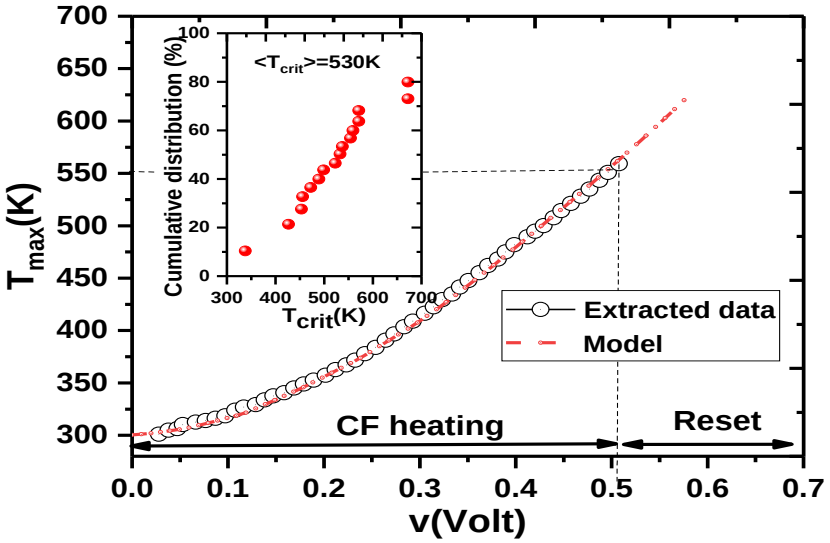


Figure III-6 Experimental validation of the model applied to the 1R-RRAM in (López,2013): CF temperature as a function of the voltage applied to the Conducting Filament: model solutions (dashed line) vs experimental data (white dots).

The second benchmark case-study is provided by 1×3×2 1D1R X-bar structure analyzed in (Luo,2016), with a row of RRAM that is active and another row that is passive. The computed transient behavior of the maximum temperature in the active and passive cells is shown in Figure III.7, successfully compared to the numerical solution given in (Luo,2016), with an error < 4.3 %.

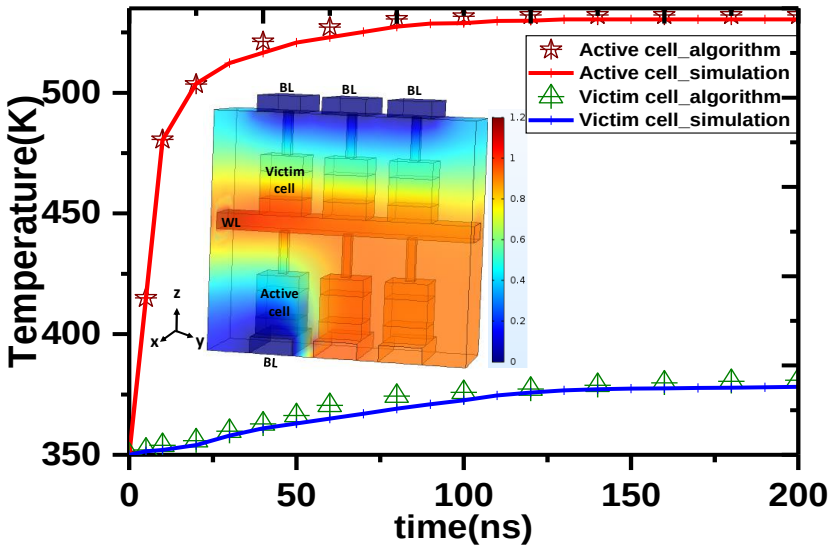


Figure III-7 Numerical validation of the model applied to the 1D1R-RRAM 1x3x2 array in (Luo,2016): active and passive cell maximum temperature as a function of time: our model (solid lines) vs model in (Luo,2016). (crosses and triangles).

III.4.2 Modelling a single RRAM cell: carbon nanotube electrodes

Given their outstanding physical properties, novel carbon-based nanomaterials such as Carbon Nanotubes (CNTs) or Graphene Nanoribbons (GNRs) have been recently proposed to realize new architectural solutions for RRAM devices (Kim,2012). This work investigates the use of these materials within the RRAM architectures in Figure II.10, to realize the WL/BL. Indeed, superior signal and thermal integrity performance have been demonstrated for CNT or GNR interconnects (Maffucci,2016 ; Slepyan,2015).

However, semiconductor industry is seriously taking into consideration the possibility to replace conventional materials with innovative ones, such as CNTs

(Maffucci,2016). Indeed, CNTs exhibit outstanding properties, such as: high current carrying capability, up to 10^8-10^9 A/cm^2, orders of magnitude higher than copper; large electron mean free path, of the order of hundreds of μm, to be compared to the few tens of nm in Cu; high Young Modulus of about 1 TPa, 5 times higher than for stainless steel; excellent thermal conductivity, up to values of about 3500 $W.m^{-1}K^{-1}$, whereas for Cu it is usually about 400 $\mathrm{W.m^{-1}K^{-1}}$.The electrical resistance of a single shell CNT of length l may be expressed as follows (Forestiere,2010; Maffucci,2017):

$$\mathrm{R(T)} = \frac{\mathrm{R_0 + R_p(T)}}{\mathrm{M(T)}} + \frac{\mathrm{R_0}}{2\mathrm{M(T)}}\frac{\mathrm{l}}{\mathrm{l_{mfp}}}, \qquad \text{(III.20)}$$

where l_{mfp} is the electron mean free path, M is the number of conducting channels, $R_0 = 12.9k\Omega$ is the quantum resistance and R_p is a parasitic term. The first term in (III.20) is the so-called contact resistance, whereas the second term is a distributed term, the intrinsic resistance, which vanishes for short lengths, $l \ll l_{mfp}$, i.e., in the ballistic transport regime. The contact resistance is given by two terms: the term R_0/M is always present, as long as the CNT is connected to a different conducting material at its terminals.

The number of conducting channels M depends on the CNT diameter, chirality and temperature, as shown in Figure III.8: here M is plotted for a metallic and a semiconducting CNT shell versus CNT diameter D, for two temperature values (Maffucci,2013). Typical single-wall CNT (SWCNT) diameters are of the order of few nm.

In order to realize CNT electrodes for the RRAM device under investigation, in the following we assume a bundle of N_b MWCNTs fed in parallel, thus lowering the huge value of resistance of single CNT. Statistically, 1/3 of the CNT shells are metallic and the other are semiconducting. Let us consider a total of N_b MWCNTs in the bundle, each of them characterized by an outmost shell diameter $Dout$ which is usually 2-4 times larger the inmost shell diameter D_{out}. Such diameters fall in a range where both metallic and semiconducting shells contribute to the conduction, according to Figure III.8. Therefore, the bundle resistance is given by (III.20), where

M is computed by summing over all the N_s shells for each individual MWCNT, and over the number of CNTs in the bundle:

$$M(T) = \sum_{i=1}^{N_b} \sum_{k}^{N_s} M_{i,k}(T), \qquad \text{(III.21)}$$

where $M_{i,k}(T)$ refers to the k^{th} shell of the i^{th} CNT in the bundle, of diameter $D_{i,k}$.

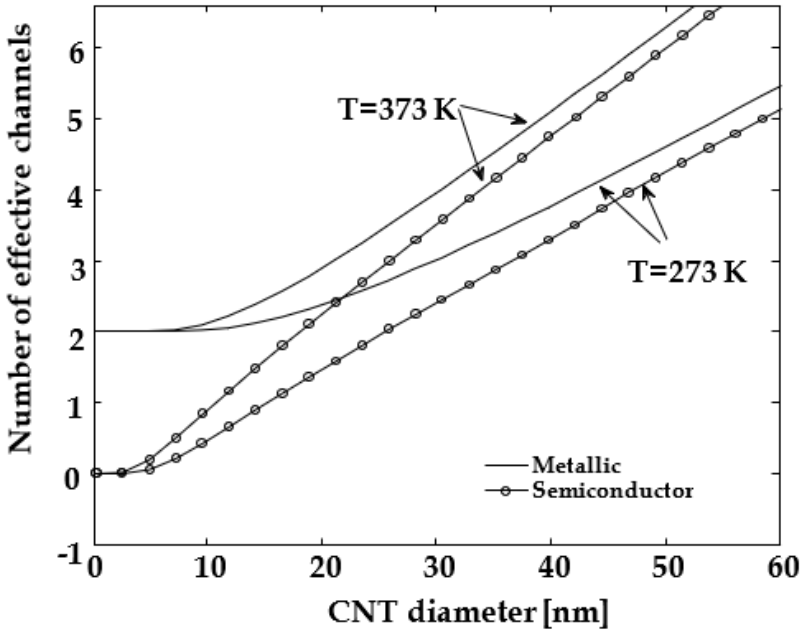


Figure III-8 Equivalent number of conducting channels for metallic (armchair) and semiconducting (zig-zag) CNTs, at two different temperatures.

In a CNT interconnect there are two counteracting mechanisms as temperature increases: from one hand, R should increase since $lmfp(T)$ decreases, whereas, $R_{CNT}(T)$ should decrease since $M_{i,k}(T)$ increases. The balance between these counteracting factors can provide an excellent thermal stability (Maffucci,2013). Once calculated the bundle resistance, $R_{CNT}(T)$, the equivalent electrical conductivity can be obtained as (III.23) and can be fitted by means of formula (III.19), providing the results in Figure III.9.

$$\sigma(T) = l/R(T)S \qquad \text{(III.22)}$$

Taking into account the WL/BL dimensions in Table III.1, we assume a densely-packed bundle of 10 identical MWCNTs, with D = 16 nm and 24 total shells (Chiodarelli,2013). As for the contact resistance, we should take into account a CNT/Ni contact, since the CNT bundles cannot completely replace the Ni bars, otherwise, it would be not possible to create the filament.

Therefore, we assume the presence of a small Ni electrode at the top of the RRAM cell. Unfortunately, huge contact resistances for CNT/Ni electrode are reported, in the range of $M\Omega$ (An,2012). Here, we assume the following model for the contact resistance:

$$R_c(\mathrm{T}) = \beta(\mathrm{T} - T_0) + R_{c0} \qquad \text{(III.23)}$$

with $\beta = 13\ \mathrm{K}\Omega$ and $R_{c0} = 30\ \mathrm{K}\Omega$ at $T{=}T_0{=}300\mathrm{K}$. Although lower values of contact resistance may be obtained for instance by using rapid thermal annealing (Magnani,2016), we assume here the above conservative values, in view of studying realistic cases. The resulting equivalent conductivity is fitted by (III.19) as in Figure III.9, with $a_1 = 2.5\ GS.m^{-1}$, $a_2 = 1\ GS.m^{-1}$, $b_1 = 9.6\ m.K^{-1}$, $b_2 = 2.2\ m.K^{-1}$ and $c = 5.64\ MS.m^{-1}$. The values of the conductivity at 300K are in Table III.1.

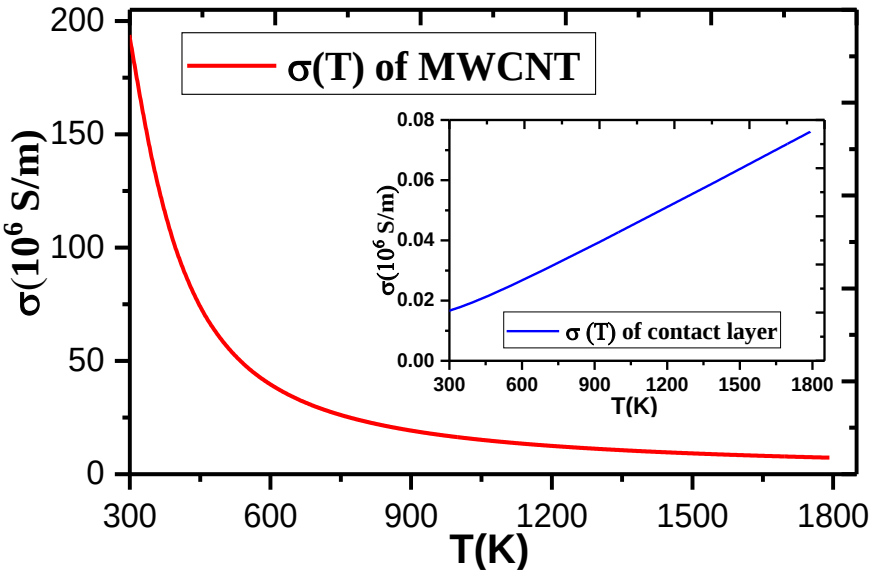


Figure III-9 Equivalent electrical conductivity of the bundle of multi-walled CNT. INSET: equivalent electrical conductivity for the contact layer (Zayer,2019).

The thermal conductivity of isolated CNTs can reach values as high as 3300 $\mathrm{W.m^{-1}.K^{-1}}$, but when they are bundled this value is strongly reduced, depending on the bundle quality (for instance, density, alignment, defects, and so on…). Once again, to study a realistic case with a standard bundle quality, here we consider the value of 200 $\mathrm{W.m^{-1}.K^{-1}}$, the lower one reported in (Forestiere,2010). All the other parameters have been given in Table III.1.

III.4.3 Modelling a single RRAM cell, improved conductive filament model

As pointed out in the introduction, the starting point of our analysis is the 1D-1R cell given in Figure II.10b. In order to introduce the multiphysics model and its parameters, it is needed to provide here a short description of the physical mechanisms leading to the destruction of the conducting filament (CF), hence to the switching from LRS to HRS (i.e., RESET).

In the considered cell, the formation/dissolution of the CF is a complex mechanism dictated by thermochemical reactions, including localized redox processes (Larentis,2012; Ielmini,2015), and ion migration. The SET and RESET mechanisms may be described through defect migration (e.g., excess hafnium and oxygen vacancies) induced by the local values of electric field and temperature (Ielmini,2011). During the SET process, the ions are emitted from the active electrode and migrate through the oxide, under the action of a voltage bias applied to the active electrode (anode, positive top electrode, TE), whereas the bottom electrode, BE, is grounded (cathode). The LRS state reached by the cells after the CF is formed is also responsible for Joule heating that greatly increases its temperature, and provides the thermal energy necessary to facilitate ion migration. In the RESET process, the filament rupture is a consequence of a thermal effect: it ends up breaking due to the high temperature and the device turns back to HRS. The actual conditions that determine the rupture may significantly change from one RRAM to another one, for instance, due to a different metal oxide (Cho,2006; Mattioli,2008; Jeong,2008; Marucco,1981). If the temperature increases as a consequence of the cell's self-heating, these conditions can be achieved by applying a minimum voltage level,

typically V_{RESET} = 0.53 V (Lahbacha,2020; Li,2017; Russo,2009). However, the conditions for resetting a single cell can also be reached in absence of any voltage applied to that cell, as a consequence of a thermal exchange from the nearby cells. In this case, an unwanted RESET occurs, and hence the thermal crosstalk leads to the device failure.

Since the final goal of this study is to compare different architectural arrangements of cells, rather than to study the single cell, a simplified model for the single cell has been here used. As detailed in the next paragraph, the formation/dissolution of the CF is simply described by an equivalent CF conductivity, that models the gradual and smooth transition between LRS and HRS occurring during the RESET, following a non-linear law with respect to temperature. The V-I characteristic curve of such devices is known to be highly non-linear. In our simplified model, a linear approximation is used for the LRS and HRS, that can be adopted if we limit our analysis to the branch of the V-I curve that refers to the RESET operation, as shown in (Russo,2009). With the above-mentioned limitations, this simple model is suitable for our purposes for perform the signal and thermal integrity analysis.

A crucial temperature-dependent parameter is given by the equivalent electrical conductivity to be associated to the CF in the oxide. Compared to previous works done by the Authors (Zayer,2019; Zayer,2020), and (Lahbacha,2020), here the CF conductivity model is improved, to properly account for the variation of the conductivity while the RESET switching is in progress. To this end, the conductivity of the CF is formulated as:

$$\sigma(\mathrm{T}) = \sigma_1 \left(1 - \frac{1}{1+\left(\exp\left(-B(T-T_{CRIT})\right)\right)}\right) + \sigma_2, \qquad \text{(III.24)}$$

This equation describes a smooth transition from high (σ_1) to low (σ_2) conductive states (see Figure III.10). The parameters appearing in (III.24) strongly depend on the CF status, as for instance the filament actual geometry and the local doping. In the following, we assume the values $\sigma_1 = 3.3 \cdot 10^5\ \Omega^{-1}m^{-1}$ and $\sigma_2 = 10^3\ \Omega^{-1}m^{-1}$, corresponding to a typical dopant density of the CF (Larentis,2012; Park,2010), and the value of the critical temperature T_{CRIT} = 550K taken from (Lahbacha,2020; Li,2017; Russo,2009). This parameter is the mean value of the temperature range where the transition occurs. In this way, we can take into account a statistical distribution of the RESET, that can actually take place for different temperature values around T_{CRIT}. Here, a uniform distribution is assumed in the range $T_{CRIT} \pm 20\%$, obtained by putting $B = 0.153$ in (III.24).

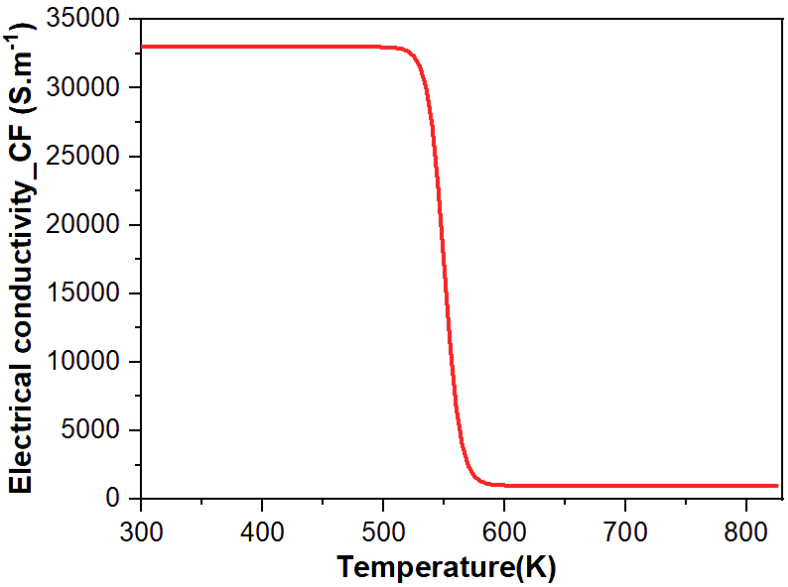


Figure III-10 Temperature-dependent electrical conductivity of the conductive filament (Ni).

The electrical conductivity of the metal oxide HfO_2, is assumed to be thermally activated by Arrhenius equation (Ielmini,2011):

$$\sigma(T) = \sigma_2 \exp\left(-\frac{E_{AC}}{k_B T}\right), \qquad \text{(III.25)}$$

where σ_2 is a pre-exponential factor, $E_{AC} = 0.05$ eV is the activation energy for insulating conduction, k_B is Boltzmann's constant, and *T* is the local temperature.

Next, the thermal conductivity of the surrounding medium HfO_2 is here modeled as in (Panzer,2009),

$$k_{HfO} = k_{HfO0}(1 + \lambda(T - T_0)), \qquad \text{(III.26)}$$

where k_{HfO0} is the value at $T_0 = 300\,K$, and $\lambda = 10\,mK^{-1}$, is the linear thermal coefficient.

In the temperature range of interest for this work (300 K – 1500 K), the thermal conductivity of the CF can be assumed to be constant, with the value provided in Table III.2 (Milošević,2006). Note that this value may change slightly from metal to metal.

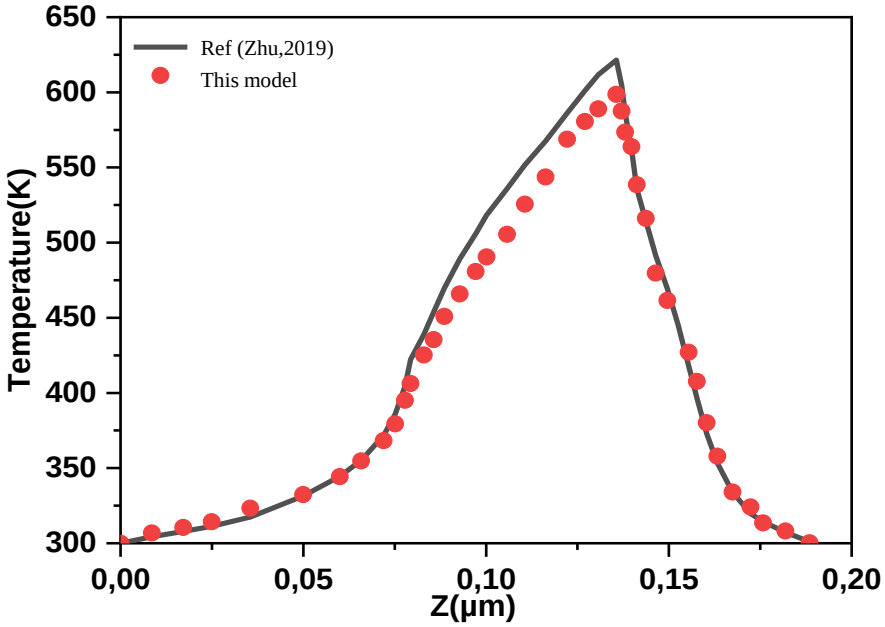


Figure III-11 Model comparison: temperature values computed at the center of a RRAM 1D-1R cell along the vertical axis (z-axis), by means of our model (red dots) and compared to the results in (Zhu,2019) (black line).

Nevertheless, an adaptive tetrahedral mesh is used to implement the numerical model. A proper mesh assessment has been carried out for each simulation, by refining step by step the mesh element size in order to ensure good convergence. The finally adopted mesh has been chosen so to provide a relative error on the estimated maximum temperature less than 0.3%.

In order to compare the Multiphysics model based on Ni metal proposed here to the results available in the literature, the 1D-1RRAM cell studied in (Zhu,2019) was implemented, where the details of geometry and material parameters can be found. The results obtained with the proposed model are successfully compared to those provided in (Zhu,2019), as reported in Figure III.11. In details, Figure III.11 plots the steady-state temperature at the center of the structure, along the vertical axis of the device (z-axis), after a RESET signal of voltage 1.6V.

III.4.1 Assessment of the FEM solution: mesh size and sensitivity

The purpose of the mesh sensitivity study in 3D 4×4×4 crossbar RRAM is to determine a mesh trade-off between the accuracy of the results and the computation time of the simulation, in order to obtain recommendations on the optimal mesh. A tetrahedral mesh is used in the COMSOL software for discrete the domains of our 4×4×4 structures. Several sizes of the elements of the mesh are tested (Table III.3) in order to ensure good convergence. Figure III.12 shows the evolution in steady-state of the maximum temperature for different size mesh elements.

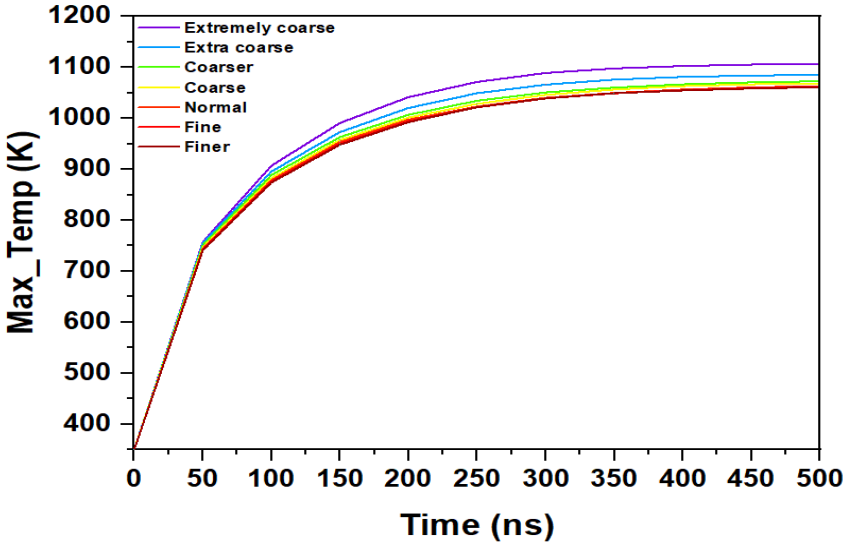


Figure III-12 Time evolution of the temperature rise for different size mesh elements.

As shown in Figure III.13, the maximum temperature varies as the dimensions of the element decrease and then reaches a value of stability. When the number of elements is low (Extremely coarse), the resulting solution deviates from the exact solution and the average relative error on the maximum temperature is of the order of 4% comparing with normal mesh. On the other hand, when the number of elements is greater than 20000, the effect of this number of the solution becomes very small and it can be concluded that the computer code has converged to the exact solution, then the error decreases again until 0.08% for the fine mesh. That clearly proves that convergence is indeed reached and that the normal mesh is the most adequate for this computation.

Table III-3 Illustrates the number of elements for each mesh.

Element size of Mesh	Extremely	Extra	Coarser	Coarse	Normal	Fine	Finer
Nb of elements	14451	15310	18701	25581	38488	52538	78006
Max Temp (K)	1106.9	1085.6	1072.8	1068.8	1063.5	1062.6	1061
The relative error/Normal mesh	4.08%	2.08%	0.87%	0.5%	--	0.08%	0.24%

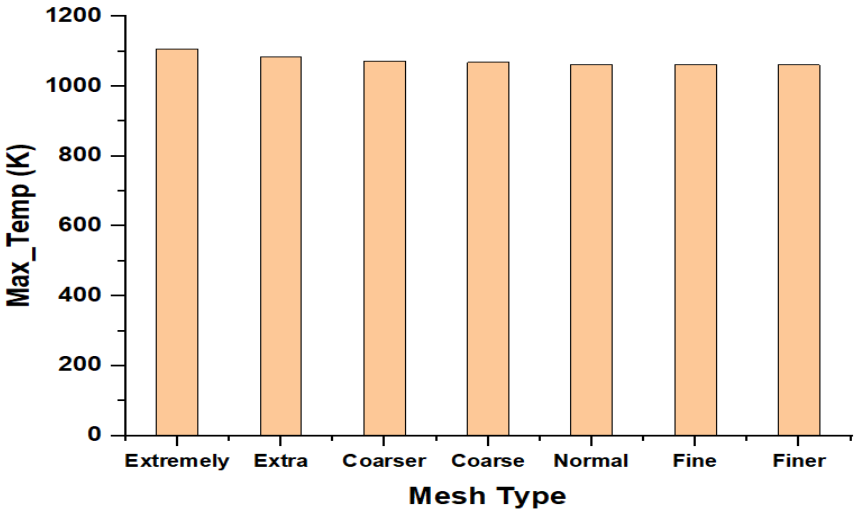


Figure III-13 Maximum temperature as function of mesh type.

Modeling of the electrical conductivity in the oxide and in the CF is necessary to solve equation (III.1). In fact, the CF presents the dopant region in the memory cell, where the formation and the rupture process are based on thermochemical reactions and then result in the change of resistance states. The unipolar switching behavior is adopted by the thermochemical mechanism, where the SET and the RESET are described through defect migration (e.g., excess hafnium and oxygen vacancies V_O) (Ielmini,2011) induced by the local electric field and temperature due to Joule heating. This migration is generated from the anodic interface under a positive top electrode (TE) bias to the cathode side is the bottom electrode (BE) which is grounded and then the formation of the conductive film (set process). In this step, the device is in the LRS, because usually, the film passes through the limited size of the small conductive channel, so the current density through the conductive channel is slightly larger, and then the resulting amount of Joule heat allows the conductive filament to greatly increase its temperature. This joule heating provides the thermal energy necessary to facilitate ion migration. Several metal oxide conductivities are characterized by the degree of non-stoichiometry of the forming filament (Cho,2006; Mattioli,2008; Jeong,2008; Marucco,1981).

III.5 Conclusions

- This chapter describes the method of coupling the electrothermal modeling for the electronic devices and then for our applications.
- The electrothermal model considered in this work for analyzing the physical model of the RRAM and of the graphene-strips, is described in detail from the electrical and thermal points of view, also the boundary conditions required to solve the system of the partial differential equation (PDE).
- The numerical implementation of this work is based on the finite element method (FEM) and implemented in COMSOL, where the mesh sensitivity is studied in order to estimate the optimal mesh.
- The implementation of the conventional physical model of the single RRAM cell is analyzed and validated against benchmarks in literature and

then an improved conductive model is described and also validated by implementing new formula describing the transition of conductive states.

- In order to replace the conductive materials (Nickel) of the interconnects by the Carbone nanotubes, a full description of the physical characterizations of the CNT parameters is presented.

Chapter IV : Electrothermal Analysis of 3D Crossbar Resistive Memories

IV.1 Introduction

In this chapter, a full 3D electro-thermal numerical model is used to analyze the signal and thermal integrity of 3D stacked RRAM arrays and to study solutions to the above-mentioned issues. In this multiphysics model (described in Chapter III), the electrical power dissipation is the heat source of the thermal problem and temperature-dependent electrical parameters are considered into the electrical one. In (Zayer,2019; Lahbacha,2020), the Authors have already demonstrated that issues like voltage drop and temperature rise may appear in 3D RRAM x-bar structures. In this chapter, a more detailed signal and thermal integrity analysis is provided for a large structure (for instance 5×5×5), also including the electrical effects of the thermal crosstalk. In addition, possible mitigation solutions are investigated, such as the use of different bias schemes and/or the use of novel nanomaterials as interconnects.

Compared to existing approaches in the literature, where the electrothermal analysis is carried out by checking the steady-state response after the application of a step-voltage bias (Zayer,2019), in this chapter a more realistic condition is analyzed, where the voltage waveform is a train of pulses, as shown in next Section.

The second target of this chapter is the proposition of the two novel architectures which are depicted in Figure IV.1, referring to a 4×4×4 array. The first one (Figure IV.1a), is based on reversing the 1D-1R cell from one layer to another one. Hereafter, it will be denoted as the “reverse architecture”. The second one (Figure IV.1d) is based on an elementary cell without the diode (Figure IV.1e): two memory cells are integrated into the array in such a way to realize two anti-serial resistive elements (Complementary Resistive Switching, CRS) sharing a thin common electrode (Lee,2010; Batude,2011). This structure will be hereafter denoted as CRS architecture. For all the considered architectures, we assume the whole 3D structure to be surrounded by Hafnium dioxide (HfO_2) which is not shown in Figure IV.1.

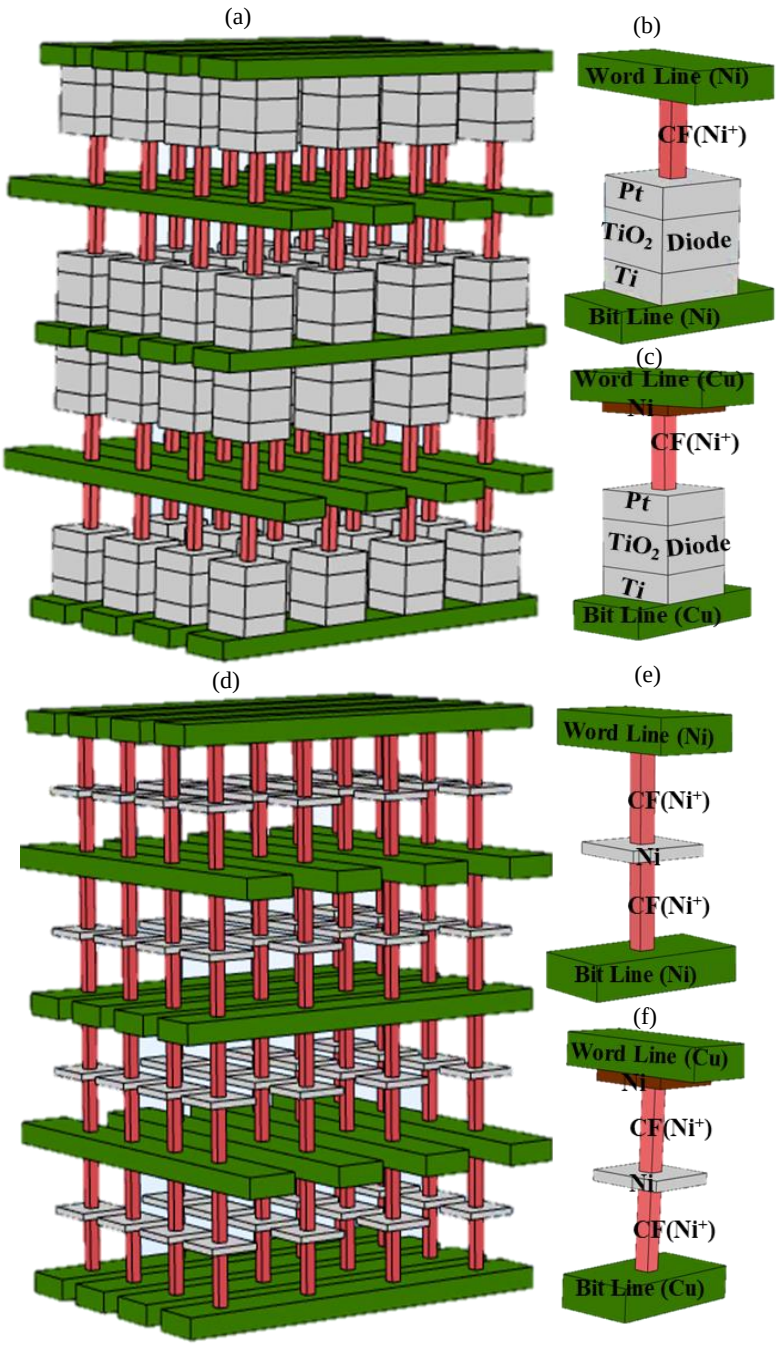


Figure IV-1 The novel proposed architectures for realizing a 4×4×4 RRAM array: a) 1D1R-1R1D reverse architecture; b) 1D-1R cell, with Ni bars; c) 1D-1R cell, with Cu bars and thin Ni layers; d) CRS architecture; e) CRS single cell, with Ni bars; f) CRS single cell,

Another novel contribution of this work is the study of the array performance when new materials are adopted to realize the bars to be used for BL/WL, conventionally made by Nickel. Toward this end, a conventional material (copper) and a novel nanomaterial (carbon nanotubes) are considered.

IV.2 Signal and thermal integrity analysis with conventional CF model

IV.2.1 Transient analysis of a single RRAM cell

Let us consider the single 1D1R RRAM cell in Figure IV.1b, with the dimensions in Table III.2. The typical RESET signal is made by a train of pulses: in each period there is a "write" pulse of a typical amplitude of about 1V, followed by a non-destructive "read" pulse, of typical amplitude of 0.1V, (Ahn,2018; Mattioli,2008). However, the electrothermal analysis in literature usually refers to the application of a DC voltage, rather than to the above train pulses, (Luo,2016; Zayer,2019). To highlight the difference, let us study the RRAM (with Ni bars), under a bias voltage described by: (i) a step function of amplitude 1.2V; (ii) a pulse train with the same amplitude, a period equal to 50ns and a duty-cycle, D= 50% (Figure IV.2a). In both cases, a rise- and fall-time of 2.5 ns is used. The maximum temperature of the device versus time is reported in Figure IV.2b: a step voltage highly overestimates the temperature.

However, the use of such a signal strongly reduces the computational cost. For this analysis, a mesh of about 6000 elements is needed, to assess the error below 1%. By using this mesh, the transient simulation in Figure IV.2 required 220s for the step voltage and 1215s for the pulsed one, on a 16 CPU-core and 32GB-RAM memory workstation. It is however possible to define an equivalent step voltage and avoid using the pulse train. To this end, we can express the maximum temperature reached after applying a bias voltage of amplitude V_p as:

$$T^{max} - T_0 = R_{th} P^J \tag{IV.1}$$

Here, R_{th} is the equivalent thermal resistance of the device and P^J is the dissipated Joule power, that can be expressed for the step and the pulse train voltage cases as:

$$P^J_{step} = \frac{V_p^2}{R_e}, \quad P^J_{pulse} = \frac{V_{trms}^2}{R_e}, \tag{IV.2}$$

where R_e is the equivalent electrical resistance of the device and V_{trms} is the true root mean square (TRMS) value of the voltage pulse, given by $V_{trms} = V_p\sqrt{D}$. From (IV.1) -(IV.2), it is:

$$T_{pulse}^{max} = DT_{step}^{max} + T_0(1 - D) \qquad \text{(IV.3)}$$

and hence the pulse voltage train can be replaced by an equivalent step voltage of amplitude equal to V_{trms}. The actual solution associated with the pulses, as shown in Figure IV.2b. In this case, this approach introduces an error of less than 4.5%.

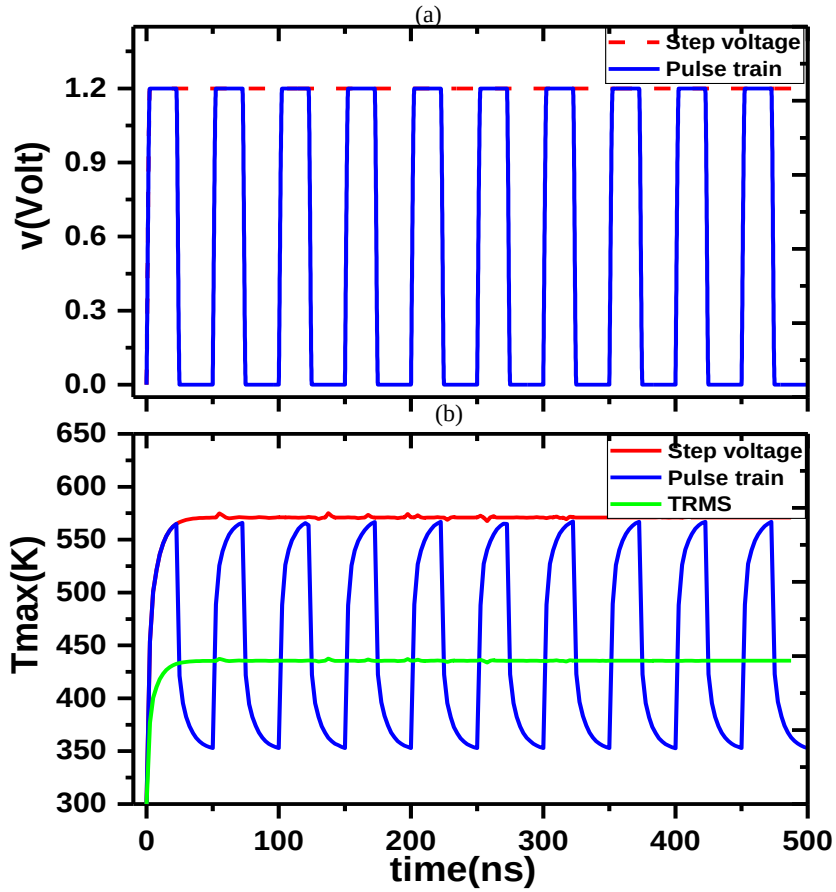


Figure IV-2 Transient analysis for a single RRAM: a) applied step and pulse train voltages; (b) corresponding maximum temperature for the two input signals and for the TRMS assumption.

The 1D1R RRAM cell is simulated under step and pulse electrical voltage signals in order to analyze the voltage and temperature distributions for the three interconnect cases. The WL and BL in the top and bottom layers of the memory cell

are assumed to be made by Ni, Cu and CNT interconnects, respectively. For the case of Cu and CNT, the TE is configured as Cu metal and as a bundle of multi-walled CNTs grown on a localized active Ni thin layer in the cross-sectional resistive switching cell by shrinking the sidewall Ni thin layer oxidation as depicted in Figures IV.3c), d) and Figures IV.3e), f), respectively.

An additional layer at the bias point (i.e., contact layer) is included to account for the effect of the lumped contact resistance for CNT/metal interfaces. Also, a Pd layer is added for the side contact between CNT and the active Ni metal with a contact resistance, $R_c(T) = 1.5k\Omega$. As a results, the voltage and thermal behaviors under step voltage are shown in Figure IV.3, where the Joule heating is generated with different dissolution rate for the different interconnect cases.

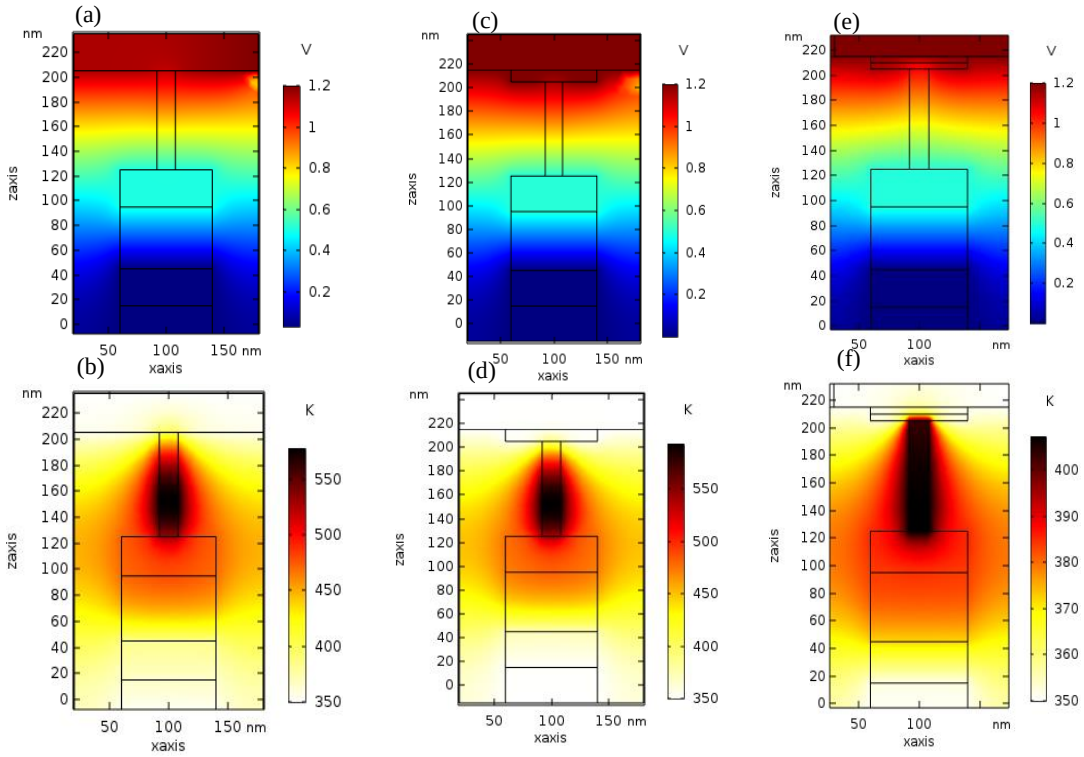


Figure IV-3 3D voltage and thermal distributions at steady state temperature for the 3D RRAM cell using the three case interconnects. a) and b) Ni, c) and d) Cu, e) and f) CNT interconnects respectively.

IV.2.2 Analysis of a 1D1R 5x5x5 RRAM crossbar architecture

In this part, a 5×5×5 RRAM crossbar structure is studied, where the cells in each layer are connected by WL and BL bars of length 0.8 µm (the cross-section dimensions are given in Table III.2). In the reference case, these bars are made by Ni and therefore they act both as the electrodes for each RRAM, and as the electrical interconnect routing the signals through the array. Alternative solutions are here investigated, consisting in leaving only a small layer of Ni at the top and bottom of each cell (to provide the active electrodes), but replacing it in the bars with another conventional conductor like Copper (Cu) or a novel conductor made by a bundle of MWCNT. The characteristics of CNTs are discussed in Chapter III and the physical parameters for Cu and CNT are reported in Table III.2.

The RESET switching is analyzed: in this case, all the cells are in the low resistance state, hence providing the highest current levels, and consequently the worst conditions in terms of voltage drop and heat production. The structure is fed as follows: the WL bars corresponding to the 1^{st}, 3^{rd} and 5^{th} layers are biased at one side or at both sides. The BL bars are instead grounded at one side or at both sides. Consequently, the RRAM cells belonging to 1^{st}, 3^{rd} and 5^{th} layers are active, whereas those belonging to the 2^{nd} and 4^{th} are passive. Given the above considerations, 4 different cases have been defined, as summarized in Table IV.1.

Table IV-1 Analyzed cases for the 5x5x5 RRAM crossbar array.

Case	Bar material	Bias level	WL terminal conditions	BL terminal conditions
1	Ni	1.8 V	one side biased, other side floating	one side grounded, other side floating
2	Ni	1.5 V	both sides biased	both sides grounded
3	Cu	1.2 V	as in Case 1	as in Case 1
4	CNT	1.2 V	as in Case 1	as in Case 1

As for the thermal management problem, here we assume that the conducting bars at the top (5th) and bottom (1st) layers are connected to a heat sink, imposing the fixed temperature of $T = 300\text{K}$.

Figure IV.4 illustrates the thermal distributions in the middle of the RRAM CFs in the 3rd layer which show the high temperature of the 5×5×5 structure. Simulation results shows that both cases of using Ni metal suffer from the problem of voltage drop, even the consideration of two side biasing scheme. As seen in Figure IV.4, due

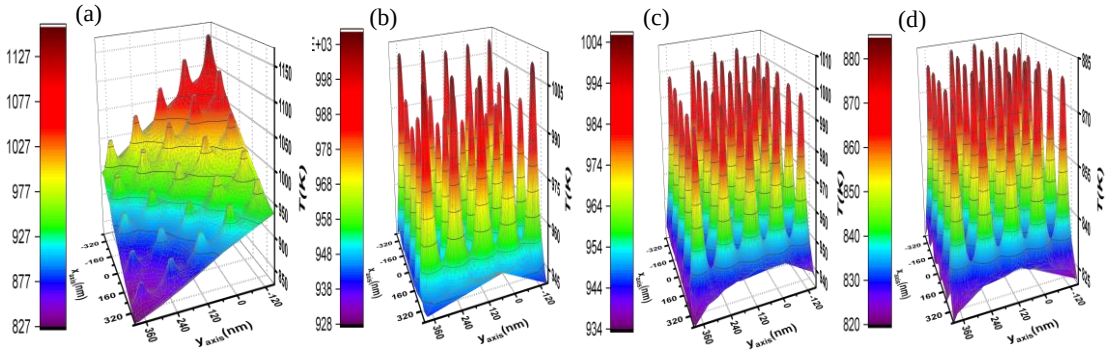


Figure IV-4 3D thermal distributions in the 3rd layer (active) of the 5×5×5 memory integration structure: thermal response along the middle of CFs for the considered four cases, respectively.

the high voltage drops when using Ni wires, most of the RRAM cells does not switch in the structure. This is why we see the highest temperature on the Ni electrode (Figure IV.4 a. In contract, for the cases of using Cu and CNT the highest temperature is located in the region of the filaments.

The computed 3D steady-state distributions of the voltage and temperature across the 5×5×5 structure are plotted in Figures IV.5 and 6, respectively, for the cases defined in Table IV.1. From Figure IV.5 it is evident that the Ni bars (cases 1 and 2) introduce a severe voltage drop, so that the voltage imposed across the CF strongly varies from the nearest to the farthest cell from the bias application point. The maximum and minimum voltage V_{CF} computed for each layer is reported in Table IV.2: for case 1, despite the high bias voltage (1.8 V), the furthest cells to the voltage supplier will not reset, being the V_{CF} below 0.5 V.

As for the layers #2 and #4, where the RRAMs are supposed not to reset, the electrical crosstalk is not so relevant, as shown by the low values of the induced

voltages reported in Table IV.2. Note that the results for the passive layers #2 and #4 are similar, as they share the same distance from the heat sink. The use of Cu (case 3) or CNT (case 4) bars may solve the problem: although the bias voltage is reduced to 1.2V, all the cells in the active layers correctly switch and the difference between the maximum and minimum values of V_{CF} is small.

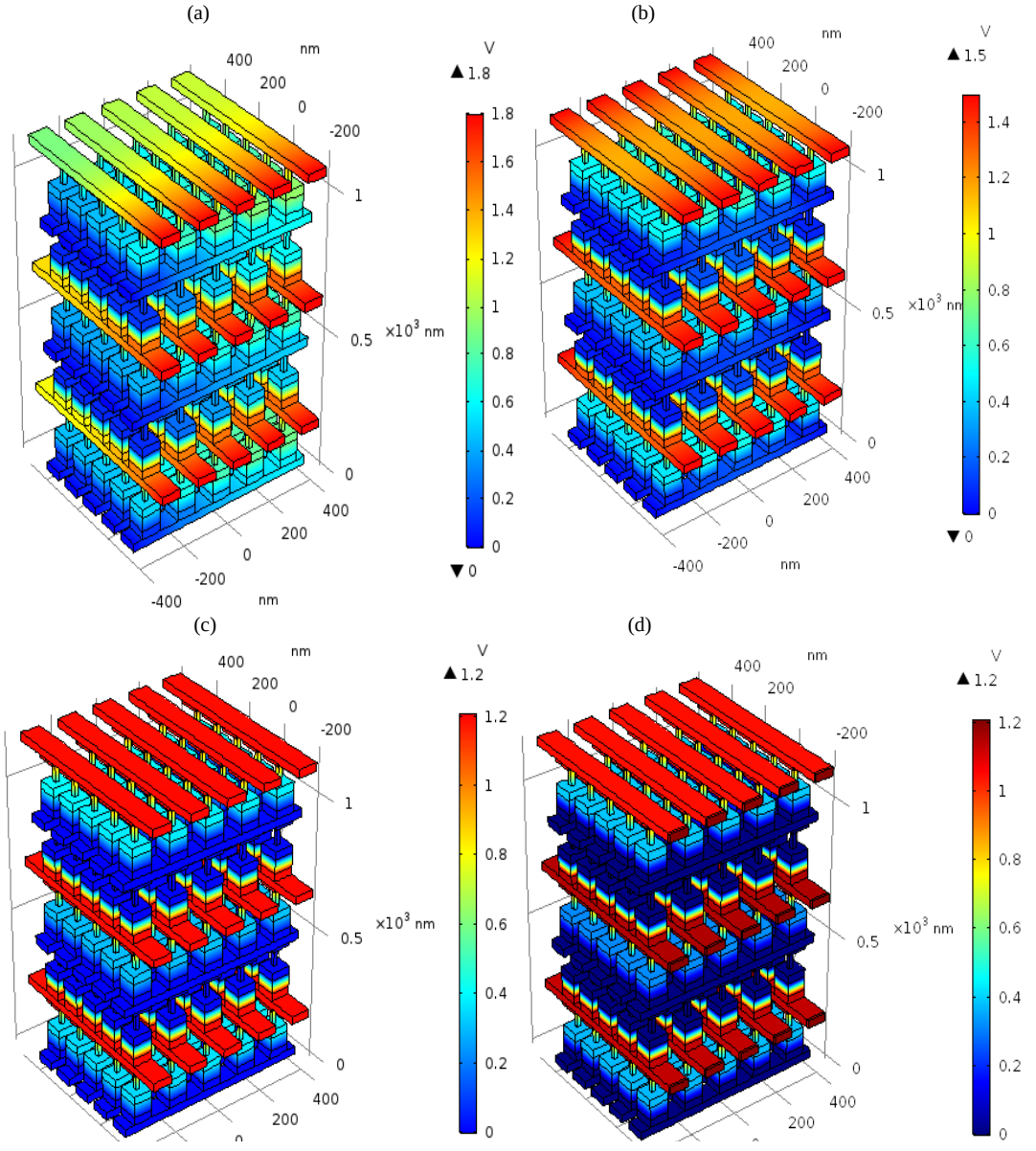


Figure IV-5 Computed steady-state voltage distribution in the RRAM X-bar structure, for the cases in Table IV.1; (a) case 1; (b) case 2; (c) case 3; (d) case 4.

As for the thermal behavior, Figure IV.6 shows that the use of Ni bars (cases 1 and 2) lead to a higher temperature rise, compared to Cu (case 3) or CNT bars (case 4). This is also shown in Figure IV.7, which plots the transient behavior of the maximum temperature value for the four cases. However, when the voltage drop is too high, the highest temperature may be found on the electrode rather than the filament, as the case of Ni bars, where many RRAM cells do not switch. The thermal performance of CNT and Cu solutions are comparable: in fact, these temperature ranges are within the CNTs material capability to maintain structural integrity, but not for Cu, being too close to its melting point. Besides, the contact resistances play a

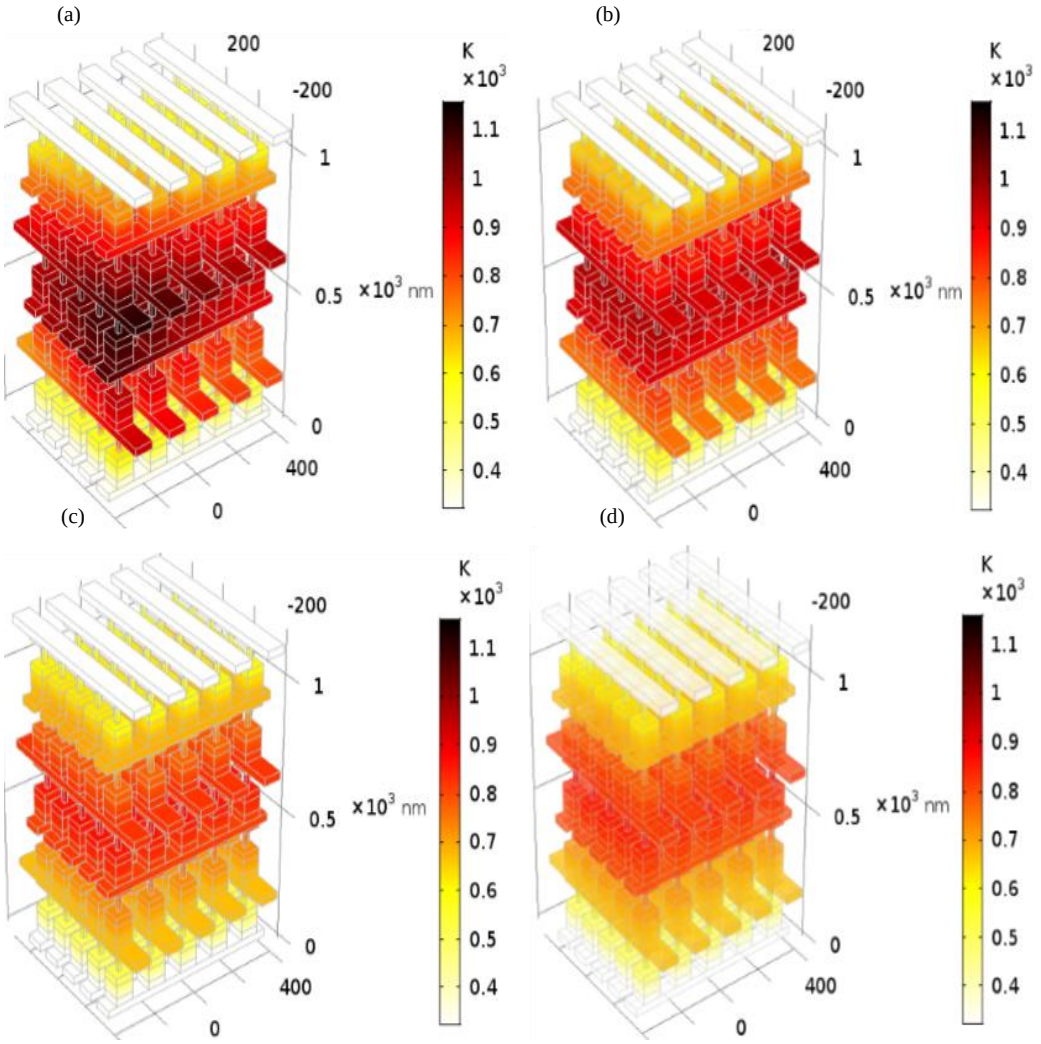


Figure IV-6 Computed steady-state temperature distribution in the RRAM X-bar structure, for the cases in Table IV; (a) case 1; (b) case 2; (c) case 3; (d) case 4.

crucial role for CNTs, as described in Chapter III. For larger structures (hence longer bars), the Cu performance worsens, whereas a better condition occurs for the CNT one, since the contact resistance becomes less important, due to the effect of ballistic transport (e.g. (Magnani,2016)). It is worth to note also that the ON-state resistance of the RRAM cells significantly affects the steady-state temperature. We have analyzed the case where the on-state resistance was increased by a factor of 10, and we found, as expected, that T_{max} is decreased from 575K to 425K in steady state.

Table IV.2 reports the maximum value of the steady-state temperature at the middle point of the CF of the cells of each layer: the inner active layer (#3) suffers

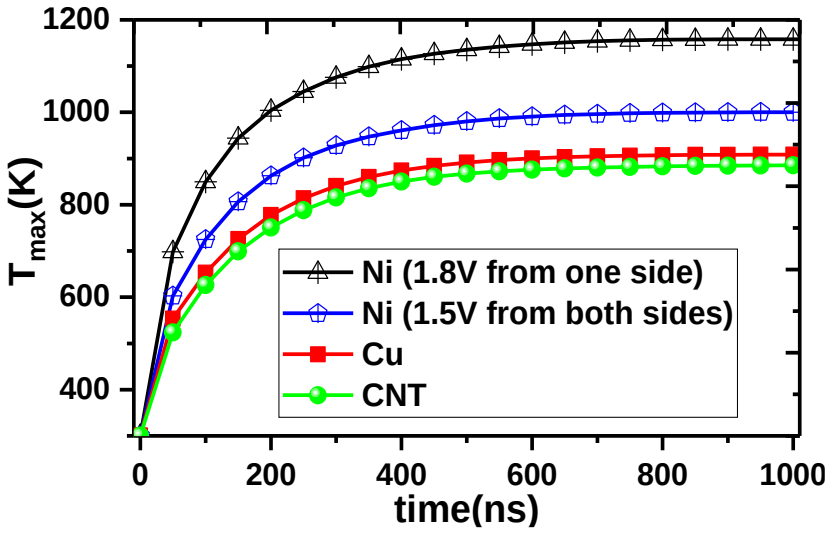


Figure IV-7 Maximum temperature computed in the 5x5x5 crossbar structure as a function of time, for the considered four cases in Table III.4.

from the highest temperature rise, being the farthest from the heatsink. The difference in the values of VCF of layer #3 compared to layers #1 and #5 is due to the higher temperature level reached by the CFs in the inner layers. The thermal crosstalk induces in the cells of passive layers (#2 and #4) temperature values higher than the critical value, T_{crit}. This means that these RRAM cells experience unwanted RESET switching, although the electrical crosstalk is negligible and the induced voltage is low. Indeed, a minimum level of voltage is needed only when an isolated RRAM is considered, where the temperature T_{crit} is reached by the self-production of heat, after the application of a suitable voltage level. However, while the thermal

crosstalk occurs severely at the large integration scale, the studied unipolar RRAM device and, in general, thermochemical memories, could be integrated into 3D x-bar structures only if the thermal crosstalk is alleviated. This requires, for instance, using advanced cooling solutions.

Table IV-2 Computed Metrics for the Signal and Thermal Integrity Analysis of the 5x5x5 crossbar structure.

Layer	Metric	Case 1	Case 2	Case 3	Case 4
#1 (active)	$V_{CF,max}$ [V]	0.96	0.85	0.82	0.73
	$V_{CF,min}$ [V]	0.51	0.74	0.79	0.72
	T_{max} [K]	840	738	662	662
#3 (active)	$V_{CF,max}$ [V]	1.12	0.96	0.87	0.81
	$V_{CF,min}$ [V]	0.67	0.86	0.86	0.80
	T_{max} [K]	1150	1010	904	884
#5 (active)	$V_{CF,max}$ [V]	0.86	0.74	0.8	0.62
	$V_{CF,min}$ [V]	0.36	0.61	0.7	0.61
	T_{max} [K]	618	574	560	540
#2 (passive)	$V_{CF,max}$ [µV]	0	165	-47.8	-38.8
	$V_{CF,min}$ [µV]	-740	-180	-72.8	-46.8
	T_{max} [K]	1000	872	769	767

Although many applications (e.g, neuromorphic and computer vision) benefit from recently demonstrated RRAM device characteristics and other memories (e.g. low energy/latency and low variation…), they always need high density of crossbar structures. The main issues analyzed here do not actually come from the single device behavior, but rather from the integration scheme (bias, interconnects, etc…). Therefore, even though other thermally induced memory devices are considered, these issues must be addressed as well. The issues tackled in our paper are proportional to the density of integration, rather than to the specific property of the single cell.

Regarding active layers in the 5×5×5 structure, both voltage level VL= [Max (Vt_{CF}-Vb_{CF}), Min (Vt_{CF} -Vb_{CF})] and v_{DR} are increased with respect to the 5×5×1 crossbar layer, where Vt_{CF} and Vb_{CF} refer to the voltage at the top and bottom of the RRAM CF, respectively. However, this could be interpreted as the following, the temperature of a given corss-point memory cell, TM in structure can be evaluated with Joule heating and heat dissipation as the following;

$$T_M = \int_{t_0}^{t_1} \frac{P_j - P_d}{c.V_{vol}} dt \qquad (IV.4)$$

where c is the heat capacity and V_{vol} is the volume of the active region in the memory cell. $P_j = R_e.i^2 = i.(V_{t\_CF} - V_{b\_CF})$ is the Joule heating power of RRAM device. $P_d = -A.\sum k_{th}\nabla T_M$ is the heat dissipation. A is the cross-sectional area of heat conduction, and ∇T_M is the temperature dispersion around the active region.

The temperature gradient ∇T_M in three directions (x, y, z) in 3D memory device leads to $\nabla T_M = T_M - T_0/D_M$, where D_M is the distance for T_M to decrease to T_0. At steady state temperature, the above-mentioned formulas lead to;

$$V_{t_{CF}} - V_{b_{CF}} = \frac{T_M}{c.V_{vol}} - A.\sum k_{th}\nabla T_M \qquad (IV.5)$$

Hence, as thermal crosstalk is more severe and higher reached T_M will results in a high potential level. (i.e., VL in the 3rd layer is higher than VL in the 1st and 5th active layers), fast diffusion of oxygen vacancies and further lead to the increase of R_e, even for victim cells. To this end, a possible solution may be to decrease the applied voltage across the WL wire in the middle layers to deals with the huge rise of temperature.

A further analysis on the thermal crosstalk is shown as the equivalent circuit presented in Figure IV.8a), where RHS is the thermal resistance of the heat sink to the ambient temperature T_0. Rthi is the thermal resistance of a given memory cell with a temperature T_i to T_0 along the heat dissipation path and P_{Ji} is the produced Joule heat, where "i" is the layer index. The derivative of heat transfer through the

crossbar structure is proportional to the negative gradient in the temperature and to the area, at right angles to that gradient, through which the heat flows. The thermal response for the thermal crosstalk along z-axis direction using the four considered case interconnects is presented in Figure IV.8b).

In fact, the asymmetric temperature distribution observation in the case of using Ni interconnect can confirm the voltage drop contribution to joule heat production. The use of Cu bars results the instability in managing the heat conduction, for instance, the temperature at steady state in the 1st and 5th layers show $T_{10} \approx T_{50} \approx 540 \gg T_0$. In contrast, CNT shows a reduced and uniform thermal distribution when compared to the other cases. The shown symmetric distribution with CNT wires is better from point of view heat removal with existing cooling systems in stackable chips.

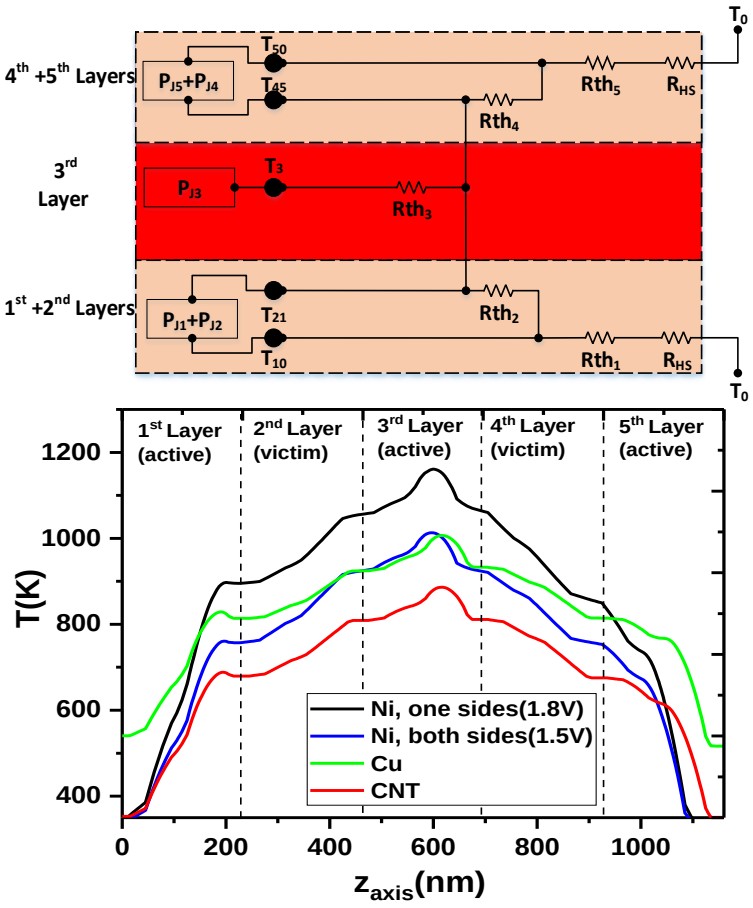


Table IV-3 Temperature profile in the 5×5×5 RRAM crossbar structure. a) Equivalent thermal crosstalk circuit. b) Thermal crosstalk along the z-axis direction at $W_{Diode}/2$ following TMAX point, ([x,y] (nm) = [-320,-128], [320,-232], [320,-128], [128,232] for the use of: Ni biased from one side, Ni biased from both sides, Cu and CNT, respectively.

However, thermal management can be done by using diamond, which is electrical insulator and good thermal conductor. In addition, dual-side heat sink can be used and/or through active and embedded cooling where a coolant is made to flow between the stacked active layers. Moreover, the reason why we propose CNTs instead of Cu is related to the manufacturability, since copper bars with such a small cross sections suffer from mechanical problems. Thus, the use of CNT nanowire is of great potential benefit for high-density RRAM arrays, when the signal and thermal integrity is the main concerns in memory design.

Although many applications (e.g., neuromorphic and computer vision) benefit from recently demonstrated RRAM device characteristics and other memories (e.g., low energy/latency and low variation…), they always need high density of crossbar structures. The main issues analyzed here do not actually come from the single device behavior, but rather from the integration scheme (bias, interconnects, etc.…). Therefore, even though other thermally induced memory devices are considered, these issues must be addressed as well. The issues tackled in our paper are proportional to the density of integration, rather than to the specific property of the single cell.

IV.3 Signal and thermal integrity analysis with improved CF model

IV.3.1 Analysis of 4×4×4 RRAM crossbar architecture

The two novel architectures proposed in this part are depicted in Figure IV.1, referring to a 4×4×4 array. The first one (Figure IV.1a), is based on reversing the 1D-1R cell from one layer to another one. Hereafter, it will be denoted as the “reverse architecture”. The second one (Figure IV.1d) is based on an elementary cell without the diode (Figure IV.1e): two memory cells are integrated into the array in such a way to realize two anti-serial resistive elements (Complementary Resistive Switching, CRS) sharing a thin common electrode (Batude,2011; Lee,2010). This structure will be hereafter denoted as CRS architecture. For all the considered architectures, we assume the whole 3D structure to be surrounded by Hafnium dioxide (HfO_2) which is not shown in Figure IV.1.

Besides investigating these new structures, this study also analyzes the advantages of using new materials and new biasing schemes. Specifically, it is proposed to realize the WL and BL bars by using Copper (Cu) and Carbon Nanotubes (CNT) instead of Nickel (Ni). In this case, a thin Ni layer is lying on the bundles of the carbon nanotubes and on the copper WLs (see Figure IV.1c and Figure IV.1f), so that the CF is still realized by Ni ions, as for the reference structure, as done in (Zayer,2020). Finally, bi-lateral biasing schemes are also investigated.

Before analyzing the performance improvement obtained by means of the novel RRAM architectures proposed in this work, we have first studied the conventional architecture so far proposed in the literature to realize a 4×4×4 crossbar array of 1D-1R cells (Sun,2015; Luo,2016). The conventional way to arrange 4 layers of 1D-1R memory cells in a vertical stack is that of placing the cells with the same polarity at each layer, and alternating a layer of word lines and a layer of bit lines. The WL bars are biased and connected to the reference electrode of each cell, whereas those of the bit lines are grounded, and connected to the reference electrode of each cell.

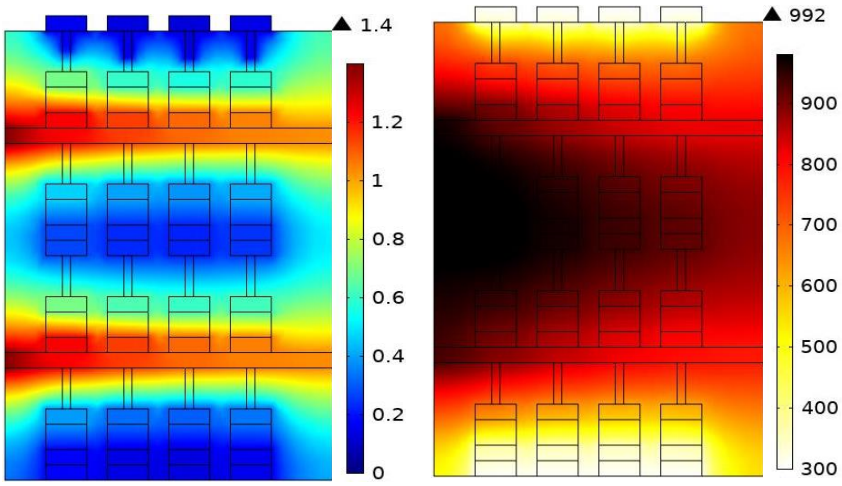


Figure IV-8 Reference architecture with Ni wires at the steady state: a) electrical potential distribution; b) temperature distribution.

This structure has been, for instance, studied in (Liang,2010; Huang,2012), where the promising features in terms of monolithic integration are highlighted, along with the potential issues related to the crosstalk noise. In (Zayer,2019; Zayer,2021), we have already proposed some possible solutions to mitigate these problems, based on

replacing the conducting materials of the WL and BL bars. Specifically, modelling results obtained by assuming both conventional conductors (like copper) or novel conducting materials (such as carbon nanotubes (Todri-Sanial,2017)) are suggesting the possibility to improve the structure's performance. As pointed out in the introduction, this work proposes to solve the signal and thermal integrity issues by moving to two alternative architectures, but also considering the possibility of replacing the Ni bars with Cu and CNT ones, as done in (Zayer,2019; Zayer,2020).

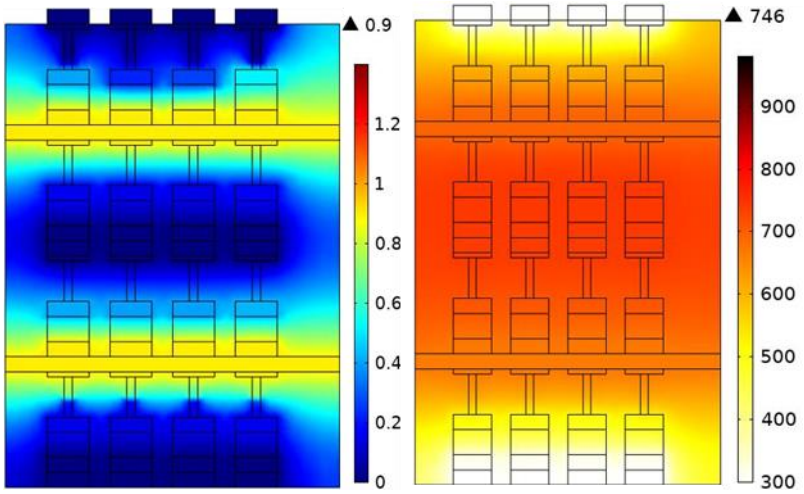


Figure IV-9 Reference architecture with Cu wires at the steady state: a) electrical potential distribution; b) temperature distribution.

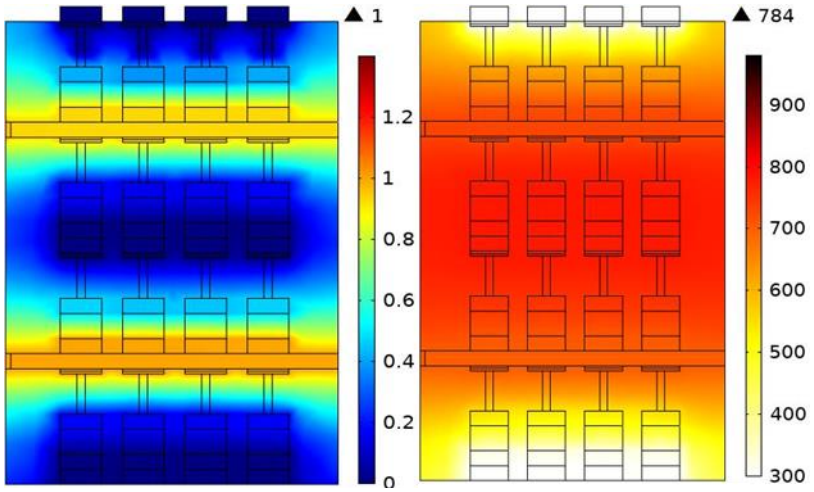


Figure IV-10 Reference architecture with CNT wires at the steady state: a) electrical potential distribution; b) temperature distribution.

The results of the analysis on this reference structure are given in Figures IV. 9,10, and 11 and refer to the distributions of the electrical potential and temperature at the steady state, for the case of Ni wires (Figure IV.9), Cu wires (Figure IV.10), and CNT wires (Figure IV.11).

The results in Figure IV.9 were obtained by considering a bias voltage of 1.4V, applied from one side of two WLs, which means that layers #1 and #3 are active (therefore they are supposed to RESET), whereas layers #2 and #4 are passive and thus they should maintain the SET state. The reason for a so high bias value is that of compensating the huge voltage drop along the Ni wires, which makes the voltage in the cells far from the bias point much lower than that of the nearest ones. Indeed, a bias of 1.4V is necessary to guarantee the minimum level of 0.7 V across the filaments of each cell, as reported in Table IV.4. This bias, however, leads to thermal integrity issues, since the cell temperature reaches values such as all the cells are resetting, including those in the passive layers, as shown in Figure IV.6b and reported in Table IV.5.

As pointed out, a way to mitigate this issue is to replace the WL and BL nickel bars with copper and carbon nanotubes ones, leaving a small layer of Ni at the top of each cell to provide the active electrode. Moving to Cu and CNT bars, the bias needed to provide the minimum RESET voltage to all cells may be lowered to 0.9V and 1V respectively, as shown in Table IV.4. Indeed, Figure IV.10a and 11a show an excellent degree of uniformity in the voltage distribution over the Cu and the CNT crossbar lines when compared to Ni interconnects. As for the thermal response, Figures IV.10b and 11b show a clear decrease in terms of maximum temperature when using Cu and CNT compared to Ni bars (Figure.9b). This solves the problems of unwanted RESET in layer #4 but not in layer #2, where the temperature still higher than the critical value is about 729 K and 771 K respectively for Cu and CNT.

To summarize, in this conventional reference structure, the heat generation induced by the active layers can change the state of the victim RRAM cells, as an effect of thermal crosstalk, which leads to unwanted RESET operations.

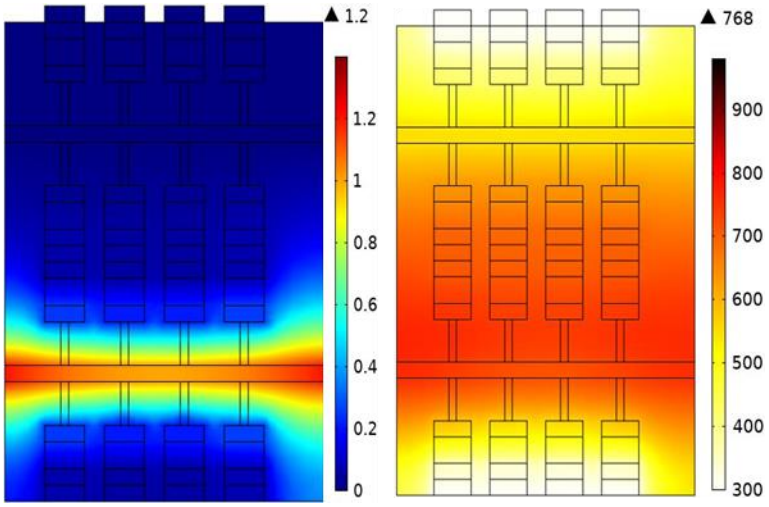


Figure IV-11 Reverse architecture with Ni wires at the steady state: a) electrical potential distribution; b) temperature distribution

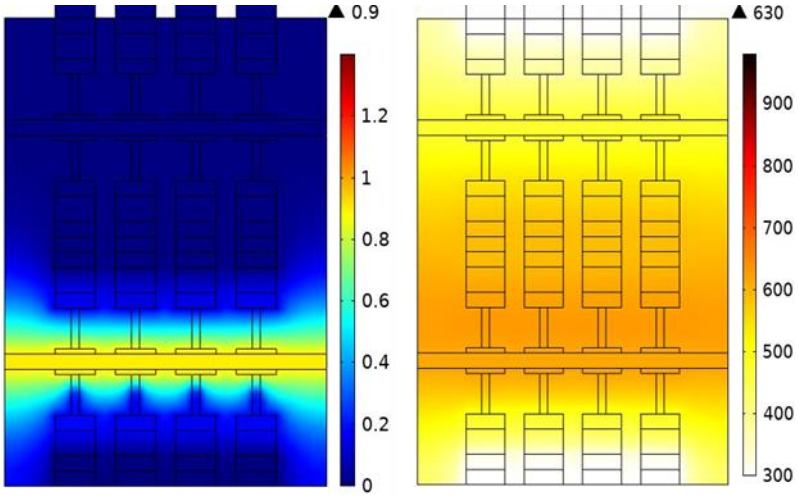


Figure IV-12 Reverse architecture with Cu wires at the steady state: a) electrical potential distribution; b) temperature distribution.

The same kind of analysis has been carried out on the two alternative architectures depicted in Figure IV.1. To compare the performance in the same conditions, we assume here again a biasing condition leading to two active layers and two passive ones. Note that in the reverse architecture (Figure IV.1a), in order to switch two layers, it is sufficient to apply the bias to only one WL. In other words,

the first main advantage of this solution is the possibility to double the number of cells that can be driven by a single biased interconnect layer. Given this consideration, now the active layers are #1 and #2, and the passive ones are #3 and #4.

The electrical potential and the temperature distributions of the 1D1R-1R1D reverse architecture are given in Figures IV.11,12, and 13 for Ni, Cu, and CNT bars, respectively. In the case of Ni bars, the voltage drop requires the application of minimum bias voltage of 1.2V at both sides of the WL, as shown in Table IV.4. Instead, the use of Cu and CNT in this reverse structure has advantages in terms of bias, since it can be applied from one WL side only, with a lower level (0.9V and 1V respectively), then improving the energy efficiency with respect to the Ni case, see Table IV.4. As for the thermal distributions in Figures IV. 12b and 13b, once again the use of Cu and CNT reduces the temperature inside the structure, and in particular inside the cells of the passive layers. As for the reference case, it is evident that the steady-state temperature rise follows the increase of the voltage level. The high voltage level required on the Ni wires reduces the energy efficiency and increases the Joule power dissipated into the conductors, leading to unwanted RESET switching.

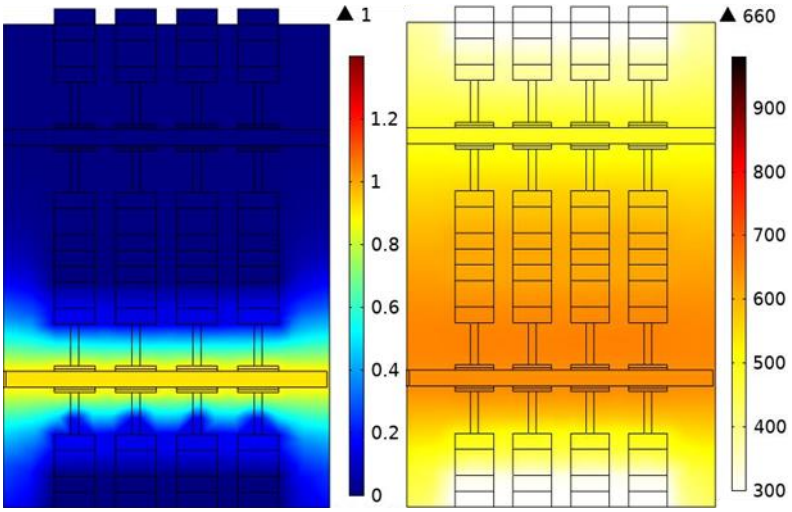


Figure IV-13 Reverse architecture with CNT wires at the steady state: a) electrical potential distribution; b) temperature distribution.

Table IV.5 clearly shows that the reverse architecture with Ni still has thermal crosstalk problems (cells of layer #3), whereas they are completely solved with the Cu and CNT bars.

The second architecture proposed here is the complementary one (CRS), see Figure IV.1d, presented in the introduction, where two anti-serial memristive elements share a common electrode. When the voltage is applied to the WL of the upper cell and to the ground of the BL of the lower one, both cells are activated. This offers an interesting perspective for solving the problem of the sneak path, without the introduction of any selector element, like the diode seen in the cells so far studied. The CRS cell presents a high overall resistance once, storing bit data, it effectively limits the leakage current in crossbar structures.

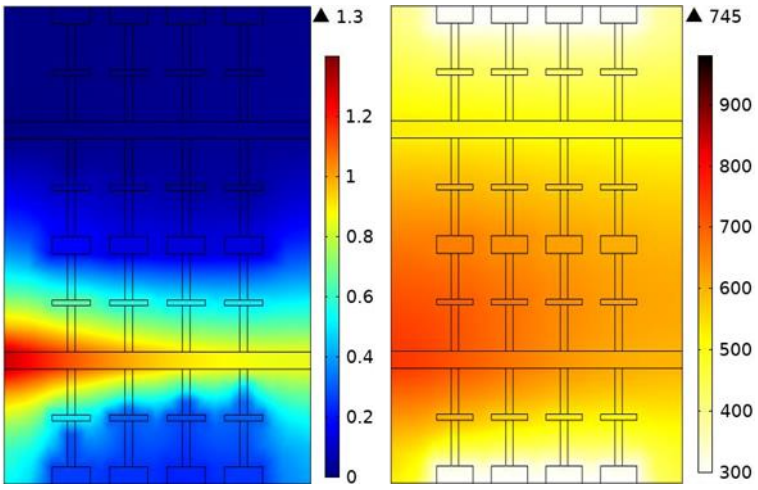


Figure IV-14 CRS architecture with Ni wires at the steady state: a) electrical potential distribution; b) temperature distribution.

The results obtained for such a structure are given in Figures IV.14, 15, and 16, for Ni, Cu, and CNT bars, respectively. Note that the active layers and the passive ones are the same as with the reverse structure.

Table IV.4 shows that for the three materials a bias level of 1.3V (for Ni), 0.8 V (for Cu and CNT) is enough to guarantee the switching level to the cells. The results of the thermal analysis are plotted in Figures IV.14b, 15b, and 16b reported in Table IV.5 provide a similar outcome as for the reverse structure, with a thermal crosstalk

problem only partially solved for the Ni case (cells in layer #3 have still unwanted RESET) and completely solved for the Cu and the CNT cases.

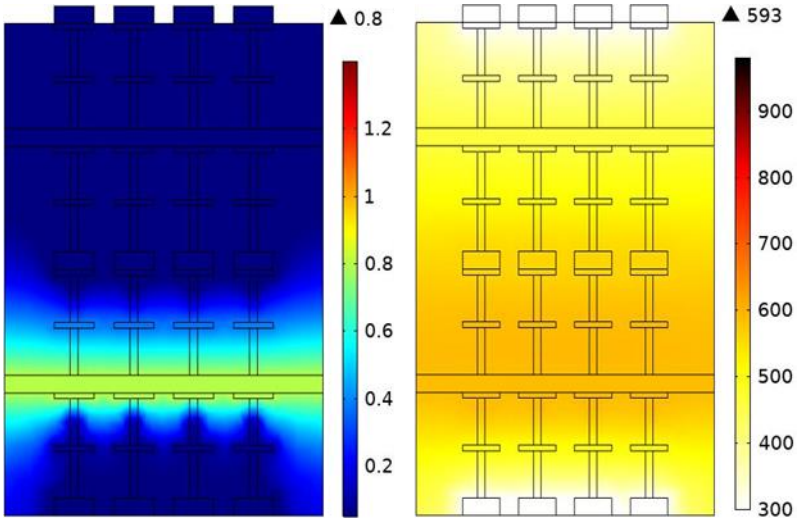


Figure IV-16 CRS architecture with Cu wires at the steady state: a) electrical potential distribution; b) temperature distribution.

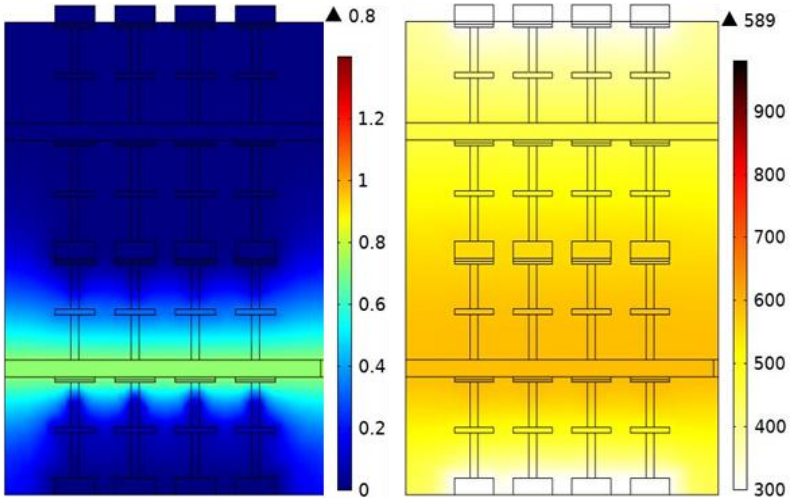


Figure IV-15 CRS architecture with CNT wires at the steady state: a) electrical potential distribution; b) temperature distribution.

From the thermal distribution seen in Figures IV.15b and 16b we note that the maximum temperature decreases compared to the conventional structure (Table IV.5), following the decrease of the applied bias. However, when compared with the

1D1R-1R1D integration (Figures IV.11,12 and 13) we took attention that this maximum is declined to a value less than the critical temperature in the two victim layers (about 430K) and then can serve to limit the effect of thermal crosstalk

problems. Furthermore, we can confirm this through the results in Table IV.5 for the maximum temperature for each layer.

Finally, it can be pointed out that the residual thermal crosstalk issue that is found in the two proposed architectures can be solved in an alternative way, without replacing the Ni bars with the Cu and CNT.

Table IV-4 Voltage levels (v) across the CF of the cells along a bar, for all the considered cases.

Structures		Conventional	Reverse	CRS
Ni	Bias	1.4V	1.2V both sides	1.3 V
	Cell1	0.80	0.73	1.02
	Cell2	0.79	0.71	0.89
	Cell3	0.76	0.71	0.81
	Cell4	0.70	0.70	0.75
Cu	Bias	0.9 V	0.9V	0.8V
	Cell1	0.75	0.72	0.79
	Cell2	0.76	0.73	0.79
	Cell3	0.76	0.73	0.79
	Cell4	0.74	0.72	0.78
CNT	Bias	1 V	1V	0.8 V
	Cell1	0.81	0.74	0.72
	Cell2	0.83	0.75	0.72
	Cell3	0.83	0.75	0.72
	Cell4	0.81	0.74	0.72

From the horizontal perspective, thermal crosstalk becomes more severe in the 1D1R-1R1D structure because it contains more active cells connecting to the same WL. For this purpose, the 1D1R-1R1D structure is polarized from a single WL in the vertical direction, but only two WLs are polarized in the horizontal direction. This means that the first and third cells are polarized and that the second and fourth cells are unpolarized (as seen in Figures IV.17,18 and 19 for the three cases of interconnections). The second victim cell is surrounded by four active cells of the two layers. Figure 13a shows the thermal distribution for the Ni wires, where the thermal crosstalk comes from the neighboring cells in the horizontal direction that can affect the victim cells.

For Cu and CNT, we notice from the thermal behavior of FiguresIV18 and 19 and the values mentioned in Table IV.6 that the effect of thermal crosstalk is decreased and the value through the victim cell is approximately 521.91K (for Cu) and 526.03K (for CNT). The temperature rise values with Cu and CNT are below the critical temperature and this confirms that the use of these wires can solve thermal integrity problems.

Table IV-5 Maximum temperature (k) of the CFs for all the considered cases.

	Layer state	Conventional Structure	Reverse Structure	CRS Structure
Ni	Bias	1.4V	1.2V both sides	1.3 V
	Layer #1	802.81	675.76	685.29
	Layer #2	972.74	757.22	737.11
	Layer #3	960.04	592.01	573.10
	Layer #4	581.00	488.30	487.91
Cu	Bias	0.9 V	0.9V	0.8V
	Layer #1	619.21	571.59	569.70
	Layer #2	729.12	626.35	591.76
	Layer #3	728.47	510.23	489.39
	Layer #4	489.48	430.00	431.63
CNT	Bias	1 V	1V	0.8V
	Layer #1	639.61	593.82	562.93
	Layer #2	771.22	657.39	588.26
	Layer #3	732.52	528.69	484.13
	Layer #4	493.41	440.24	428.06

On the other hand, the fourth victim cell is located at the last extremity of the crossbar and it is affected only on one side of neighboring cells. The values in Table V justify that the effect of thermal crosstalk is attenuated and resolved for the three cases of interconnections with respect to the critical temperature.

Indeed, the crosstalk can be mitigated by following the classical rule of widening the cell separation. Let us for instance refer to the reverse 1D1R-1R1D architecture, considering only one layer (layer #1) and assuming that only cells 1 and 3 are biased, whereas 2 and 4 are passive. In the previous cases, the horizontal distance between the cells has been assumed to be equal to 2F, being F the size of the feature cell. Table IV.6 shows the decrease of the temperature obtained in the two passive cells, by increasing the cell separation, for Ni, Cu, and CNT interconnects. A

significant decrease in thermal crosstalk is noted when the active cells are spaced away from the victim cells, so that this issue can be completely solved with a proper increase of spacing. Of course, this solution avoids the change of the bar material, but decreases the density of memory for a given volume.

Table IV-6 Maximum Temperature (K) in the two victim cells of the first layer of the 1D1R-1R1D structure for different cell spacing.

Layer #1	2nd victim cell	4th victim cell
Ni (2 F)	596.79 K	539.12 K
Ni (2.25 F)	576.37 K	530.12 K
Cu (2 F)	521.91 K	487.72 K
Cu (2.25 F)	501.78 K	473.78 K

This study demonstrates the possibility of mitigating or even solving some of the major electrothermal issues suffered by 3D stacked arrays of 1D-1R RRAMs. Two novel architectures are proposed to stack these memories, one based on a reverse arrangement (reverse) and the other one based on a complementary structure (CRS). Both of them are shown to optimize the bias management, whereas the latter one (CRS) provides the additional benefit to avoid the use of diodes. A comparative analysis has been carried out with reference to the RESET process. Compared to the

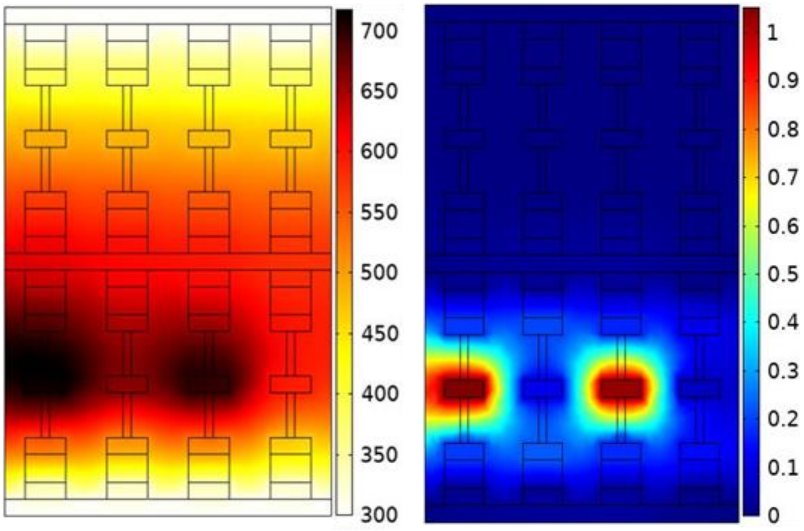


Figure IV-17 Horizontal Thermal crosstalk of the 4×4×4 1D1R-1R1D array with Ni wires at the steady state: a) temperature distribution; b) electrical potential distribution.

reference architecture, both of the novel architectures are able to drive the RESET with almost the same values of the bias voltage. This level can be strongly reduced if

the electrical interconnects of the array are realized with copper and carbon nanotubes instead of nickel. Indeed, this is a way to solve the problem of the significant voltage drop along the interconnects introduced by the high resistivity of Ni wires.

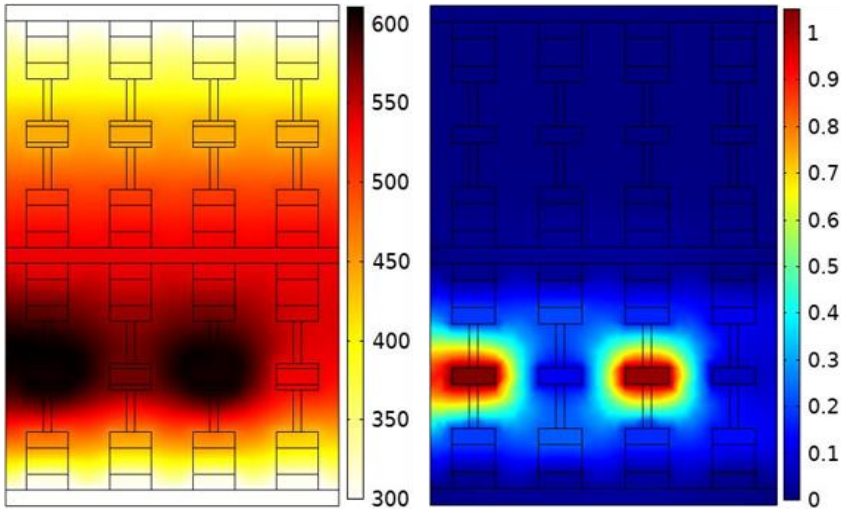


Figure IV-18 Horizontal Thermal crosstalk of the 4×4×4 1D1R-1R1D array with CNT wires at the steady state: a) temperature distribution; b) electrical potential distribution.

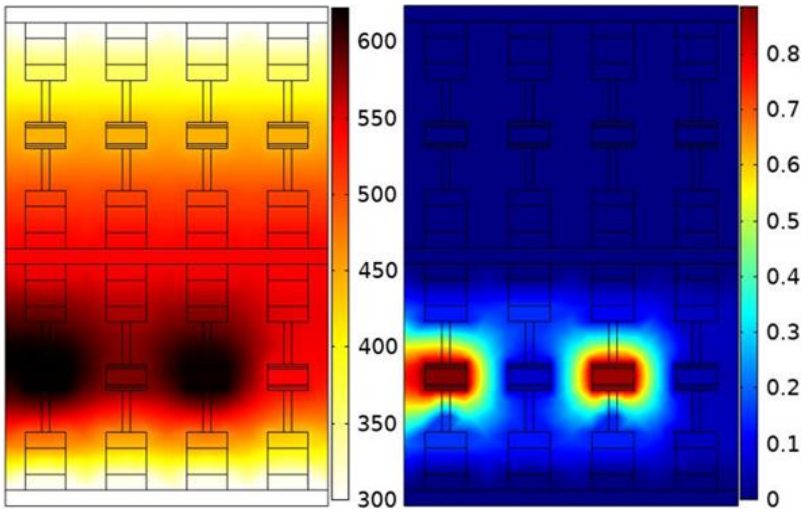


Figure IV-19 Horizontal Thermal crosstalk of the 4×4×4 1D1R-1R1D array with Cu wires at the steady state: a) temperature distribution; b) electrical potential distribution.

The new architectures are also demonstrated to strongly mitigate or even solve the problem of the unwanted RESET switching associated with the thermal crosstalk between adjacent cells. Indeed, once moving to these architectures, this problem can be solved by replacing Ni wires with Cu and CNT, or by increasing the spacing between cells.

Table IV-7 Maximum Temperature (K) of the Conducting Filaments in the first layer of the 1D1R-1R1D structure.

Layer #1	2^{nd} victim cell	4^{th} victim cell
Ni	596.79 K	539.12 K
Cu	521.91 K	487.72 K
CNT	526.03 K	491.09 K

IV.4 Conclusions

- This chapter demonstrates the possibility of mitigating or even solving the major electrothermal issues suffered by 3D stacked arrays of 1D-1R RRAMs.
- Two novel architectures are proposed to stack these memories, one based on a reverse arrangement (reverse) and the other one based on a complementary structure (CRS). Both of them are shown to optimize the bias management where the minimum bias that can be used is 0.8V, whereas the latter one (CRS) provides the additional benefit to avoid the use of diodes.
- A validation analysis has been carried out with reference to the RESET process for the conductive filament with the conventional and the improved model.
- Compared to the reference architecture, both of the novel architectures are able to drive the RESET with almost the same values of the bias voltage.
- The level of bias has been strongly reduced when the electrical interconnects of the array are realized with Cu and CNT instead of Ni

(0.9V and 0.8V) and this solves the problem of the significant voltage drop along the interconnects introduced by the high resistivity of Ni wires.

- The new architectures are also demonstrated to strongly mitigate or even solve the problem of the unwanted RESET switching associated with the thermal crosstalk between adjacent cells.
- With these architectures, the thermal crosstalk problem can be solved by replacing Ni wires with Cu and CNT, or by increasing the spacing between cells.

Chapter V : Electrothermal Analysis of a Graphene-Based Thermistor

Chapter V

Introduction

The excellent and exceptional electrothermal behavior of new graphene-based nanomaterials is one of the most fascinating properties studied in recent decades. Hence, the graphene-related materials are widely proposed in several applications where the thermal effects are presented an issue. For instance, on-chip and on-package interconnects (Morris,2018; To.Sanial,2016) thermal interface materials (Shahil,2012), heaters (Wang,2017; Smovzh,2020), and temperature sensors (Koskinen,2020). In fact, these multifunctional materials with several properties such as good electrical and thermal conductivity and low thermal inertia make it possible to provide heaters or thermal sensors with a light weigth, good processibility and rapid thermal response. The characteristics that make these materials so interesting for the above applications are the precise control of the effect of temperature on electrical parameters, such as resistivity. Indeed, Carbon-based materials can provide resistivity with a near-zero or even negative derivative relative to temperature variation, where the materials refer to the zero temperature coefficient effect (ZTC), their resistance does not change with the increase in temperature (Chu,2015). In addition, several materials used for such applications may have the effect of positive temperature coefficient (PTC) means an increase in resistance with increasing temperature while others with negative temperature coefficient (NTC) effect mean the decrease in resistance with an increase in temperature (Boom,2016; Maffucci,2017; Kumar,2019). These features offer the possibility to use these materials in applications where the pattern and weight present the main constraints, such as airborne de-icing systems based on the Joule heating effect (Karim,2018).

When it comes to the ideal, high-quality graphene-related materials, such as mono or few layers graphene sheets, single or multi-walled carbon nanotubes (CNT), where the temperature-dependent electrical resistivity is derived by validated analytical or semi-analytical models, still available in the literature (Tan,2007; Chiariello,2010; Mariani,2010). Although they are of great scientific interest, they are not very attractive for industrial applications, given their high manufacturing costs associated with the degree of control required during their manufacturing

processes and the limited yields of such processes. Instead, in the direction of industrial applications of graphene technology, the attention is rather focused on low-cost alternatives, such as nanocomposites (graphene-related composite materials). The temperature-dependent resistivity of graphene nanocomposite (Han,2019; Mohiuddin,2011), or epoxy/CNT composites have been proposed as heating elements or as temperature sensors (Neitzert,2010).

Among the latest low-cost versions of graphene, the so-called Graphene Nanoplatelets (GNPs), is composed of irregular flakes of few-layers graphene (Young,2012). These GNPs given the possibility of manufacturing by means of high-yield industrially scalable techniques such as ball-milling (Young,2012) or wet-jet milling (Castillo,2018), or microwave irradiation (Dabrowska,2014; Maffucci,2016). Indeed, GNPs present a good compromise between physical properties, large-scale production, and reasonable costs (Kovtun,2019) compared to other low-cost graphene-based materials. Thus, the electrical and thermal properties of graphene or related materials such as carbon nanotubes have recently been studied in many factory applications according to the sensitivity of their electrical properties to the external environment, such as electrochemical sensors (Kumar,2020), gas sensors (Al.Hartomy,2019), piezoresistive sensors (Luo,2013), pollution filters (Ferrigno,2019), multifunctional sensors (Huang,2019), and thermo-electric applications (Karim,2018; Prolongo,2016; Jiang,2017).

In view of these applications, the electrical, thermal and mechanical properties of the GNP-related materials have been investigated in several extensive studies. This chapter is focused on the study of the electrical resistivity of such materials, with specific emphasis on the effect of temperature. These GNPs materials are characterized by a very high weight fraction (wt%), from 70 wt% (GNPs + polymers) to 100 wt% (pure GNPs). To our knowledge, few reports are available to date to address this issue. Indeed, in almost all references cited, the GNPs fraction is much smaller, less than 5% by weight. The study given in (Jen,2019) of electrical and thermal stability is linked to a composite reinforced by hybrid fillers made by GNP and CNT at different ratios. However, the total weight of the filler is very small. On the other hand, the analysis of the hybrid GNP/CNT composite with

different GNP fractions is provided in (Huang,2019), up to 50wt%. Where in the same reference, the temperature-dependent resistivity model is performed with the detection of the NTC behavior in a large temperature range. However, in this study, the GNP is mixed with another conductive material (CNT), so it is impossible to extrapolate only the resistivity of the GNP. This analysis can be carried out in a few works as was done in (Tiran,2014). It has been shown that this material has a PTC effect and a large linear response adapted to temperature detection. A thorough study of the electrical and thermal properties given in (Wu,2012) is provided on GNP films comparable to those studied in this chapter. However, electrical conductivity is only evaluated at a fixed temperature. To this end, the chapter aims to provide and validate an analytical model identifying the temperature dependence of the electrical resistivity of the strips made by GNPs only or by composites with a very small percentage of binders and a very high concentration of GNP (> 70 % by weight).

V.1 A Graphene Nanoplatelets strip as a thermistor

The graphene strips considered in this work are industrial materials manufactured by Nanesa (Nanesa, n.d.), where the sheets are freestanding paper based on highly oriented nanoscale GNPs with a high percentage of the reinforcement phase of about 70%. The fabrication process of GNPs is summarized in Figure IV.1 and is based on the 3 main phases.

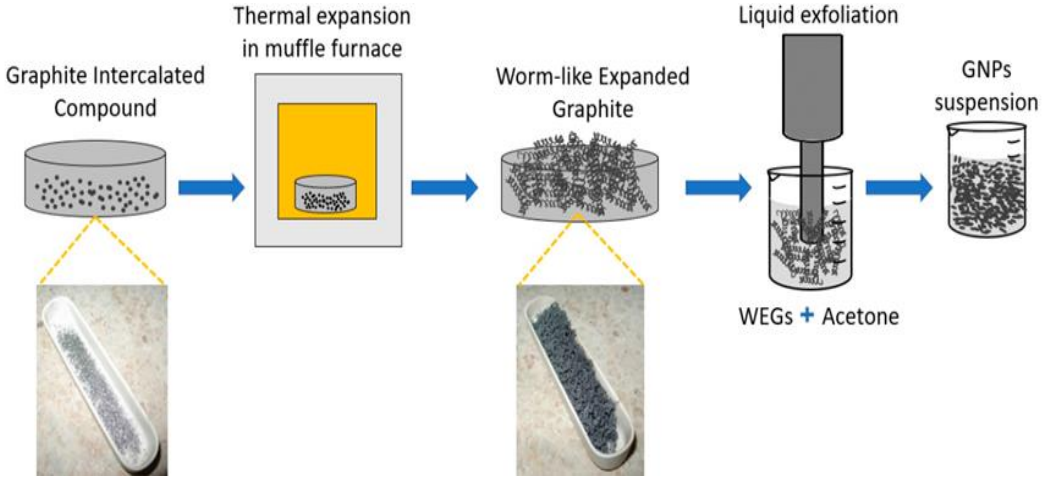


Figure V-1 Diagram of the GNP manufacturing process (Bellagamba.2020).

The first step is to prepare the sample by putting the expandable graphite flakes inside the metal melting pot. Next, the second step is represented in the thermal expansion where the graphite Graphite intercalated compounds (GIC) is placed inside a muffle furnace at 1150 °C for 5 s to perform the expansion and this treatment can increase the volume of GIC up to 200 times and form the “worm-like” expanded graphite (WEG). The last main step is the liquid exfoliation of the WEG, where these particles are dispersed in an acetone solvent and mixed with the polymer binder. Then

this mixture is sprayed at a controlled pressure by using a semiautomatic 3-axes pantograph, thus obtaining CNPs after calendering phase to attain a compact sheet and improve the thickness/alignment ratio.

Table V-1 The Graphene Strips.

Material	GNPs (%)	Binder (type)	Thickness (µm)	Width (mm)	Length (mm)
G-Paper	100	---	55	10	100
G-PREG (95/5)	95	polyurethane	75	10	100
G-PREG (80/20)	80	polyurethane	75	10	100

Figure IV.2 shows the Scanning Electron Microscope (SEM) picture of single GNP flakes, with the average thickness of about 14 nm and the average lateral dimension of about 30-40 µm. The dimensions and special shapes of these particles make them more efficient in transmitting a barrier property. on the other hand, the structure of GNP makes them excellent thermal and electrical conductors.

Following the previous fabrication steps, three types of graphene materials are considered in this chapter with different percentages of GNPs and polymeric binders. The first material consists of pure GNPs, hereafter referred to as G-Paper. The other two materials are designated as G-Preg 95/5 and G-Preg 80/20, based on the mixture between GNPs and binders at low concentration (Table IV.1). The choice of these materials is based on several characteristics: G-Paper has the best thermal and electrical properties and G-Preg is mechanically stable and has good interaction with other polymers. The dimensions of graphene strips are given in Table IV.1.

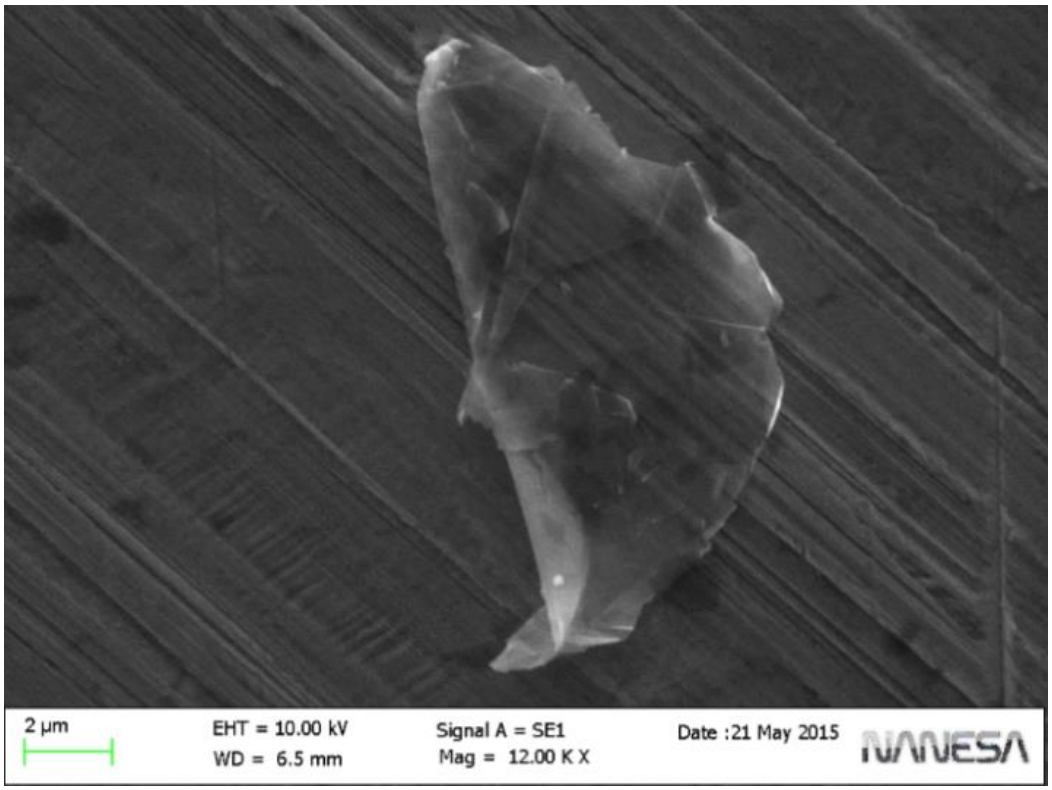


Figure V-2 Microscope pictures of GNPs: SEM image of a single graphene flake (the scale is 2 µm).

The GNP papers are cut into small strips measuring 10mm x 180mm. To this end, an appropriate test map based on FR4 has been carried out, as shown in Figure IV.3, with two amperometric electrodes and several voltmetric electrodes of different positions. The strip is placed on the printed circuit board by touching the two gold-coated copper terminal electrodes to reduce the contact resistance and is secured by a plastic frame. This later may close the strip in a sandwich structure that has been mechanically tightened with screws.

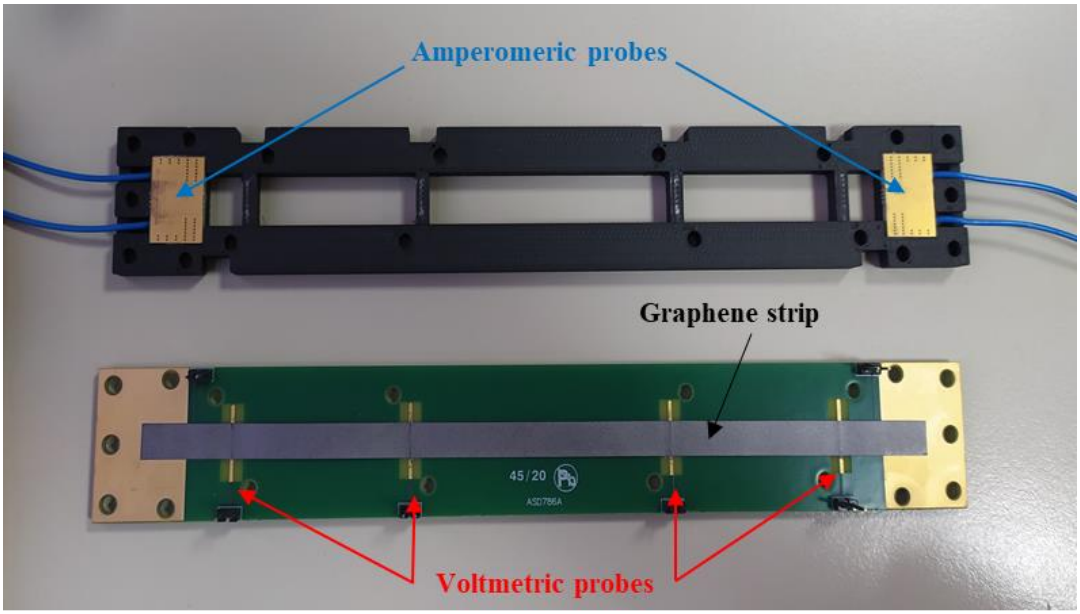


Figure V-3 Experimental characterization of the electrical resistance of the GNP strips: test-board (bottom), and fixing frame (top).

V.2 Electrothermal model of the GNP thermistor

To modulate the electrical resistivity, the experimental results of the measured resistance are compared to the results obtained from the numerical simulations. To do this, a 3D electrothermal model was developed in Comsol Multiphysics (Comsol-multiphysics,n.d.), coupling the electrical and the thermal problems. Figure IV.4, shows the equivalent model of the text board with GNP strips, where the solutions of this electrothermal model are given by coupling the Fourier heat flow equation to the Poisson electrical equation as demenstrated in chapter III.

The numerical solution of the model was augmented with proper electrical and thermal boundary conditions and implemented by means of a finite-element approach based on the use of adaptive tethraedons mesh.

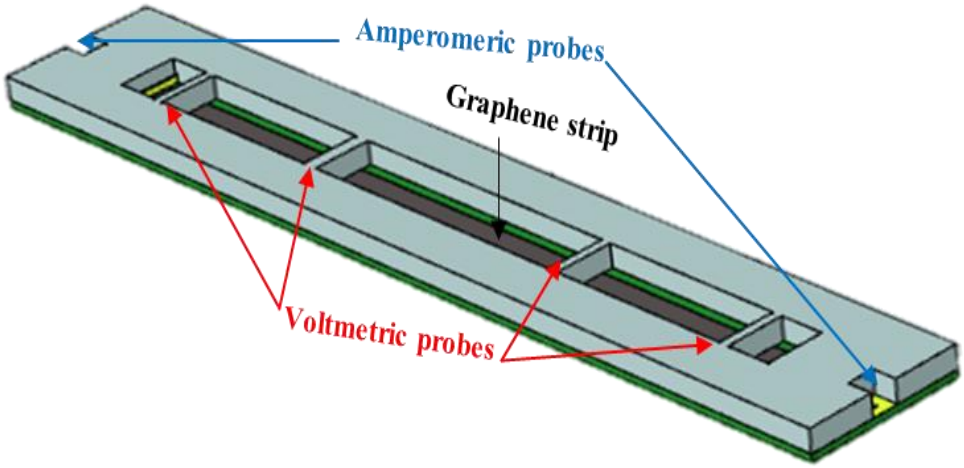


Figure V-4 The electrothermal CAD model developed in COMSOL Multiphysics.

Furthermore, homogeneous Dirichlet conditions were imposed on one electrode while a known current density was imposed on the other one.

In the following section, the equivalent homogeneous resistivity ρ_{eq}will be determinated for the whole GNP strip, which does not depend on the position vector r. However, the electrical resistivity should be modeled as a tensor, that is to say the diagonal matrix:

$$\rho(T) = \mathrm{diag}\left[\rho_{xx}(T), \rho_{yy}(T), \rho_{zz}(T)\right] \qquad \text{(V.7)}$$

Considering the in-plane isotropic of the material, with the in-plane components are almost equal ($\rho_{xx} = \rho_{yy} = \rho_{||}$), but with the perpedicular component ρ_{zz} is usually at least one order of magnitude lower (Ferrigno,2019). Instead, in our case the vertical component current imposed on the electrodes is negligible, thus the tensor (IV.7) can be replaced by the scalar function $\rho_{eq}(T) = \rho_{||}(T)$ without introducing significant errors.

Finally, the isotropic of the in-plane resistivity was verified by measuring the resistance of the G paper strips at room temperature: the values of the two orthogonal directions for the current were less than 1%.

V.3 Experimental characterization of the GNP thermistor

V.3.1 Set-up assessment and preliminary characterization

The measurements of the electrical resistance of the GNP strips is obtained through :

$$R_m = \frac{V_v}{I_a} \qquad \text{(IV.8)}$$

Where , V_v, is the measured voltage across the voltmetric electrodes corresponding to the current imposed on the amperometric electrodes I_a as shown in Figure IV.3.

These preliminary measurements are made at room temperature with two 6 ½ digit multimeters: Agilent 34401A (for current) and Keithley 2700 (for voltage), with the current source, is the QJE QJ-3005 DC power supply, further for AC tests, the test board is attached to an impedance meter, GWINSTEK LCR-8110G. Thus, to remove contributions from the setup (connectors and cables) and the contact resistance of the electrodes, proper calibration is required and this is why the two voltmetric electrodes are used in different positions. After the electrothermal behavior was carried out by placing the test boards with strips in the climate chamber ACS DY110 (Figure IV.5) and the electrical resistance was measured with a wide temperature range [-40, +60] °C. To do this the first step is to stabilize the chamber at the specific temperature value so that its distribution on the test device is uniform in a satisfactory manner, and the next step is the resistance measurement.

In the DC state with the use of the 4-probe technique, the measured resistance (IV.8) may be presented by two terms associated with the contact resistance between the graphene band and the copper electrodes and also taking into account the resulting contact resistance at the interface between the bands and the voltmetric electrodes. To do this, the expression of R_m is modeled as the resistance of the graphene interconnect (To. Sanial,2016; Maffucci,2017):

$$R_m(T) = R_C(T) + r(T)L_v \qquad \text{(V.9)}$$

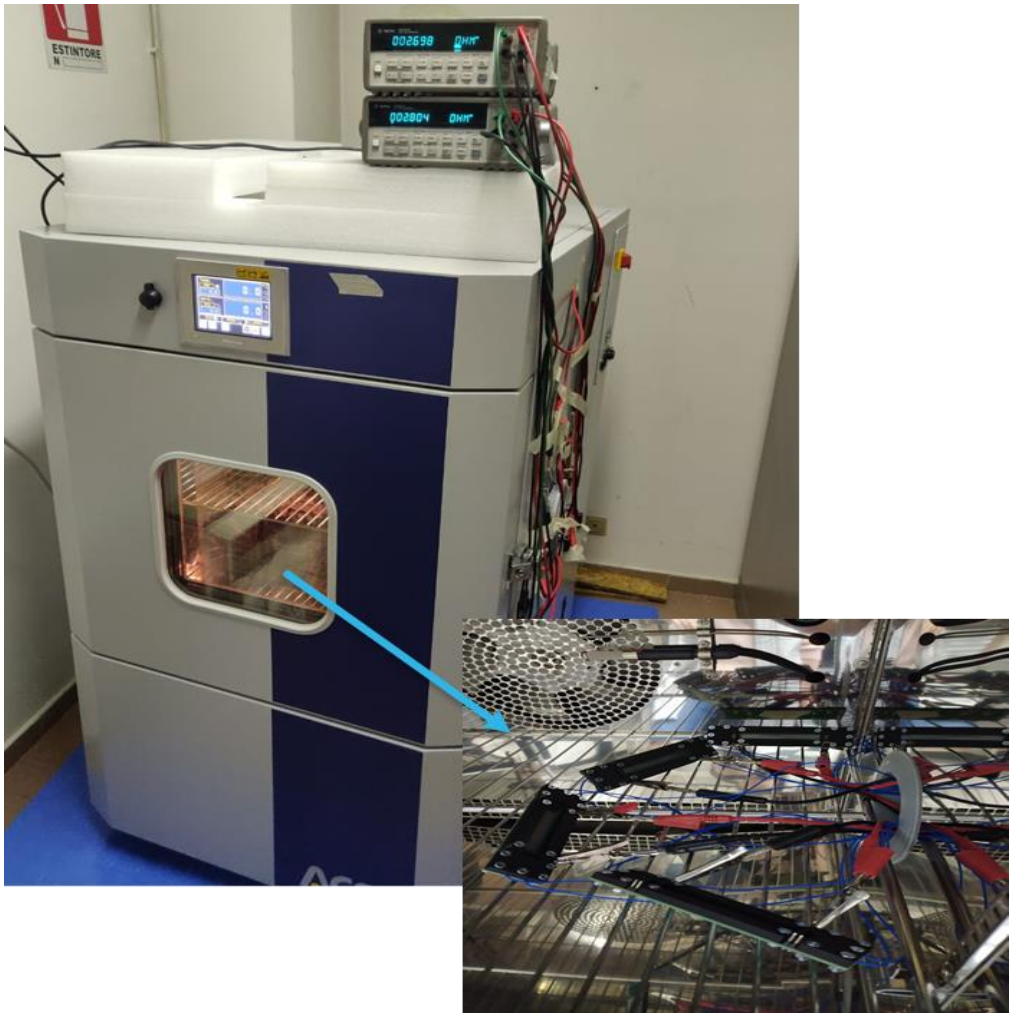


Figure V-5 The climatic chamber (ACS DY110) hosting the test-board and the strips with the external measurement circuit.

Here r presents the resistance per unit length of the graphene strip and is also called intrinsic resistance, L_v is the distance between two pairs of voltmetric probes and the R_C is the contact resistance. R_C represents the equivalent term of the local voltage drop

taken into account due to the mismatch between the strips of different materials (Wilhite,2014). Thus, for the nanoscale interconnects, R_C may has a high value to become the principal contribution to the resistance. In fact, also in the ideal case of the perfect contacts, R_C resistance has a minimum value of about 6.45 kΩ per conducting channel (To.Sanial,2016). Nevertheless, given the dimensions of the bands considered in these measurements, the contact resistance is expected to be

negligible, due to the large number of conductive parallel channels associated with graphene interconnect of such widths. In order to verify this assumption, different experimental R_m values were mesured at room temperature by changing the voltmetric probes over four different distances L_v: 40, 60, 100, and 140 mm (Figure IV.6) of the the graphene strip (G-preg 95/5) and this made it possible to measure 4 different values of voltage and R_C can be estimated by the measuring R_m since it does not depend on the L_v.

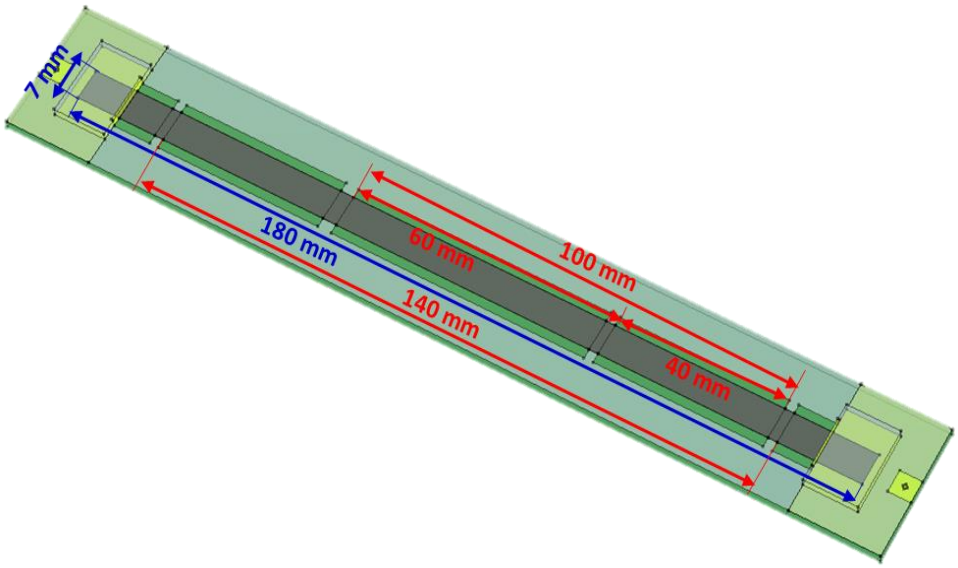


Figure V-6 The CAD model based on G-Preg (95/5) strip with different voltmetric probes.

For this experiment, we consider at each measuring position the same contact materials and the same applied contact pressure as well as for surface finishing and the geometry of the contact materials is almost the same, so at a given temperature, (IV.9) may be expressed as follows:

$$R_m = \frac{\rho_m}{S} \cdot L_v + R_c \qquad \text{(V.10)}$$

By applying the Generalised Least Squares algorithm (Carotenuto,2005), we can estimate the values of ρ_m/S and R_C, as shown in Table IV.2, for each length, we have the corresponding mesured values R_m. As previously expected, the value of R_C which is in the order of a few mΩ could be negligible compared the total value of R_m, which is of the order of Ω.

Table V-2 Estimated values at room temperature of the contact resistance term in Rm (9).

Measured data		Estimated values	
L(m)	R_m (Ω)	ρ_m/S (Ω/m)	R_c (Ω)
$4.0 \cdot 10^{-2}$	1.524	38.26	$12.11 \cdot 10^{-3}$
$6.0 \cdot 10^{-2}$	2.309		
$1.0 \cdot 10^{-1}$	3.830		
$1.4 \cdot 10^{-1}$	5.370		

Based on the above considerations, the preliminary characterization was performed by changing the position of the Lv, voltmetric electrodes as shown in Table IV.2. The resulting values of the Rm measure allowed us to estimate the contact resistance as RC =12 mΩ, so it will be negligible. For these tests, the values of the current used to characterize the bands and measure the resistance are of the order of 10 mA. Instead, the linear characteristic V-I was checked in the range of [0-1] A, in order to achieve the current levels necessary to provide a joule heating effect to the experimental tests. Figure IV.7 shows the V-I response for the three graphene materials at room temperature.

The first experiment was based on the G-Preg band (95/5) with a dimension of width and length of 7x180mm respectively (Figure IV.6). The results mentioned in Table IV.3 are derived by implementing the electrical resistivity corresponding to the measured resistance in the numerical model, then the numerical resistance for each voltmetric probes is resulting from the simulation. It should be noted that the electrical resistivity values are almost the same for different experimental resistances so that the electrical resistivity model is stable for different probe positions since it is independent of the length of the strip.

The maximum relative error when comparing the experimental resistance and the numerical one is about 2.093% for the strip length 40 mm and the minimum error is about 0.8% for 100 mm as mentioned in the Table IV.3.

The same results are obtained within the second test for the same GNP strip (G-Preg 95/5) but with different strip's width and length (11x180 mm). For this analysis the electrical resistivity values are increased compared to the first test and this increase is

following the decrease of the experimental resistance since the width strip is higher than the one in the first test.

Furthermore, the stability of the model is still exist as showed in Table IV.4. As mentioned for the first test, almost the same percentages in change of the relative error were obtained due to the stability of our model. Ultimately, the main purpose of using different probe positions is to be able to estimate the contact resistance, as it does not depend on the length of the strip.

Table V-3 Numerical resistance against experimental resistance for different voltmetric positions for 7x180 mm G-Preg size.

TECHNIQUE (7x180 mm)	L [mm]	R[Ω] Experimental	ρ [Ωm]	R [Ω] Numerical	Relative Error %
4 Probes	140	4.986	$18.70 \cdot 10^{-6}$	4.930	1.123
4 Probes	100	3.553	$18.65 \cdot 10^{-6}$	3.525	0.774
4 Probes	60	2.167	$18.96 \cdot 10^{-6}$	2.132	1.592
4 Probes	40	1.381	$18.12 \cdot 10^{-6}$	1.352	2.093

Table V-4 Numerical resistance against experimental resistance for different voltmetric positions for 11x180 mm G-Preg size.

TECHNIQUE (11x180 mm)	L [mm]	R [Ω] Experimental	ρ [Ωm]	R [Ω] Numerical	Relative Error %
4 Probes	140	3.3633	$19.82 \cdot 10^{-6}$	3.325	1.139
4 Probes	100	2.3902	$19.72 \cdot 10^{-6}$	2.372	0.761
4 Probes	60	1.4376	$19.77 \cdot 10^{-6}$	1.415	1.572
4 Probes	40	0.9581	$19.76 \cdot 10^{-6}$	0.938	2.098

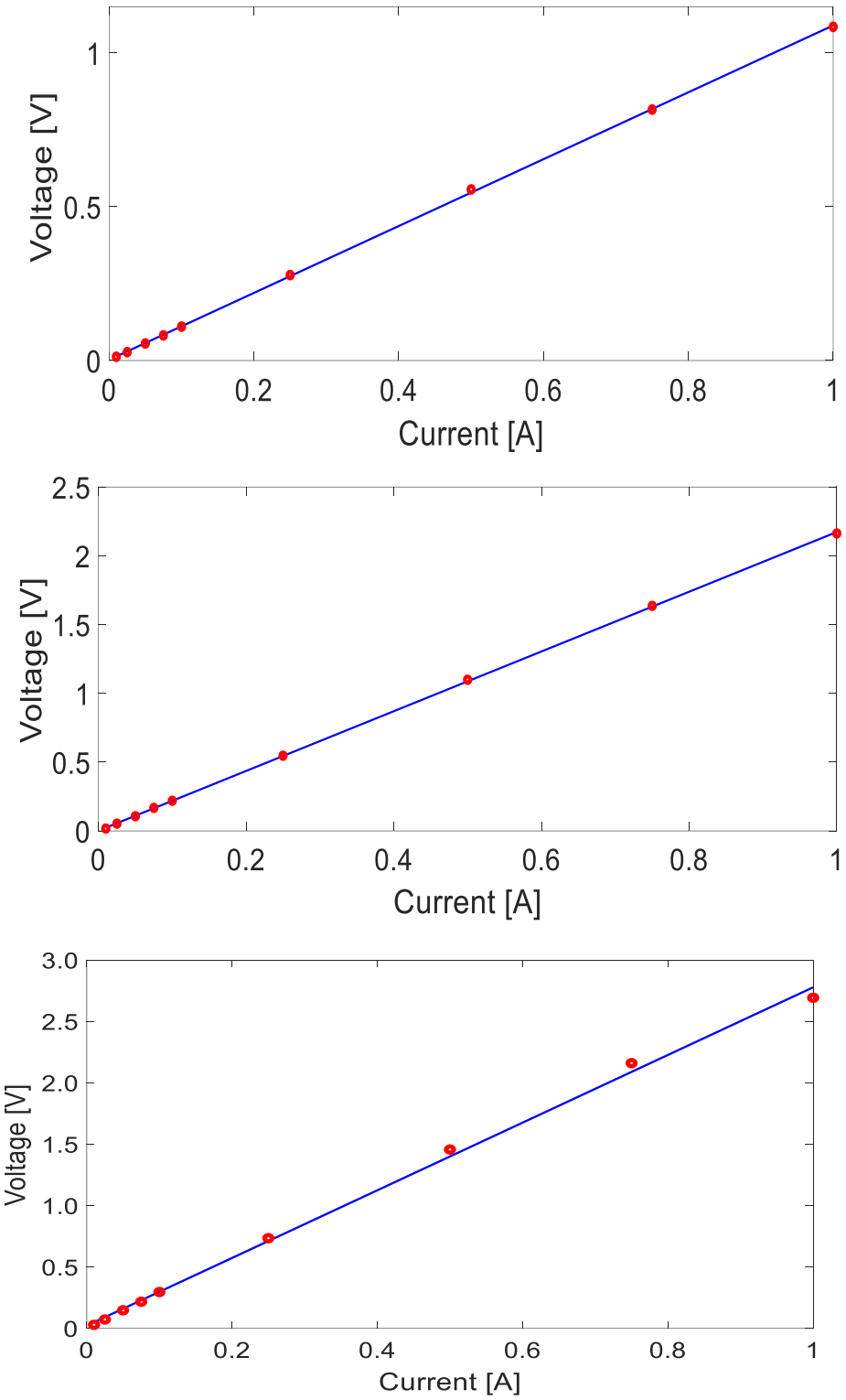


Figure V-7 Linear V-I characteristic at room temperature, for: (a) G-paper; (b) G-Preg 95/5; (c) G-Preg 80/20. Red dots: experimental data. Blue line: linear interpolation.

The numerical simulations were carried out for 3D CAD model analyses with COMSOL software, by an adaptive tetrahedral mesh. Several sizes of mesh elements are simulated and taken into account as shown in Table IV.5 in order to reach the stability of the model and to ensure the good convergence during the simulation. The purpose of the mesh sensitivity study is to determine a compromise between the accuracy of the results and the computation time of the simulation, so that to obtain recommendations on the optimal mesh. Table IV.5 shows that the numerical resistance increases with respect to the increase of the number of the element (from the Fine to Finer mesh) and the then reaches a value of stability. For the Fine mesh with 82030 domain elements, the numerical resistance is not so consisting with experimental one, where the difference is about 10%. With the increase of the number the element in Finer mesh (176412 domain elements), the error between the numerical and measurement resistance decreases of about 9.6% to 0.718% for the case of 100mm and then good agreement is achieved. That clearly proves that convergence is indeed reached and that the finer mesh is the most adequate for this computation, that allowed to estimate the numerical uncertainty introduced by this mesh to be in the order of 0.03%.

Table V-5 Numerical resistance against experimental resistance for different voltmetric positions for 7x180 mm G-Preg size with mesh estimation.

TECHNIQUE	L [mm]	R [Ω] Experimental	ρ[Ωm]	R [Ω] Numerical (Fine mesh)	R [Ω] Numerical (Finer mesh)	R [Ω] Numerical (Extra Finer mesh)
4 Probes	140	4.986	$18.70.10^{-6}$	4.492	4.930	4.932
4 Probes	100	3.5525	$18.65 \cdot 10^{-6}$	3.212	3.525	3.527
4 Probes	60	2.1665	$18.96 \cdot 10^{-6}$	1.943	2.132	2.133
4 Probes	40	1.3809	$18.12 \cdot 10^{-6}$	1.232	1.352	1.355

V.3.2 Electrothermal characterization and parameter estimation

The electrothermal characterization of the GNP strips of the three materials is performed by placing the test boards inside the climatic chamber (Figure IV.5) and cycling the temperature in the range [-40,60] °C, then measuring the electrical resistance for each sample with a current value is about 1 mA. In our experiment, steady-state results were recorded at temperatures of 20°C and the dimensions of the strips considered are 10x100 mm of width and length respectively. After the climate chamber was stabilized, resistance was measured at each temperature value for all GNP bands, as shown in Figure IV.8. These results show the typical negative temperature coefficient (NTC) characteristic of resistance for each material, where resistance values decrease with temperature. Furthermore, in this temperature cycle the responses are almost linear, and it is noted that the resistance value increases in relation to the increase in the percentage of binder in the bands. Figure IV.8 shows the cycle with the increasing temperatures and the cycle for the decreasing temperatures for all materials.

The way to obtain a negative temperature coefficient of the resistance with graphene-bound materials has been already discussed, for example in graphene-polymer composites (Zhao,2017), in graphene oxide (Morris,2018), instance in hybrid GNP/CNT composites (Huang,2019), and in carbon-nanotube interconnects (To.Sanial,2016). More recently, in (Kumar,2019), the same behavior was considered for graphene papers similar to those used in our experiment, treating with graphene resistor deposited on a paper support, using graphene ink and a bar coating film.

To explain the NTC behavior, there are two physical mechanisms. The first is based on the electrical conduction along the single graphene straw: the conduction in the interconnection based on graphene is modulated by the effective number of conductive channels, M, which depends on the size, temperature and chirality (To. Sanial,2016; Forestiere,2010).

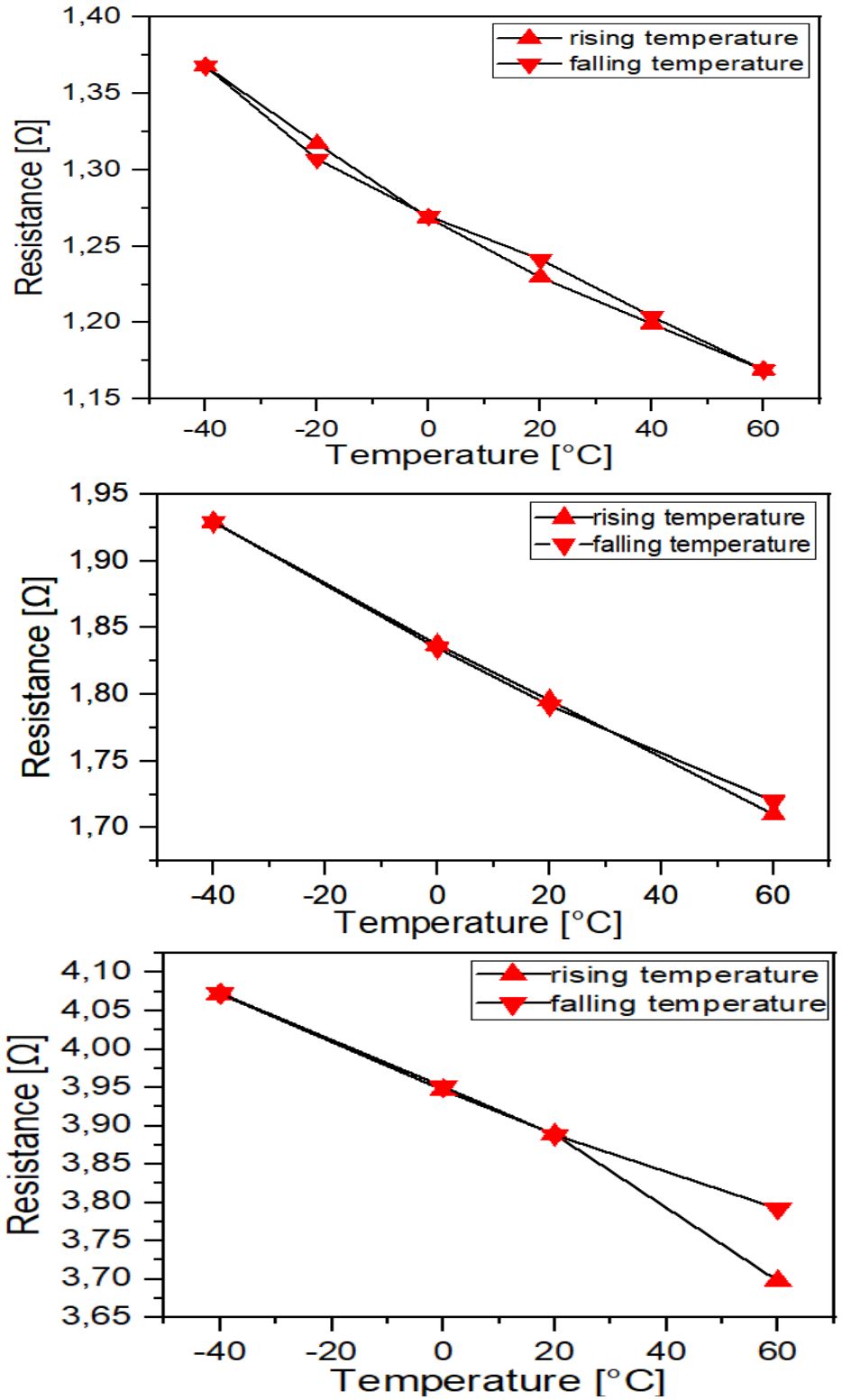


Figure V-8 Measured DC resistance when the temperature is cycling between -40 and +60 °C, for: (a) G-paper; (b) G-Preg (95/5); (c) G-Preg (80/20). The curves indicated the cycle with the increasing temperatures and the cycle for the decreasing temperatures.

(a)

For the carbon nanotubes (Forestiere,2011), the function M(T) is increase with respect to the temperature *T* as well as for graphene ribbons in (Maffucci,2013). For these nanocarbon lines, the distributed term in (IV.9) can be formulated as follows (Tiran,2014; Maffucci,2017):

$$r(T) = \frac{r_0}{l_{mfp}(T)M(T)}, \qquad \text{(V.11)}$$

Here, r_0 is a constant value, and l_{mfp} is the mean free path, that is a decreasing function of T. Practically, the possibility of obtaining a negative derivative of $r(T)$ in relation to T comes from the counteracting actions of M and l_{mfp}.

The second mechanism is based on the conduction between two neighbouring GNPs. In fact, the graphene strips used in our expriment are made by pressed GNPs flakes and not by pure graphene sheets. Then, the electron transport pattern at the interfaces between two adjacent flakes implies hopping and tunneling effects. The NTC behavior can be justified within the theory of the Variable Range Hopping (VRH) as shown in (Zhao,2017), where the considered case-studies provides a resistivity that decreases with temperature, being proportional to $1/T^{1/4}$.

V.4 Modelling the equivalent electrical resistivity

The measured electrical resistance values are given the following series of Tables IV 6-8, for all the materials during the temperature cycle [-40,60] after the stabilization of the climatic chamber, since the heat in this case is produced by the chamber whereas, in the first experiment, the heat is generated by the joule effect due to the high current value of about 1A.

The numerical resistance made by Comsol multiphysics based on the numerical model, with the use of the adapted finer mesh are also given in the same tables IV6-8. These results are comparing with the experimental results for the strips of 10x100 mm of dimensions, in order to get a good rapport between the measurement and the numerical model. For the G-paper, the relative error between the experimental resistance and the numerical one is about 1.9% during all the temperature cycle. However, for the G-preg (95/5) and G-preg (80/20), the relative error is in the

average of 0.6% of difference, thus an excellent agreement between the experimental and the numerical resistance was obtained.

Table V-6 Average values of the numerical resistance against experimental resistance during the temperature cycle [-40; +60°C] for 10x100 mm G-Paper size.

T °C	R_G-Paper [Ω] Mesurment	ρ_G-Paper [Ωm]	R_G-Paper [Ω] Numerical	Relative Error %
-40	1.3677	$8.6753.10^{-6}$	1.3406	1.981
-20	1.3120	$8.3215.10^{-6}$	1.2859	1.989
0	1.2690	$8.0493.10^{-6}$	1.2438	1.986
20	1.2355	$7.8367.10^{-6}$	1.2110	1.983
40	1.2015	$7.6212.10^{-6}$	1.1776	1.989
60	1.1691	$7.4154.10^{-6}$	1.1459	1.984

Table V-7 Average values of the numerical resistance against experimental resistance during the temperature cycle [-40; +60°C] for 10x100 mm G-Preg 95/5 size.

T °C	R_80/20 [Ω] Mesurment	ρ_80/20 [Ωm]	R_80/20 [Ω] Numerical	Relative Error %
-40	4.0728	$4.3637.10^{-5}$	4.0459	0.66
0	3.9486	$4.2306.10^{-5}$	3.9224	0.664
20	3.8884	$4.1661.10^{-5}$	3.8627	0.661
60	3.7446	$4.0121.10^{-5}$	3.7199	0.66

The measured values of the electrical resistance obtained from our experimental results were used together with those provided by Comsol multiphysics simulations based on a numerical model, to determine an equivalent resistivity for each graphene

material, in analytical form and able to take the temperature dependence into account.

Table V-8 Average values of the numerical resistance against experimental resistance during the temperature cycle [-40; +60°C] for 10x100 mm G-Preg 80/20 size.

T °C	R_95/5 [Ω] Experimental	ρ_95/5 [Ωm]	R_95/5 [Ω] Numerical	Relative Error %
-40	1.9294	$2.0672.10^{-5}$	1.9166	0.663
0	1.8361	$1.9673.10^{-5}$	1.8240	0.659
20	1.7937	$1.9218.10^{-5}$	1.7818	0.663
60	1.7119	$1.8342.10^{-5}$	1.7006	0.66

Indeed, the mean value of the measured resistance is taken for each temperature value T_i of the considered range and indicated in the following as $R_m(T_i)$. Then, the numerical model is used to estimate the simulated values of the electrical resistance at the same temperature, $R_s(T_i)$. As mentioned earlier in the numerical model that the graphene strip is described by a conductor and has a homogeneous equivalent resistivity, $\rho_{eq}(T_{i,k})$. The value of $\rho_{eq}(T_i)$ is defined by taking as the one that minimizes the Mean Square Error (MSE) between R_m and R_s, mentioned as :

$$MSE(\rho_{eq,n}) = \sqrt{\sum_{k=1}^{n} \left(R_m(T_i) - R_s(\rho_{eq,k}, T_i)\right)^2} \qquad \text{(V.12)}$$

Here *n* presents the number of samples dedicated for the numerical simulation. For instance, Figure IV.9 shows this procedure for the G-paper at *T*=20°C. Thus, after getting the equivalent homogeneous resistivity ρ_{eq}, we can compare the simulated resistance, R_s, derived by implemented this value in the full numerical model, to the analytical approximation, $R_{s,a}$, derived by considering the graphene strip as an ohmic conductor:

$$R_{s,a} = \frac{\rho_{eq}}{S} \cdot L_v \qquad \text{(IV.13)}$$

The maximum relative error between these two estimations was found to be below 0.6%.

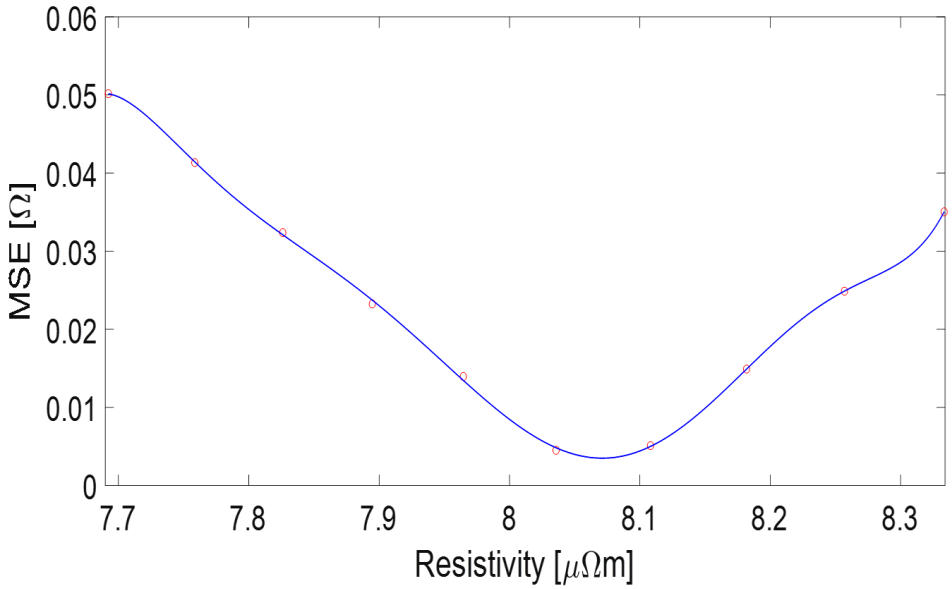


Figure V-9 The equivalent resistivity model corresponds to the minimum Mean Square Error function (IV.12) for G-paper at 20°C.

Thus, the analytical model of resistivity is approached by means of the same linear law usually adopted to define the behavior of conventional conductors such as copper (Chiariello,2010; Steinhögl,2005):

$$\rho_{eq}(T) = \rho_0(1 + \alpha(T - T_0)) \qquad \text{(V.14)}$$

Where T_0 is the reference temperature, $\rho_0 = \rho_{eq}(T = T_0)$ and α is the resistance coefficient and defined as Temperature Coefficient of the Resistance (TCR) computed at T_0, since it is:

$$\mathrm{TCR}(T_0) = \frac{1}{R}\frac{dR}{dT}\bigg|_{T=T_0} = \alpha \qquad \text{(V.15)}$$

and this assumed the relation between the resistivity and the resistance as mentioned in (V.13).

The model coefficients used for the case studied GNP materials and for the copper are listed in Table IV.9, where the equivalent resistivity values obtained conform to the values adopted in literature for similar materials and with the room temperature electrical conductivity of GNP papers at percentage. In addition, the values obtained for the equivalent resistivity ρ_0 is in the range from 12.5 to 40 μΩm, and in the same order as the values given in Table V.9.

Table V-9 Fitting parameters at T0= 20 °C, for the linear model of the resistivity in (IV.11), for the GNP Strips and Copper.

Material	ρ_0(μΩm)	α (1/°C)
Cu	$1.68.10^{-2}$	$3.90.10^{-3}$
G-paper	7.86	$-1.55{\cdot}10^{-3}$
G-Preg (95/5)	19.32	$-1.31.10^{-3}$
G-Preg (80/20)	41.57	$-0.837.10^{-3}$

Figure V.10 shows the results for all the GNP materials analyzed in this work, where the linear dependence with the temperature is illustrated with a negative coefficient of the resistance, and the experimental values are mentioned as red dots.

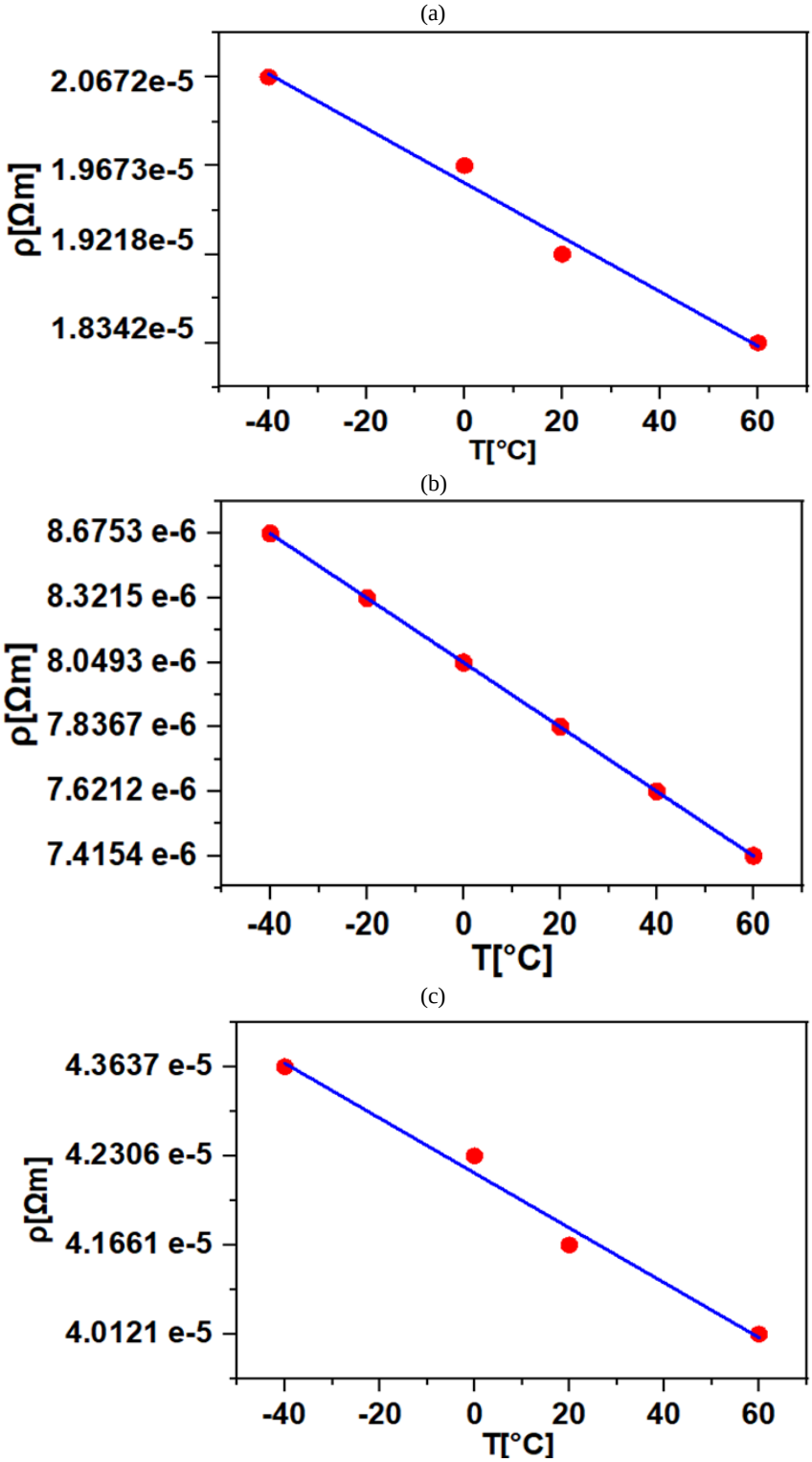


Figure V-10 Equivalent resistivity vs temperature of the three graphene materials: (a) G-paper; (b) G-Preg (95/5); (c) G-Preg (80/20). Experimental values (red dots) and simulated ones (blue line).

V.5 Validation of the thermistor model: GNP strip as heating element

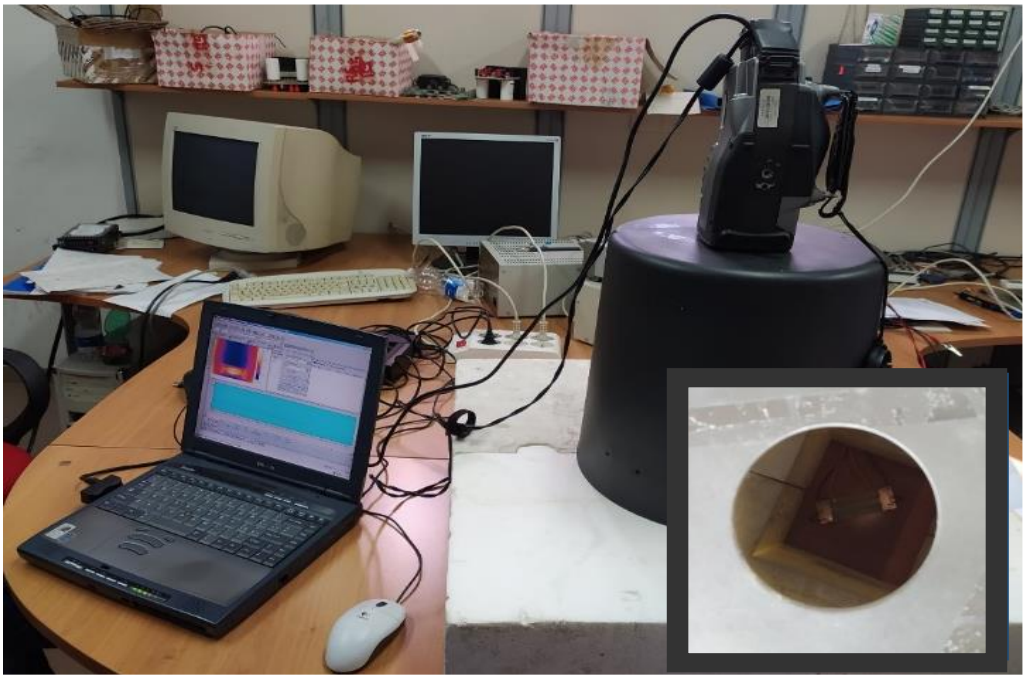
In the previous section, the simulations results were compared with the experimental ones to provide the analytical model of the equivalent homogeneous resistivity $\rho_{eq}(T)$. In order to validate these results, such a resistivity model was used in (IV.4) to predict the behavior of the graphene strips when working as heating elements, by the Joule effect.

To do this, the test-board reported in Figure IV.2 was put into a hollow box made of polystyrene and by a blackened aluminum cylinder, to guarantee thermal insulation from the environment. A thermal (IR) camera was placed on the top of the box with three thermocouples were used to measure the temperature distributions. Therma-CAM S40 was used, with an image resolution of 320x240 pixels, sensitivity 0.08 °C, and a maximum acquisition frame rate of 50 Hz as showed in Figure V.11(a). A high current value was imposed for this experiment, enough to derive a significant Joule effect, able to increase the maximum temperature along the strip of at least 10°C with respect to the environmental temperature. This current is made by the power supply QJE QJ-3005A and the multimeters Agilent 34401A and Keithley 2700 were used to check the imposed value of the current and to measure the resulting voltage.

For the G-paper, the current value required to provide this result was equal to or greater than 0.7A. Thus, the resistivity model is still valid since this current value falls within the range of linearity of the V-I response (see Figure V.7).

Figure V.11(b) shows the temperature distribution of paper, measured by the thermo-camera when the steady-state is reached. Indeed, the highest temperature is at the center of the strip and this is reasonable given the large dimensions of the terminal copper electrodes, which act as cooling fins.

(a)



(b)

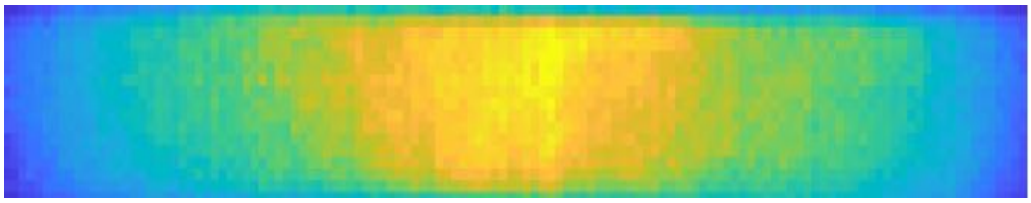


Figure V-11 Setup for the Joule heating characterization: (a) picture of the setup with side view and (inset) top view. Equipment used here: Therma-CAM S40. (b) Distribution inside the hollow polystyrene cylinder of the steady-state temperature, when using a G-paper

The profiles of the measured temperature along the graphene strip are analyzed here for different time-instants, where the initial time is at which the current has been imposed. Figure V.12 shows the steady-state result obtained after 1h (blue line), and compares it with that obtained by means of the numerical model (red line). The resistivity of the G-paper is modelled now by the linear model (V.13) based on the parameters mentioned in Table IV.6. From these profiles, a good agreement is found along the strip, with a slight deviation at the ends, this due to the local thermomechanical effects of the copper electrodes since they are not taken into account in the numerical model.

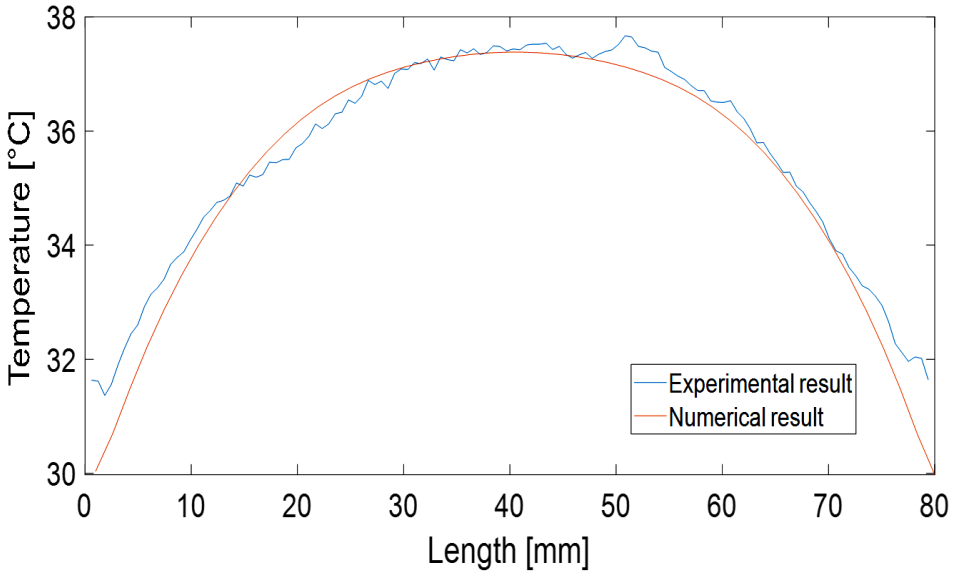


Figure V-12 Spatial distribution of the temperature along the axis of the graphene strip (G-paper), for a current of 0.7A steady state condition reached after 3600 s (1 hour): measured vs simulated solutions.

V.6 Conclusions

- In this chapter, the analytical model describing the temperature-dependent electrical resistivity of thin strips made by graphene nanoplatelets, either pure or mixed with dielectric binders has been derived.
- The model has been obtained by employing the results of the full 3D numerical simulation performed by Comsol software and of the electrothermal experimental characterization.
- The analysis is based on macroscopic strips (widths and lengths of the order of cm) made by graphene nanoplatelets, eventually reinforced by a small percentage of binders.
- At the room temperature, the electrical resistivity was found to fall in the range [7.86, 41.57] μΩm, with the coefficient of temperature that was comprised in the range [-1.55, -0.837] ·10-3 (1/°C) depends on the graphene materials.

- In a very wide temperature range, [-40, +60] °C, an equivalent resistivity has been identified, which follows the same linear law generally adopted for conventional materials, but with a negative temperature coefficient.
- The resistivity model was validated by another experiment where the same graphene bands were considered as heating elements (Thermistor) by exploiting the Joule effect: the estimated heat production using the identified equivalent resistivity led to a temperature distribution confirmed by the experimental results.
- The exceptional stability of the performance of these bands analyzed here suggests their use in electrothermal applications such as sensors or thermal resistors.

CONCLUSIONS

In this thesis, two electrothermal applications have been carried out, the first being a RRAM based on memristive devices, and the second a thermistor based on graphene strips.

As for the first application, a signal and thermal integrity analysis in 3D 1D-1RRAM crossbar have been conducted with the investigation of the use of Nickel, Copper, and Carbon Nanotubes (CNT) as word and bit lines, in a single layer and in the 3D monolithic integration. The electrothermal model of the conductive filament has been first validated against available experimental and simulation results, and then it has been improved with the use of a new function that allowed the smooth transition between the low and the high conductive states.

Simulation results of the 3D monolithic integration show that the IR drop along the Ni metal interconnects caused by the leakage current can lead to an insufficient voltage required for a successful RESET operation of the memories. Then the increase of voltage leads to the permanent breakdown stuck of near cells and increases both the joule power and RRAM operating temperature, due to high voltage stress. To face this issue, new architectures (1D1R-1R1D and CRS) have been proposed, as well as new materials have been investigated, such as Copper and CNT. Such solutions have been demonstrated to provide significantly improved performance in terms of signal and thermal integrity and shows a reduced temperature rise.

As for the thermistor application, three macroscopic strips are analyzed with different percentages of graphene nanoplates and polymers, in order to provide the equivalent electrical resistivity as a function of the temperature. An analytical model of the temperature-dependent resistivity has been carried out, based on the results of an electrothermal experimental characterization and of a 3D numerical simulation. A negative derivative of the resistivity versus temperature has been observed, in a wide range ([-40, +60 °C]). The model of the electrical resistivity has been validated by

another experiment, where these graphene strips have been successfully demonstrated their capability of acting as heating elements.

In terms of prospects, future work should cover the following topics:

On the basis of this thesis work, it is possible to propose some ways of improvement in the realization of future memory devices and heaters elements.

- A better understanding of the physics of RRAM to benefit as much as possible from the electrical properties of RRAM for both memory applications and neuromorphic hearts.
- Identification of synaptic matrix models associated with an appropriate learning circuitry to allow a more efficient and adapted hardware implementation, as well as online and real-time learning.
- To increase the efficiency of CRS devices it is suggested to work on optimizing the electroforming step, which might require less development at first. A lower electroforming voltage value could be combined with a longer application time. At the same time, we could work on developing training-free devices or CS devices.
- In addition, if RRAM memories were to be embedded in future nomadic systems, the memory cells would certainly rest a low-thickness high-k oxide (e.g. hafnium oxide HfO_2), exhibiting bipolar behaviour, integrated in a 1D/1R architecture and allowing multi-bit storage using control methods based on $I_{forming/set}$ and I_{reset} current control.
- For the thermistor based on graphene strips, future works will be devoted to complete the analysis of the parameters by estimating also the thermal conductivity, and carrying on a systematic study of the characteristics of the thermal response of the heating elements.
- In addition, work can be done to assess the mechanical performance of the strips studied in this thesis, when considering them in a realistic assembly.

LIST OF PUBLICATIONS

Journal Publications:

[P.1] Lahbacha, K., Zayer, F., Belgacem, H., Dghais, W. and Maffucci, A., (2021). "Performance Enhancement of Large Crossbar Resistive Memories with Complementary and 1D1R-1R1D RRAM Structures," in IEEE Open Journal of Nanotechnology, 2, pp.111-119. DOI : 10.1109/OJNANO.2021.3124846.

[P.2] Lahbacha, K., Sibilia, S., Trezza, G., Giovinco, G., Bertocchi, F., Chiodini, S., ... & Maffucci, A. (2022). Electro-Thermal Parameters of Graphene Nano-Platelets Films for De-Icing Applications. Aerospace, 9(2), 107. DOI.org/10.3390/aerospace9020107.

[P.3] Fakhreddine, Z., Lahbacha, K., Melnikov, A., Belgacem, H., de Magistris, M., Dghais, W. and Maffucci, A., (2020). Signal and Thermal Integrity Analysis of 3-D Stacked Resistive Random-Access Memories. IEEE Transactions on Electron Devices, 68(1), pp.88-94. DOI : 10.1109/TED.2020.3036574.

Conference Publications:

[P.1] Lahbacha, K., Zayer, F., Dghais, W., Maffucci, A., & Belgacem, H. (2020). Reliable 3D 1D1R-1R1D Solution for Victim Layers in Monolithic RRAM Integration. In Proc. of 2020 IEEE International Conference on Design & Test of Integrated Micro & Nano-Systems (DTS), Hammamet, Tunisia, 7-10 June 2020, pp.1-4, article number 9196043, DOI: 10.1109/DTS48731.2020.9196043.

[P.2] Lahbacha, K., Belgacem, H., Dghais, W., Zayer, F. and Maffucci, A., (2021). High Density RRAM Arrays with Improved Thermal and Signal Integrity. In Proc. of 2021 IEEE 25th Workshop on Signal and Power Integrity (SPI), Siegen, Germany, 10-12 May 2021, pp. 1-4, article number 21015831, DOI: 10.1109/SPI52361.2021.9505230.

[P.3] Lahbacha, K., Belgacem, H., Dghais, W., Zayer, F. and Maffucci, A., (2021). Electrothermal RRAM Crossbar Improvement with 3-D CRS and 1D1R-1R1D Architectures. In Proc.of 2021 IEEE International Conference on Design & Test of Integrated Micro & Nano-Systems (DTS), Sfax, Tunisia, 7-10 June 2021, pp. 1-5, article number 21045453, DOI: 10.1109/DTS52014.2021.9498259.

[P.4] Zayer, F., Lahbacha, K., Dghais, W., Belgacem, H., de Magistris, M., Maffucci, A., & Melnikov, A. V. (2019). Electrothermal analysis of 3D Memristive 1D-1RRAM Crossbar with Carbon Nanotube Electrodes. In Proc.of 2019 IEEE international Conference on Design & Test of integrated micro & nano-Systems (DTS), Gammarth, Tunisia, 28 April-1 May 2019, pp.1-6, article number 19191837, DOI: 10.1109/DTSS.2019.8915266.

[P.5] Zayer, F., Lahbacha, K., Dghais, W., Belgacem, H., de Magistris, M., Maffucci, A., & Melnikov, A. V. (2019). Thermal and Signal Integrity Analysis of Novel 3D Crossbar Resistive Random-Access Memories. In Proc.of 2019 IEEE 23rd Workshop on Signal and Power Integrity (SPI), Chambéry, France, 18-21 June 2019, pp. 1-4, article number 18883423, DOI: 10.1109/SaPIW.2019.8781680.

REFERENCES

Ahn, E. C., Wong, H. S. P., & Pop, E. (2018). Carbon nanomaterials for non-volatile memories. Nature Reviews Materials, 3(3), 1-15.

Akinaga, H., & Shima, H. (2010). Resistive random access memory (ReRAM) based on metal oxides. Proceedings of the IEEE, 98(12), 2237-2251.

Al-Hartomy, O. A., Khasim, S., Roy, A., & Pasha, A. (2019). Highly conductive polyaniline/graphene nano-platelet composite sensor towards detection of toluene and benzene gases. Applied Physics A, 125(1), 1-9.

Amer, S., & Rose, G. S. (2019, March). A multi-driver write scheme for reliable and energy efficient 1s1r reram crossbar arrays. In 20th International Symposium on Quality Electronic Design (ISQED) (pp. 64-69). IEEE.

An, L., & Friedrich, C. R. (2012). Measurement of contact resistance of multiwall carbon nanotubes by electrical contact using a focused ion beam. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 272, 169-172.

Argall, F. (1968). Switching phenomena in titanium oxide thin films. Solid-State Electronics, 11(5), 535-541.

Baek, I. G., Lee, M. S., Seo, S., Lee, M. J., Seo, D. H., Suh, D. S., ... & Moon, J. T. (2004, December). Highly scalable nonvolatile resistive memory using simple binary oxide driven by asymmetric unipolar voltage pulses. In IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004. (pp. 587-590). IEEE.

Bailey, C. (2008, December). Thermal management technologies for electronic packaging: current capabilities and future challenges for modelling tools. In 2008 10th Electronics Packaging Technology Conference (pp. 527-532). IEEE.

Batude, P., Vinet, M., Previtali, B., Tabone, C., Xu, C., Mazurier, J., ... & Poiroux, T. (2011, December). Advances, challenges and opportunities in 3D CMOS sequential integration. In 2011 International Electron Devices Meeting (pp. 7-3). IEEE.

Bellagamba, I., Boccuni, F., Ferrante, R., Tombolini, F., Marra, F., Sarto, M. S., & Iavicoli, S. (2020). Workers' exposure assessment during the production of graphene nanoplatelets in R&D laboratory. Nanomaterials, 10(8), 1520.

Bertaud, T., Walczyk, D., Walczyk, C., Kubotsch, S., Sowinska, M., Schroeder, T., ... & Grampeix, H. (2012). Resistive switching of HfO2-based Metal–Insulator–Metal diodes: Impact of the top electrode material. Thin Solid Films, 520(14), 4551-4555.

Burr, G. W., Kurdi, B. N., Scott, J. C., Lam, C. H., Gopalakrishnan, K., & Shenoy, R. S. (2008). Overview of candidate device technologies for storage-class memory. IBM Journal of Research and Development, 52(4.5), 449-464.

Cagli, C., Buckley, J., Jousseaume, V., Cabout, T., Salaun, A., Grampeix, H., ... & De Salvo, B. (2011, December). Experimental and theoretical study of

electrode effects in HfO 2 based RRAM. In 2011 International Electron Devices Meeting (pp. 28-7). IEEE.

Carotenuto, A., Giovinco, G., Viglietti, B., & Vanoli, L. (2005). A new procedure for the determination of calibration curves for a gas chromatograph used in natural gas analysis. Chemometrics and intelligent laboratory systems, 75(2), 209-217.

Castillo, A. D. R., Pellegrini, V., Ansaldo, A., Ricciardella, F., Sun, H., Marasco, L., ... & Bonaccorso, F. (2018). High-yield production of 2D crystals by wet-jet milling. Materials Horizons, 5(5), 890-904.

Chang, M. (2007, February). Foundry future: Challenges in the 21st century. In 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (pp. 18-23). IEEE.

Chen, P. Y., Peng, X., & Yu, S. (2018). NeuroSim: A circuit-level macro model for benchmarking neuro-inspired architectures in online learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 37(12), 3067-3080.

Chen, M. C., Chang, T. C., Tsai, C. T., Huang, S. Y., Chen, S. C., Hu, C. W., ... & Tsai, M. J. (2010). Influence of electrode material on the resistive memory switching property of indium gallium zinc oxide thin films. Applied Physics Letters, 96(26), 262110.

Chen, A. (2013, August). Emerging memory selector devices. In 2013 13th Non-Volatile Memory Technology Symposium (NVMTS) (pp. 1-5). IEEE.

Chiariello, A. G., Miano, G., & Maffucci, A. (2010, October). Size and temperature effects on the resistance of copper and carbon nanotubes nano-interconnects. In 19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems (pp. 97-100). IEEE.

Chiodarelli, N., Fournier, A., & Dijon, J. (2013). Impact of the contact's geometry on the line resistivity of carbon nanotubes bundles for applications as horizontal interconnects. Applied Physics Letters, 103(5), 053115.

Chiodarelli, N., Fournier, A., Okuno, H., & Dijon, J. (2013). Carbon nanotubes horizontal interconnects with end-bonded contacts, diameters down to 50 nm and lengths up to 20 μm. Carbon, 60, 139-145.

Cho, E., Han, S., Ahn, H. S., Lee, K. R., Kim, S. K., & Hwang, C. S. (2006). First-principles study of point defects in rutile Ti O 2− x. Physical Review B, 73(19), 193202.

Chua, L. (1971). Memristor-the missing circuit element. IEEE Transactions on circuit theory, 18(5), 507-519.

Chua, L. (2019). Resistance switching memories are memristors. In Handbook of memristor networks (pp. 197-230). Springer, Cham.

Chu, K., Lee, S. C., Lee, S., Kim, D., Moon, C., & Park, S. H. (2015). Smart conducting polymer composites having zero temperature coefficient of resistance. Nanoscale, 7(2), 471-478.

Ciarlet, P. G. (2002). The finite element method for elliptic problems. Society for Industrial and Applied Mathematics.

Dabrowska, A., Bellucci, S., Cataldo, A., Micciulla, F., & Huczko, A. (2014). Nanocomposites of epoxy resin with graphene nanoplates and exfoliated graphite: Synthesis and electrical properties. physica status solidi (b), 251(12), 2599-2602.

De Salvo, B. (2013). Silicon non-volatile memories: paths of innovation. John Wiley & Sons.

Fakhreddine, Z., Lahbacha, K., Melnikov, A., Belgacem, H., de Magistris, M., Dghais, W., & Maffucci, A. (2020). Signal and Thermal Integrity Analysis of 3-D Stacked Resistive Random Access Memories. IEEE Transactions on Electron Devices, 68(1), 88-94.

Ferrigno, L., Cataldo, A., Sibilia, S., Maffucci, A., & Bellucci, S. (2019). A monitorable and renewable pollution filter based on graphene nanoplatelets. Nanotechnology, 31(7), 075701.

Forestiere, C., Maffucci, A., & Miano, G. (2010). Hydrodynamic model for the signal propagation along carbon nanotubes. Journal of Nanophotonics, 4(1), 041695.

Forestiere, C., Maffucci, A., & Miano, G. (2011). On the evaluation of the number of conducting channels in multiwall carbon nanotubes. IEEE Transactions on Nanotechnology, 10(6), 1221-1223.

Gonon, P., Mougenot, M., Vallée, C., Jorel, C., Jousseaume, V., Grampeix, H., & El Kamel, F. (2010). Resistance switching in HfO 2 metal-insulator-metal devices. Journal of Applied Physics, 107(7), 074507.

Goux, L., Czarnecki, P., Chen, Y. Y., Pantisano, L., Wang, X., Degraeve, R., ... & Altimime, L. (2010). Evidences of oxygen-mediated resistive-switching mechanism in TiN\HfO 2\Pt cells. Applied Physics Letters, 97(24), 243509.

Gül, F. (2019). Addressing the sneak-path problem in crossbar RRAM devices using memristor-based one Schottky diode-one resistor array. Results in Physics, 12, 1091-1096.

Gutierrez, H. M., Christoffersen, C. E., & Steer, M. B. (1999, October). An integrated environment for the simulation of electrical, thermal and electromagnetic interactions in high-performance integrated circuits. In IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging (Cat. No. 99TH8412) (pp. 217-220). IEEE.

Han, S., Chand, A., Araby, S., Cai, R., Chen, S., Kang, H., ... & Meng, Q. (2019). Thermally and electrically conductive multifunctional sensor based on epoxy/graphene composite. Nanotechnology, 31(7), 075702.

Hickmott, T. W. (1962). Low-frequency negative resistance in thin anodic oxide films. Journal of Applied Physics, 33(9), 2669-2682.

Hoefflinger, B. (2011). ITRS: The international technology roadmap for semiconductors. In Chips 2020 (pp. 161-174). Springer, Berlin, Heidelberg.

Hoefflinger, B. (2020). IRDS—International Roadmap for Devices and Systems, Rebooting Computing, S3S. In NANO-CHIPS 2030 (pp. 9-17). Springer, Cham.

Huang, J. J., Hou, T. H., Hsu, C. W., Tseng, Y. M., Chang, W. H., Jang, W. Y., & Lin, C. H. (2012). Flexible one diode–one resistor crossbar resistive-switching memory. Japanese journal of applied physics, 51(4S), 04DD09.

Huang, J., Yang, X., Her, S. C., & Liang, Y. M. (2019). Carbon nanotube/graphene nanoplatelet hybrid film as a flexible multifunctional sensor. Sensors, 19(2), 317.

Hui, F., Grustan-Gutierrez, E., Long, S., Liu, Q., Ott, A. K., Ferrari, A. C., & Lanza, M. (2017). Graphene and related materials for resistive random access memories. Advanced Electronic Materials, 3(8), 1600195.

Ielmini, D., & Waser, R. (Eds.). (2015). Resistive switching: from fundamentals of nanoionic redox processes to memristive device applications. John Wiley & Sons.

Ielmini, D. (2011). Modeling the universal set/reset characteristics of bipolar RRAM by field-and temperature-driven filament growth. IEEE Transactions on Electron Devices, 58(12), 4309-4317.

Ielmini, D., Nardi, F., & Cagli, C. (2011). Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories. Nanotechnology, 22(25), 254022.

Iwai, H. (2015). Future of nano CMOS technology. Solid-State Electronics, 112, 56-67.

Jakopović, Ž., Šunde, V., & Benčić, Z. (2001). Electro-thermal modelling and simulation of a power-MOSFET. Automatika: časopis za automatiku, mjerenje, elektroniku, računarstvo i komunikacije, 42(1-2), 71-77.

Janicki, M., De Mey, G., & Napieralski, A. (2002). Application of Green's functions for analysis of transient thermal states in electronic circuits. Microelectronics Journal, 33(9), 733-738.

Jen, Y. M., & Huang, J. C. (2019). Synergistic effect on the thermomechanical and electrical properties of epoxy composites with the enhancement of carbon nanotubes and graphene nano platelets. Materials, 12(2), 255.

Jeong, D. S., Schroeder, H., Breuer, U., & Waser, R. (2008). Characteristic electroforming behavior in Pt/TiO 2/Pt resistive switching cells depending on atmosphere. Journal of applied physics, 104(12), 123716.

Jiang, H., Wang, H., Liu, G., Su, Z., Wu, J., Liu, J., ... & Zhou, W. (2017). Light-weight, flexible, low-voltage electro-thermal film using graphite

nanoplatelets for wearable/smart electronics and deicing devices. Journal of Alloys and Compounds, 699, 1049-1056.

Karim, N., Zhang, M., Afroj, S., Koncherry, V., Potluri, P., & Novoselov, K. S. (2018). Graphene-based surface heater for de-icing applications. RSC advances, 8(30), 16815-16823.

Khattak, Z., & Ali, H. M. (2019). Air cooled heat sink geometries subjected to forced flow: A critical review. International Journal of Heat and Mass Transfer, 130, 141-161.

Kim, H., Sah, M. P., & Adhikari, S. P. (2012). Pinched hysteresis loops is the fingerprint of memristive devices. arXiv preprint arXiv:1202.2437.

Kim, S., Zhou, J., & Lu, W. D. (2014). Crossbar RRAM arrays: Selector device requirements during write operation. IEEE Transactions on Electron Devices, 61(8), 2820-2826.

Kim, S., Kulkarni, D. D., Rykaczewski, K., Henry, M., Tsukruk, V. V., & Fedorov, A. G. (2012). Fabrication of an ultralow-resistance ohmic contact to MWCNT–metal interconnect using graphitic carbon by electron beam-induced deposition (EBID). IEEE transactions on nanotechnology, 11(6), 1223-1230.

Koskinen, T., Juntunen, T., & Tittonen, I. (2020). Large-area thermal distribution sensor based on multilayer graphene ink. Sensors, 20(18), 5188.

Kovtun, A., Treossi, E., Mirotta, N., Scidà, A., Liscio, A., Christian, M., ... & Palermo, V. (2019). Benchmarking of graphene-based materials: real commercial products versus ideal graphene. 2D Materials, 6(2), 025006.

Kumar, S., Bhatt, K., Kumar, P., Sharma, S., Kumar, A., & Tripathi, C. C. (2019). Laser patterned, high-power graphene paper resistor with dual temperature coefficient of resistance. RSC advances, 9(15), 8262-8270.

Kumar, V., Kaur, I., Arora, S., Mehla, R., Vellingiri, K., & Kim, K. H. (2020). Graphene nanoplatelet/graphitized nanodiamond-based nanocomposite for mediator-free electrochemical sensing of urea. Food chemistry, 303, 125375.

Lahbacha, K., Zayer, F., Dghais, W., Maffucci, A., & Belgacem, H. (2020, June). Reliable 3D 1D1R-1R1D Solution for Victim Layers in Monolithic RRAM Integration. In 2020 IEEE International Conference on Design & Test of Integrated Micro & Nano-Systems (DTS) (pp. 1-4). IEEE.

Lanza, M. (2014). A review on resistive switching in high-k dielectrics: A nanoscale point of view using conductive atomic force microscope. Materials, 7(3), 2155-2182.

Larentis, S., Nardi, F., Balatti, S., Gilmer, D. C., & Ielmini, D. (2012). Resistive switching by voltage-driven ion migration in bipolar RRAM—Part II: Modeling. IEEE Transactions on Electron Devices, 59(9), 2468-2475.

Lee, J., & Mudawar, I. (2008). Fluid flow and heat transfer characteristics of low temperature two-phase micro-channel heat sinks–Part 1: Experimental

methods and flow visualization results. International Journal of Heat and Mass Transfer, 51(17-18), 4315-4326.

Lee, J., & Mudawar, I. (2009). Low-temperature two-phase microchannel cooling for high-heat-flux thermal management of defense electronics. IEEE transactions on components and packaging technologies, 32(2), 453-465.

Lee, H. Y., Chen, P. S., Wu, T. Y., Chen, Y. S., Wang, C. C., Tzeng, P. J., ... & Tsai, M. J. (2008, December). Low power and high speed bipolar switching with a thin reactive Ti buffer layer in robust HfO2 based RRAM. In 2008 IEEE International Electron Devices Meeting (pp. 1-4). IEEE.

Lee, H. Y., Chen, Y. S., Chen, P. S., Gu, P. Y., Hsu, Y. Y., Wang, S. M., ... & Tsai, M. J. (2010, December). Evidence and solution of over-RESET problem for HfO x based resistive memory with sub-ns switching speed and high endurance. In 2010 International Electron Devices Meeting (pp. 19-7). IEEE.

Lee, J., Shin, J., Lee, D., Lee, W., Jung, S., Jo, M., ... & Hwang, H. (2010, December). Diode-less nano-scale ZrO x/HfO x RRAM device with excellent switching uniformity and reliability for high-density cross-point memory applications. In 2010 International Electron Devices Meeting (pp. 19-5). IEEE.

Liang, J., Chen, R., Ramos, R., Lee, J., Okuno, H., Kalita, D., ... & Todri-Sanial, A. (2019). Investigation of Pt-salt-doped-standalone-multiwall carbon nanotubes for on-chip interconnect applications. IEEE Transactions on Electron Devices, 66(5), 2346-2352.

Liang, J., & Wong, H. S. P. (2010). Cross-point memory array without cell selectors—Device characteristics and data storage pattern dependencies. IEEE Transactions on Electron Devices, 57(10), 2531-2538.

Li, S., Chen, W., Luo, Y., Hu, J., Gao, P., Ye, J., ... & Yin, W. Y. (2017). Fully coupled multiphysics simulation of crosstalk effect in bipolar resistive random access memory. IEEE Transactions on Electron Devices, 64(9), 3647-3653.

Liu, C., Miao, L., Hu, D., Huang, R., Fisher, C. A. J., Tanemura, S., & Gu, H. (2013). Enhanced asymmetrical transport of carriers induced by local structural distortion in chemically tuned titania: A possible mechanism for enhancing thermoelectric properties. Physical Review B, 88(20), 205201.

Long, S., Perniola, L., Cagli, C., Buckley, J., Lian, X., Miranda, E., ... & Suñé, J. (2013). Voltage and power-controlled regimes in the progressive unipolar RESET transition of HfO 2-based RRAM. Scientific reports, 3(1), 1-8.

López, R., & Sánchez, D. (2013). Nonlinear heat transport in mesoscopic conductors: Rectification, Peltier effect, and Wiedemann-Franz law. Physical Review B, 88(4), 045129.

Luo, S., & Liu, T. (2013). SWCNT/graphite nanoplatelet hybrid thin films for self-temperature-compensated, highly sensitive, and extensible piezoresistive sensors. Advanced Materials, 25(39), 5650-5657.

Luo, Y., Chen, W., Cheng, M., & Yin, W. Y. (2016). Electrothermal characterization in 3-D resistive random access memory arrays. IEEE Transactions on Electron Devices, 63(12), 4720-4728.

Luo, Y., Chen, W., Cheng, M., Kang, K., & Yin, W. Y. (2016, July). Electrothermal simulation of Resistive Random Access Memory (RRAM) array using finite difference method. In 2016 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP) (pp. 1-3). IEEE.

Maffucci, A., & Miano, G. (2013). Number of conducting channels for armchair and zig-zag graphene nanoribbon interconnects. IEEE transactions on nanotechnology, 12(5), 817-823.

Maffucci, A., & Miano, G. (2013). Number of conducting channels for armchair and zig-zag graphene nanoribbon interconnects. IEEE transactions on nanotechnology, 12(5), 817-823.

Maffucci, A., Todri Sanial, A., & Dijon, J. (2016). Carbon Nanotubes for Interconnects: Process, Design and Applications Compatibility, 57(6), 1645-1654.

Maffucci, A., Micciulla, F., Cataldo, A., Miano, G., & Bellucci, S. (2016). Bottom-up realization and electrical characterization of a graphene-based device. Nanotechnology, 27(9), 095204.

Maffucci, A., Micciulla, F., Cataldo, A. E., Miano, G., & Bellucci, S. (2017). Modeling, fabrication, and characterization of large carbon nanotube interconnects with negative temperature coefficient of the resistance. IEEE Transactions on Components, Packaging and Manufacturing Technology, 7(4), 485-493.

Magnani, A., De Magistris, M., Todri-Sanial, A., & Maffucci, A. (2016). Electrothermal analysis of carbon nanotubes power delivery networks for nanoscale integrated circuits. IEEE Transactions on Nanotechnology, 15(3), 380-388.

Mariani, E., & von Oppen, F. (2010). Temperature-dependent resistivity of suspended graphene. Physical Review B, 82(19), 195403.

Marucco, J. F., Gautron, J., & Lemasson, P. (1981). Thermogravimetric and electrical study of non-stoichiometric titanium dioxide TiO2− x, between 800 and 1100° C. Journal of Physics and Chemistry of Solids, 42(5), 363-367.

Mattioli, G., Filippone, F., Alippi, P., & Bonapasta, A. A. (2008). Ab initio study of the electronic states induced by oxygen vacancies in rutile and anatase TiO 2. Physical Review B, 78(24), 241201.

Milošević, N. D., & Maglić, K. D. (2006). Thermophysical properties of solid phase hafnium at high temperatures. International journal of thermophysics, 27(2), 530-553.

Mohiuddin, M., & Hoa, S. V. (2011). Temperature dependent electrical conductivity of CNT–PEEK composites. Composites Science and Technology, 72(1), 21-27.

Moore, G. E. (2006). Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp. 114 ff. IEEE solid-state circuits society newsletter, 11(3), 33-35.

Moore, G. E. (1965). The Future of Integrated Electronics, Fairchild Semiconductor. Electronics magazine.

Morris, J. E. (2018). Nanopackaging: Nanotechnologies and electronics packaging. In Nanopackaging (pp. 1-44). Springer, Cham.

Nauenheim, C., Kugeler, C., Rudiger, A., Waser, R., Flocke, A., & Noll, T. G. (2008, August). Nano-crossbar arrays for nonvolatile resistive RAM (RRAM) applications. In 2008 8th IEEE Conference on Nanotechnology (pp. 464-467). IEEE.

Neitzert, H. C., Vertuccio, L., & Sorrentino, A. (2010). Epoxy/MWCNT composite as temperature sensor and electrical heating element. IEEE transactions on nanotechnology, 10(4), 688-693.

Nozières, J. P. (2010). Têtes de lecture et mémoires magnétiques. Reflets de la physique, (18), 12-16.

Panzer, M. A., Shandalov, M., Rowlette, J. A., Oshima, Y., Chen, Y. W., McIntyre, P. C., & Goodson, K. E. (2009). Thermal properties of ultrathin hafnium oxide gate dielectric films. IEEE Electron Device Letters, 30(12), 1269-1271.

Park, S. G., Magyari-Köpe, B., & Nishi, Y. (2010). Impact of Oxygen Vacancy Ordering on the Formation of a Conductive Filament in $\hbox {TiO} _ {2} $ for Resistive Switching Memory. IEEE Electron Device Letters, 32(2), 197-199.

Pesare, M., Giorgio, A., & Perri, A. G. (2001). An analytical method for the thermal layout optimisation of multilayer structure solid-state devices. Solid-State Electronics, 45(3), 511-517.

Prolongo, S. G., Moriche, R., Del Rosario, G., Jiménez-Suárez, A., Prolongo, M. G., & Ureña, A. (2016). Joule effect self-heating of epoxy composites reinforced with graphitic nanofillers. Journal of Polymer Research, 23(9), 1-7.

Raoux, S., Burr, G. W., Breitwisch, M. J., Rettner, C. T., Chen, Y. C., Shelby, R. M., ... & Lam, C. H. (2008). Phase-change random access memory: A scalable technology. IBM Journal of Research and Development, 52(4.5), 465-479.

Reohr, W., Honigschmid, H., Robertazzi, R., Gogl, D., Pesavento, F., Lammers, S., ... & Muller, G. (2002). Memories of tomorrow. IEEE circuits and devices magazine, 18(5), 17-27.

Russo, U., Ielmini, D., Cagli, C., & Lacaita, A. L. (2009). Filament conduction and reset mechanism in NiO-based resistive-switching memory (RRAM) devices. IEEE Transactions on Electron Devices, 56(2), 186-192.

Sabry, M. N. (1999). Static and dynamic thermal modeling of ICs. Microelectronics Journal, 30(11), 1085-1091.

Shahil, K. M., & Balandin, A. A. (2012). Graphene–multilayer graphene nanocomposites as highly efficient thermal interface materials. Nano letters, 12(2), 861-867.

Sheu, S. S., Chiang, P. C., Lin, W. P., Lee, H. Y., Chen, P. S., Chen, Y. S., ... & Tsai, M. J. (2009, June). A 5ns fast write multi-level non-volatile 1 K bits RRAM memory with advance write scheme. In 2009 Symposium on VLSI Circuits (pp. 82-83). IEEE.

Simmons, J. G. (1971). Conduction in thin dielectric films. Journal of Physics D: Applied Physics, 4(5), 613.

Slepyan, G. Y., Boag, A., Mordachev, V., Sinkevich, E., Maksimenko, S., Kuzhir, P., ... & Maffucci, A. (2015). Nanoscale electromagnetic compatibility : quantum coupling and matching in nanocircuits. IEEE Transactions on Electromagnetic.

Smovzh, D. V., Kostogrud, I. A., Boyko, E. V., Matochkin, P. E., & Pilnik, A. A. (2020). Joule heater based on single-layer graphene. Nanotechnology, 31(33), 335704.

Steinhögl, W., Schindler, G., Steinlesberger, G., Traving, M., & Engelhardt, M. (2005). Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller. Journal of Applied Physics, 97(2), 023706.

bStrukov, D. B., Snider, G. S., Stewart, D. R., & Williams, R. S. (2008). The missing memristor found. nature, 453(7191), 80-83.

Sun, P., Lu, N., Li, L., Li, Y., Wang, H., Lv, H., ... & Liu, M. (2015). Thermal crosstalk in 3-dimensional RRAM crossbar array. Scientific reports, 5(1), 1-9.

Sun, W., Choi, S., & Shin, H. (2016). A new bias scheme for a low power consumption ReRAM crossbar array. Semiconductor Science and Technology, 31(8), 085009.

Tan, Y. W., Zhang, Y., Stormer, H. L., & Kim, P. (2007). Temperature dependent electron transport in graphene. The European Physical Journal Special Topics, 148(1), 15-18.

Theis, T. N., & Wong, H. S. P. (2017). The end of moore's law: A new beginning for information technology. Computing in Science & Engineering, 19(2), 41-50.

Thomas, J. W. (2013). Numerical partial differential equations: finite difference methods (Vol. 22). Springer Science & Business Media.

Tian, M., Huang, Y., Wang, W., Li, R., Liu, P., Liu, C., & Zhang, Y. (2014). Temperature-dependent electrical properties of graphene nanoplatelets film

dropped on flexible substrates. Journal of Materials Research, 29(11), 1288-1294.

Todri-Sanial, A., Dijon, J., & Maffucci, A. (2017). Carbon nanotubes for Interconnects. Berlin, Germany:: Springer.

Tseng, Y. T., Chen, P. H., Chang, T. C., Chang, K. C., Tsai, T. M., Shih, C. C., ... & Sze, S. M. (2017). Solving the Scaling Issue of Increasing Forming Voltage in Resistive Random Access Memory Using High-k Spacer Structure. Advanced Electronic Materials, 3(9), 1700171.

Türkes, P., & Sigg, J. (1998). Electro-thermal simulation of power electronic systems. Microelectronics journal, 29(11), 785-790.

Vallée, C., Gonon, P., Mannequin, C., Chevolleau, T., Bonvalot, M., Grampeix, H., ... & Jousseaume, V. (2011). Plasma treatment of HfO2-based metal–insulator–metal resistive memories. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 29(4), 041512.

Vellvehi, M., Jordà, X., Godignon, P., & Millan, J. (2006, April). Electro-thermal simulation of a DC/DC converter using a relaxation method. In EuroSime 2006-7th International Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems (pp. 1-7). IEEE.

Vorotilov, K. A., & Sigov, A. (2012). Ferroelectric memory. Physics of the Solid State, 54(5), 894-899.

Wang, R., Xu, Z., Zhuang, J., Liu, Z., Peng, L., Li, Z., ... & Gao, C. (2017). Highly stretchable graphene fibers with ultrafast electrothermal response for low-voltage wearable heaters. Advanced Electronic Materials, 3(2), 1600425.

Waser, R., Dittmann, R., Staikov, G., & Szot, K. (2009). Redox-based resistive switching memories–nanoionic mechanisms, prospects, and challenges. Advanced materials, 21(25-26), 2632-2663.

Waser, R., Dittmann, R., Salinga, M., & Wuttig, M. (2010). Function by defects at the atomic scale–New concepts for non-volatile memories. Solid-state electronics, 54(9), 830-840.

Wilhite, P., Vyas, A. A., Tan, J., Tan, J., Yamada, T., Wang, P., ... & Yang, C. Y. (2014). Metal–nanocarbon contacts. Semiconductor Science and Technology, 29(5), 054006.

Wójciak, W., & Napieralski, A. (1997). Thermal monitoring of a single heat source in semiconductor devices—the first approach. Microelectronics journal, 28(3), 313-316.

Wong, H. S. P., Lee, H. Y., Yu, S., Chen, Y. S., Wu, Y., Chen, P. S., ... & Tsai, M. J. (2012). Metal–oxide RRAM. Proceedings of the IEEE, 100(6), 1951-1970.

Wu, H., & Drzal, L. T. (2012). Graphene nanoplatelet paper as a light-weight composite with excellent electrical and thermal conductivity and good gas barrier properties. Carbon, 50(3), 1135-1145.

Xu, G. (2007, March). Evaluation of a liquid cooling concept for high power processors. In Twenty-Third Annual IEEE Semiconductor Thermal Measurement and Management Symposium (pp. 190-195). IEEE.

Yang, Y., Sheridan, P., & Lu, W. (2012). Complementary resistive switching in tantalum oxide-based resistive memory devices. Applied Physics Letters, 100(20), 203112.

Yang, J. J., Inoue, I. H., Mikolajick, T., & Hwang, C. S. (2012). Metal oxide memories based on thermochemical and valence change mechanisms. MRS bulletin, 37(2), 131-137.

Young, R. J., Kinloch, I. A., Gong, L., & Novoselov, K. S. (2012). The mechanics of graphene nanocomposites: a review. Composites Science and Technology, 72(12), 1459-1476.

Zahoor, F., Zulkifli, T. Z. A., & Khanday, F. A. (2020). Resistive random access memory (RRAM): an overview of materials, switching mechanism, performance, multilevel cell (MLC) storage, modeling, and applications. Nanoscale research letters, 15(1), 1-26.

Zayer, F., Dghais, W., Benabdeladhim, M., & Hamdi, B. (2019). Low power, ultrafast synaptic plasticity in 1R-ferroelectric tunnel memristive structure for spiking neural networks. AEU-International Journal of Electronics and Communications, 100, 56-65.

Zayer, F., Dghais, W., & Belgacem, H. (2019). Modeling framework and comparison of memristive devices and associated STDP learning windows for neuromorphic applications. Journal of Physics D: Applied Physics, 52(39), 393002.

Zayer, F., Lahbacha, K., Dghais, W., Belgacem, H., de Magistris, M., Maffucci, A., & Melnikov, A. V. (2019, June). Thermal and signal integrity analysis of novel 3D crossbar resistive random access memories. In 2019 IEEE 23rd Workshop on Signal and Power Integrity (SPI) (pp. 1-4). IEEE.

Zayer, F., Lahbacha, K., Dghais, W., Belgacem, H., de Magistris, M., Melnikov, A. V., & Maffucci, A. (2019, April). Electrothermal analysis of 3D memristive 1D-1RRAM crossbar with carbon nanotube electrodes. In 2019 IEEE International Conference on Design & Test of Integrated Micro & Nano-Systems (DTS) (pp. 1-6). IEEE.

Zhang, Z. M., Zhang, Z. M., & Luby. (2007). Nano/microscale heat transfer (Vol. 410). New York: McGraw-Hill.

Zhao, S., Lou, D., Zhan, P., Li, G., Dai, K., Guo, J., ... & Guo, Z. (2017). Heating-induced negative temperature coefficient effect in conductive graphene/polymer ternary nanocomposites with a segregated and double-percolated structure. Journal of Materials Chemistry C, 5(32), 8233-8242.

Zhu, G., Chen, W., Wang, D., Xie, H., Zhao, Z., Gao, P., ... & Yin, W. Y. (2019). Study on high-density integration resistive random access memory array from

multiphysics perspective by parallel computing. IEEE Transactions on Electron Devices, 66(4), 1747-1753.

http://www.explainthatstuff.com/integratedcircuits.

http://www.nanesa.com/en-US/Graphene

https://www.comsol.com/comsol-multiphysics