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Analysis of Multistage DC/AC converter based on Pulsating DC link principle

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To my parents, my brother and my two sisters
for their love, patience and support.

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ABSTRACT

Nowadays the different application fields of the Power Electronics and the industries are demanding incessant enhancements of the features of power converter as efficiency, reliability and power density. To answer to this request, the researchers are pushing the limits of these features thanks to the growing use of Wide band-gap (WBG) power devices, new improvements in the field of power magnetics and new topologies of converter. The aim of this thesis is present the results of complete analysis of new topology of insulated DC/AC converter, based on the Pulsating DC link principle. A preliminary study of the topologies used in the field of multistage isolated DC/AC converter is presented, focusing the attention on the solutions based on Fixed DC link and the new architectures based on topology innovations and particular design. In particular in the horizon of the novel and innovative DC/AC insulated topologies, the attention was focalized on the Pulsating DC link Converter (PDLC), reliable architecture featured by pulsating evolution of the DC link thanks to the elimination of the intermediate filter. A novel version of the PDLC topology is presented, highlighting the interesting feature of the Zero Voltage Transition (ZVT) of the VSI stage, thanks to an accurate use of the pulsating DC link. Moreover it has been demonstrated how the action of Active Clamp circuit is strictly necessary, to minimize the overvoltage problem on the DC link voltage and manage the overvoltage associated energy. Successively a complete analysis of the proposed topology during the energising phases is reported, showing the equivalent representation of the PDLC and the relative differential equation system. According to this results a multiparametric analysis of the converter is performed, using accurate LTspice simulations, for different combinations of influence parameters. Thanks to this analysis, the design guidelines for the main components of the converter, as transformer and Active Clamp circuit, have been defined. Regarding the modulation techniques for this topology, a complete overview of the different operating principles is presented as well as the review of the techniques presented in literature. The attention has been focused on the techniques based on the ZVT of the inverter stage, since they permit the reduction of the switching losses of this stage. Specifically two different modulation techniques based on the described principle are presented, showing the different operating

principles and the relative implementations. The main difference between the two techniques is the relationship between the switching frequencies of the main power stages, that is a fundamental aspect in PDLC topology and influences the features of the modulation technique. To validate the analytical analysis and simulation results, a 30kW prototype of proposed PDLC topology has been implemented and the main details of the implementation are provided. To conclude the thesis, the prototype was fully characterized on resistive load and the principal results are presented, highlighting the ZVT of the Inverter stage and the results achieved with the two different modulation techniques.

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INTRODUCTION

In the last decades the role of Power Electronics has become central and fundamental in many industrial applications thanks to the introduction of new converter topologies, the availability of new very performing devices and the improvements in modulation and control techniques. Moreover the industries are incessantly demanding enhancements of features as efficiency, reliability and dimensions of converter, through the introduction of more strict requests and standards. Consequently these new constraints are pushing the research in this field toward new and innovative topologies based on new semiconductor devices as Wide band-gap (WBG) and/or new operation principle. The aim of this thesis is to analyse a new topology of multistage DC/AC converter based on the Pulsating DC link principle. This innovative architecture, called Pulsating DC link Converter (PDLC), is featured by pulsating evolution of the intermediate DC link, instead of the traditional fixed and controlled DC link. Thanks to the removal of intermediate filter stage, the system becomes more reliable and is capable to achieve the Zero Voltage Transition of the second stage. In particular this feature is achieved thanks to the use of an opportune modulation technique, that allows the commutations of the VSI stage during Zero portions (ZPs) of the Pulsating DC link voltage.

This thesis is organised as follow:

- In the first chapter the DC/AC insulated converter topology has been exploited, focalizing the attention on the architectures and on the challenges that the researchers are facing in this application field.
- The second chapter is focused on the Pulsating DC link Converter (PDLC) and its interesting features, highlighting aspects as the use of pulsating DC link for the ZVT of VSI stage and the necessity of adding a further power stage for the reduction of the overshoot voltage of the DC link.
- Instead in the third chapter the proposed PDLC architecture has been fully characterized, especially during the energising phases to analyse the evolution of the main features and the effects of the main influence parameters. In particular, LTSpice simulation are used to study the

evolution of Pulsating DC link voltage and primary current of transformer which have been investigated to define the design guidelines of the main components of this architecture. Moreover, the commutation of the first stage, Phase Shifted Bridge converter (PSB), have been studied to highlight the differences with the traditional version of PSB and see the effects of the removal of output filter on them.

- The fourth chapter is dedicated to the modulation techniques for the PDLC architecture and the requested features to exploit the peculiarities of this innovative power converter. The main operation principles of the modulation technique are presented and discussed and the main techniques present in literature are overviewed. In particular the attention is focused on the techniques based on the ZVT of the inverter stage and the related implementation.
- In the fifth and last chapter of this thesis two versions of PDLC prototypes are presented and discussed, providing accurate details on the power devices used and the implementation. Subsequently the experimental results, achieved with two different modulation technique based on the use of Pulsating voltage to achieve the ZVT of VSI stage are presented and compared. In particular aspects as the efficiency of the converter, quality of output voltage, ZVT commutation and operation of active Clamp are analysed according to the achieved results.

CHAPTER 1. DC/AC INSULATED CONVERTER

In the field of Power Electronics one of the most spread topology of power converters is the DC/AC converter family, also entitled Inverters, which allows the conversion of DC voltage source into a controlled AC voltage. They are used in different fields of application as Photovoltaic (PV) array, electrical Drives, electrical Vehicles and generally in all applications where it is necessary to supply loads with AC voltages from DC sources. The Inverters can be classified in the following two categories, according to the galvanic isolation between the input and the output:

- Not insulated: this category is featured by the absence of galvanic separation between the input and output terminals of the converter. If the application requires the isolation, it can be achieved connecting a transformer (Grid frequency transformer) at the output of inverter;
- Insulated: this category is based on multistage architecture where one or more stages are used to achieve the galvanic isolation feature, as showed in [1] where the solutions for Auxiliary power supply are investigated, while one is used for the conversion of electrical energy (from DC to AC). In particular the isolation is achieved thanks to a medium frequency transformer which works at frequencies greater than grid frequency (typically tens of kHz instead of 50Hz or 60Hz for U.S), allowing the reduction of volume and weight of the transformer. To simplify the study of this family, we can represent this topology as two stage power converter where the first stage is a generic Insulated DC/DC converter while the second stage is a common DC/AC converter. Figure 1 reports two possible schematizations of insulated topology.

The attention of this chapter and in general of this thesis, is focused on the insulated DC/AC converter because, thanks to the innovations in the fields of Power Electronics (new performing devices and soft-switching topologies) and electrical transformer (Planar solutions and new performing core material), this solution is most suitable and

performing for application as power supply for railway applications and solar power converter.

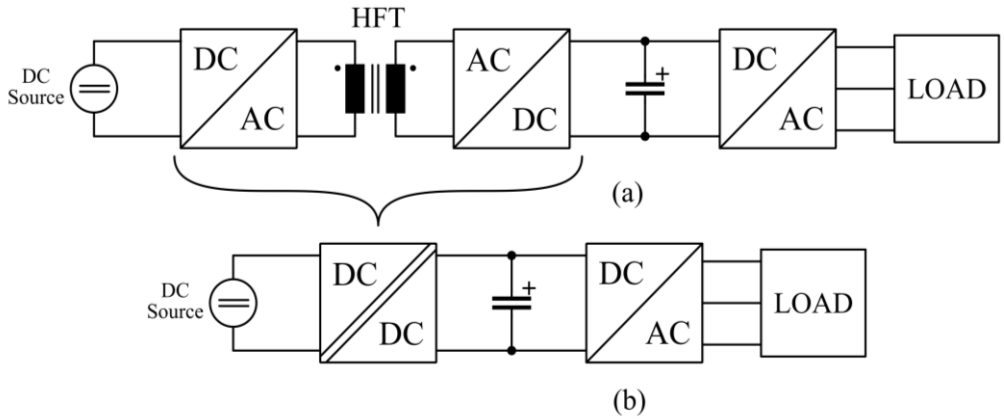

Figure 1 – Generic (a) and simplified (b) schematization of Insulated DC/AC architecture

1.1 Widespread architectures and modulation techniques

Starting from the simplified schematization of insulated DC/AC converter reported in Figure 1, the architectures can be distinguished according to the topology of first power stage since the second inverter stage is common to all the architectures considered. Moreover the first stage, apart from providing galvanic isolation, has to generate a controlled and stabilised DC output voltage, necessary for the operation of the second stage. This DC voltage is also known as Fixed DC link from which all the architecture based on that principle are indicated as Fixed DC Link Converter (FDLC). To obtain this feature it is necessary to use a filter made of a large capacitor and a large inductor, at the output of the first power stage to minimize the DC link voltage ripple whose frequency is usually twice the switching frequency of the first stage. The use of large capacitors and inductors causes the following two effects on the performances of the power converter:

- Worsening of its dynamic response because the output filter induces a pair of complex conjugate poles located close to the imaginary axis of the complex s-plane. These poles slow down the transient response of the converter and may cause stability problems to the system.
- Decoupling of the power stages that compose the FDLC, for which it is possible to use independent modulation techniques. In this way the interactions between the stages are minimized and the operation of single

stage can be optimised, to improve the overall performances of the converter. Practically the two power stages can be seen as two independent converters that are connected through the common DC bus.

As said before the first stage of FDLC is realised by two power stages, one operating as inverter while the other one operating as rectifier connected between each other through a medium frequency transformer. The topology of the two power stages is strongly influenced by the desired performances and the level of power. For example for the inverter stage the following main two architecture can be used:

- Half Bridge: There is just one leg of power switches which feeds the transformer with AC voltage with an amplitude equal to half input voltage. This solution is suitable for low-medium power application due to the lower losses of switches.
- Full Bridge: This solution is formed by two legs of power switches with the midpoints connected to the primary side of the transformer. Moreover, it is suitable for high power application due to generated AC voltage that is double of the half bridge solution.

For the rectifier stage the following two solutions can be used:

- Full Bridge: It is formed by two legs of power diodes which have to block the voltage on the secondary of transformer.
- Full Wave rectifier: This solution requires just two power diodes but the transformer must have two secondary windings (center tapped transformer) and every diode has to block twice the voltage on the secondary of the transformer. To improve the efficiency, the diodes can be replaced with MOSFETs to achieve the synchronous rectification (reduction of power losses during the conduction phases).

To conclude the choice of the rectifier stage is usually a trade-off between the efficiency of the power stage and the complexity of design and realisation of the medium frequency transformer.

Other solutions more performing and efficient for the implementation of insulated DC/DC converter can be found in the field of quasi-resonant and resonant converter. In particular the solutions more suitable and promising are: Phase Shifted Full Bridge (PSB) and the Series-Parallel Resonant Converter (LLC) which are characterized by Zero Voltage Switching (ZVS) in Turn-on commutations. The LLC converter is based on the resonance between the parameter of transformer and an external capacitor, which is designed to achieve the ZVS conditions for the Turn-on of the switches.

However this converter is modulated with a complex frequency control, which, together with the complicated design of Medium frequency transform due to the wide frequency range, makes this converter unsuitable for many high power applications. Instead the PSB is modulated with a simple modulation technique called Phase Shift Modulation which allows the control of output voltage through the phase shift between the driving signals of the legs of the full bridge. Moreover, the inductance necessary to achieve the ZVS conditions for the Turn-on of the switches can be integrated in the transformer as leakage inductance, saving space and weight. For these reasons the PSB is one of the most spread solution for the first stage of Insulated DC/AC converter. The schematic of PSB is depicted in Figure 2.

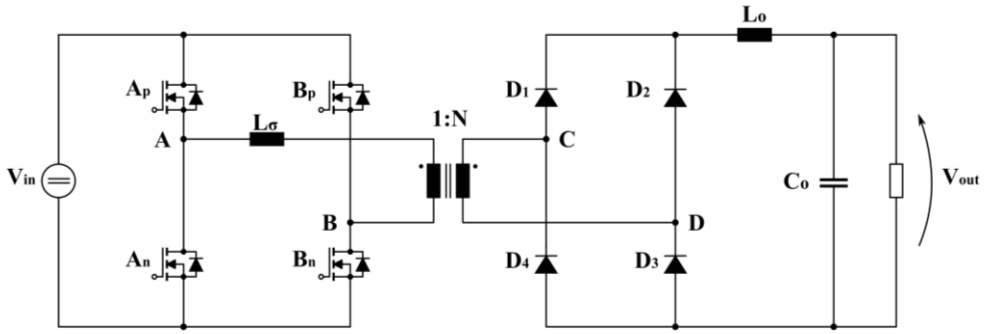

Figure 2 – Schematic of Phase Shifted Full Bridge (PSB)

Regarding the Inverter stage the most employed solution in FDLC architectures is the Two Level Voltage Source Inverter (VSI), whose three phase version is reported in Figure 3.

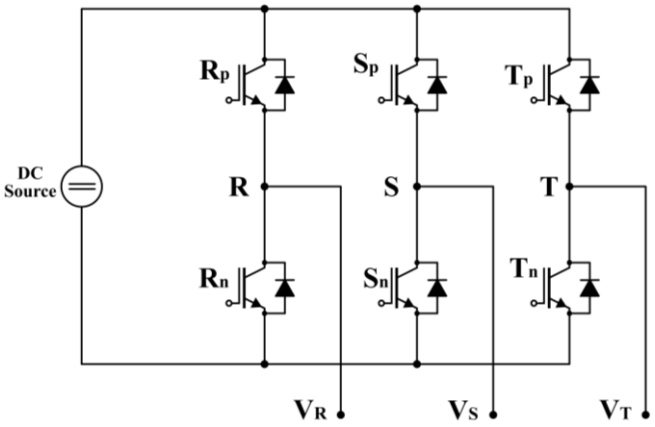

Figure 3 – Schematic of Two Level Voltage Source Inverter (VSI)

The power switches of each inverter leg are modulated in such a way to achieve, an alternative square output voltage at the fundamental frequency, which can achieve the sinusoidal shape thanks to the action of lowpass filter. The control of power switches is performed with modulation techniques that define the conduction and interdiction phases of the switches, using an appropriate dead time between the transitions of every leg to avoid the short circuit of the latter. The most known and used modulation techniques for three phase VSI are the following two:

- Sinusoidal Pulse Width Modulation (SPWM): is a particular case of PWM technique where the carrier signal at high frequency is compared with sinusoidal modulation signal at the fundamental frequency. Choosing an opportune value of modulation and frequency index, alternative square voltages with reduced harmonic content at low frequency can be obtained;
- Space Vector Modulation (SVM): is a digital technique based on the symmetric component of the three phase VSI, which permits the achievements of better performances than SPWM thanks to the absence of limits due to the overmodulation (huge limit of PWM) of the VSI . The symmetric component depends on the logic combination of the six switches of the VSI and the possible values can be represented with a voltage hexagon.

1.2 Challenges in the field of Insulated DC/AC Converter

As all the fields of Power Electronics, the research on the Insulated DC/AC Converter is continuously being accomplished to improve the main features of this architecture. In particular there are two reasons that are pushing the researchers to improve the quality of this architecture, thanks to the new technologies and materials. The first one is due to the industrial standards that, in the last decades, are demanding improvements in the fields of efficiency, physical dimensions and power density of these power converter. Together with these improvements the concept of reliability has become fundamental in every aspect of the power converter system as presented in [2], from the single components to the overall system, requiring much effort to achieve it. The other reason is due to the climate changes that are driving the economies to a decarbonization challenge as reported in [3], requiring the reduction of the use of fossil resources in the production of electrical energy. This challenge requires the wide use of renewable sources as Photovoltaic and Eolic to replace the

fossil resource. From the side of power converters, the aim is to minimize the losses of conversion and transmission of electrical energy to achieve the maximization of the energy utilization from the different users. According to these reasons, the main features of analysed architecture that are challenged by the researchers are the following:

- Maximise the efficiency of conversion thanks to the reduction of the power losses in the power converter. This is the main aim of researchers in the field of Power Electronics, which can be achieved improving the characteristics of power devices and introduce architecture based on new efficient and performing power devices. Moreover, the use of soft-switching technique is another way to reduce the switching losses of power devices.
- Improve the reliability of the system, using components and architecture more reliable and/or minimize the utilization of less reliable components. This target requires a deep analysis of every single element of power converter to study the failure mechanics and estimate the life cycle of the component. Moreover, more reliable design of component has been done to reduce the failure rate of components and extend their life cycle.
- Reduce the weight and volume of power converter using new materials and reducing the size of heatsinks, which is a consequence of the reduction of power losses of the architecture. Another aspect is to define new structure for magnetic components (transformer and inductor) that are featured by low profile and reduced weight, without compromising their main features.
- Increase the power density of the converter. This feature is a consequence of the increase of the Efficiency and the reduction of the volume.

In the next paragraphs every point of the above list is detailed to show limits we are facing today and what we can do in the future to overcome them.

1.2.1 Efficiency

The role of power devices based on Silicon (Si) in the field of Power Electronics is leading thanks to their features, production and manufactory cost. However in the last decades the continuous improvements requested by the power application have showed the physical limits of Silicon, especially for high frequency applications. Meanwhile the research about new materials has never stopped, improving the features of promising materials and reaching quality and reliability, necessary for power devices. This study provided the market of semiconductor devices with new

performing devices called Wide Band-Gap (WBG) devices. These new devices are characterized by excellent features, which are superior than the Silicon counterpart, making them fundamental to achieve new performances in all the fields of Power Electronics as presented in [4], [5] and [6]. The name of these devices is due to their values of Band-Gap energy of the semiconductor, requested energy to move the electrons from the Valence band to the Conduction band. The band gaps of these materials are more than three times the energy requested for Silicon. The most famous and spread WBG devices are the following two:

- Devices based on Silicon Carbide (SiC).
- Devices based on Gallium Nitride (GaN).

From the wide Band-Gap energy feature derive many interesting characteristics that make the SiC and GaN devices suitable for several application fields as High Temperature application, high frequency/speed application and high voltage application as reported in [7] and [8] where SiC and GaN devices and their application were reviewed, respectively. In Figure 4 the main features of the WBG and Si devices are listed, to simplify the comparison between them.

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, E_g (eV)	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant, $\varepsilon_r{}^a$	11.9	13.1	9.66	10.1	9	5.5
Electric breakdown field, E_c (kV/cm)	300	400	2,500	2,200	2,000	10,000
Electron mobility, μ_n ($cm^2/V{\cdot}s$)	1,500	8,500	500 80	1,000	1,250	2,200
Hole mobility, μ_p ($cm^2/V{\cdot}s$)	600	400	101	115	850	850
Thermal conductivity, λ (W/cm·K)	1.5	0.46	4.9	4.9	1.3	22
Saturated electron drift velocity, v_{sat} ($\times 10^7$ cm/s)	1	1	2	2	2.2	2.7

Figure 4 – Main features of WBG and Si devices (the picture is taken from [4])

Another interesting feature of WBG materials is the high value of Electric Breakdown field E_c, which is near to seven/eight times the value of Silicon. This value is very important because it influences the vertical structure of the semiconductor chip of the power device (width and doping of Drift region) and related on-resistance (conduction phase). In particular the Width of Drift region W_{BD} can be expressed as:

$$W_{BD} \approx \frac{2*V_{BD}}{E_c} \tag{1.1}$$

where V_{BD} is the breakdown voltage of the power device. From the equation (1.1), it can be noted that the width W_{DB} decreases with the rise of E_c allowing the reduction of the dimensions of power devices. The increase of E_c results also in the increase of the doping of the Drift region. Consequently thanks to the high values of E_c the WBG devices can block the same voltage of Silicon devices but with a reduced width and a larger conductivity or with the same dimensions can be blocked a voltage greater than the Silicon. Instead regarding on-resistance of power device, which is equal to the resistance of Drift region, can be expressed with the following equation for an unipolar device:

$$R_{on} = \frac{4*V_{BD}^2}{\varepsilon*\mu_n*E_c^3} \tag{1.2}$$

Where ε is the dielectric constant and μ_n is the electron mobility. Analysing the equation and remembering the ratio between the values of E_c of WBG and Si, the value of on-resistance of WBG devices is smaller than Silicon (near hundred times). Figure 5 reports the specific on-resistance of several devices based on Si and WBG materials for different values of breakdown voltage, together with the limits of the different materials.

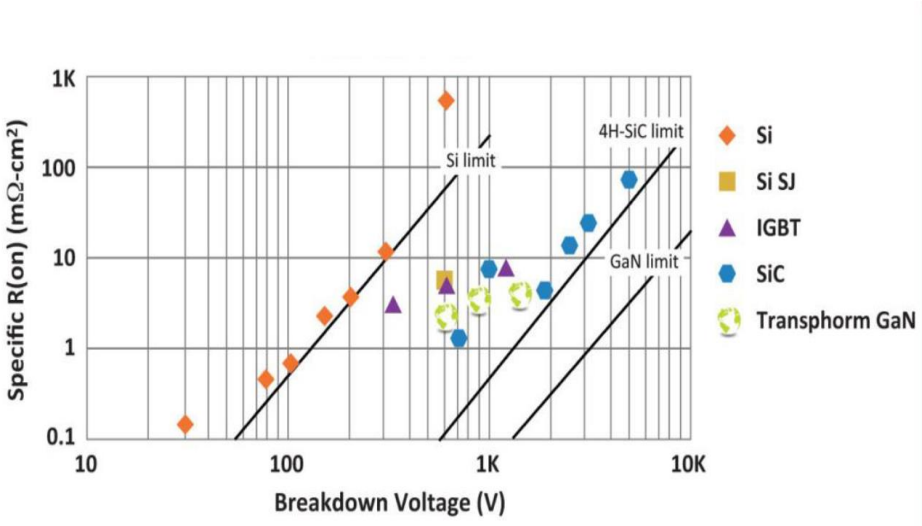

Figure 5 – Specific R_{on} vs breakdown voltage of devices based on Si and WBG, plotted together the limits of the materials (the picture is taken from [9])

From the above figure we can note how the devices based on Silicon have reached the limits of this materials while for the WBG materials there is space to improve them.

To compare the power devices and their main features, the Figures of Merit (FOM), presented by Baliga in [10] and [11] are widely used, since they permit to study in simple way the related switching and conduction characteristics. The reduction of the

dimensions of power devices thanks to the high values of Electrical critical Field reduces the values of parasitic capacitance of devices, especially the input one. The reduction of parasitic capacitance, together the high values of Electron Saturation velocity make the power devices based on WBG materials suitable for applications that requires high switching frequencies as proposed in [12]. The last interesting feature of WBG materials is the Thermal conductivity which especially for the SiC material is almost five times of the Silicon, while for the GaN is almost similar to it. This feature together with the high values of Band-Gap energy of WBG materials, allows the operation of power devices at high operation temperature. Moreover, high values of thermal conductivity provide lower value of thermal resistance between junction and case, which allow the disposal of generated heat to the ambient with small increase of the device junction temperature. To conclude this comparative analysis between the main WBG materials (SiC and GaN) and Silicon, the main features of these three materials are depicted in the spider chart reported in Figure 6.

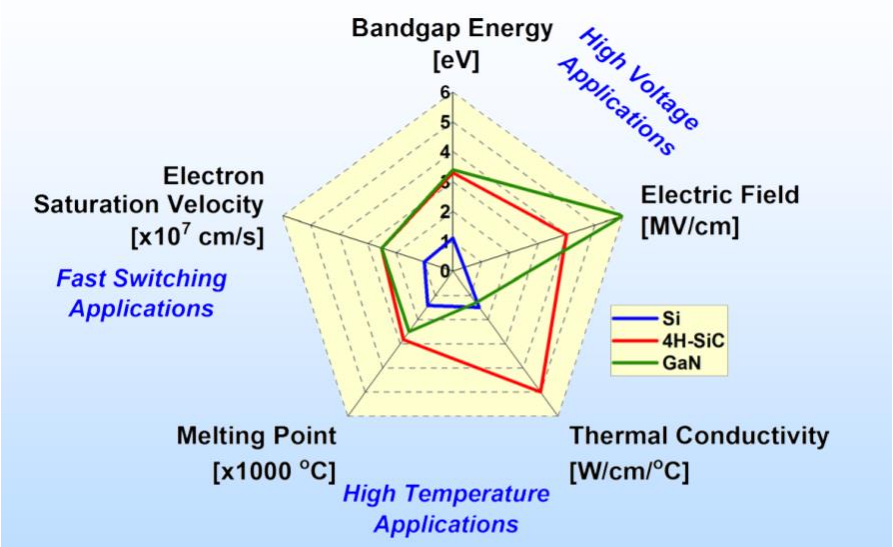

Figure 6 – Graphical comparison of main features of power devices, highlighting the topology of applications (the picture is taken from [13])

Thanks to this particular representation the comparison of these materials is simplified, allowing the classification of the suitable application on the basis of the characteristics of the materials.

The power devices based on WBG materials can be classified according to the operating switching frequency and the value/size of the Breakdown voltage, which are the main features that allow the device choice. For example the SiC devices are characterized by high Breakdown voltage, the entry level size is 650V, and maximum

switching frequencies of hundreads of KiloHertz. Instead the GaN devices are featured by lower Breakdon voltage, from tens of Volts to maximum 650V, and switching frequency that can reach a few MegaHertz. To conclude this analysis about how maximising the efficiency of power converter thanks the WBG devices, in Figure 7 a graph is reported that shows the applications fields of the Wide Band-Gap devices produced by the Infineon company.

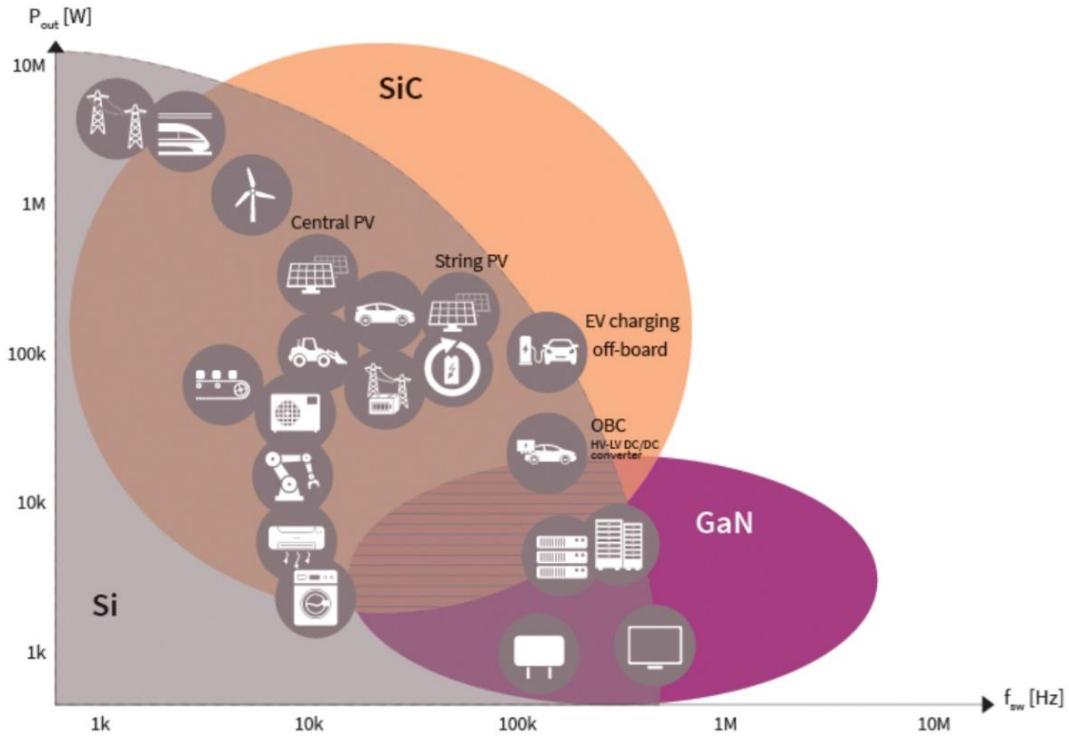

Figure 7 – Infineon Wide Band-Gap devices application (the picture is taken from the Infineon Website [14])

From the figure above it can be observed that the SiC devices as well as the GaN devices are suitable for many applications that just few years ago were exclusively covered by Si devices. Thanks to the interesting features of WBG devices, the boundaries defined by the Silicon's limits have been pushed showing new unexplored and appealing horizons in the field of Power Electronics. An example of this is reported in [15], [16] and [17] where the features of SiC devices and converter based on them are compared with the equivalent in Silicon, showing the superior behaviour of SiC and its better performances.

However to take advantage of the better performances of the WBG devices, as the high switching frequencies and better switching performances, it is absolutely necessary to deal with new challenges as the layout, packaging and EMI problems as

showed in [18] and [19] where these issues are evaluated. In particular, with the increase of the switching frequency, the minimization of parasitic components (principally stray inductances) of the devices and of layout board become a fundamental aspect, especially for the devices based on GaN material. In the case of devices based on Si, the stray inductances due to the device and its package are much lower than the parasitic parameters of the layout. Regarding the devices based on SiC, they require an accurate layout to avoid overshoot voltage and the inductances of the package must be considered in the design. Instead, for GaN devices, the role of these inductances are fundamental since, even if the layout is optimized they can extremely affect the evolution of the characteristics and performances. For this reason the packaging of GaN devices has been revisited to minimize the values of parasitic inductances, especially the Source one, thanks to the developing of new tipology of packages. For example for GaN power switches the traditional TO-247 packaging has quickly been replaced by integrated packages that present very short pin or integrated in the chip. Thanks to the minimization of the length of the pins, a reduction of 10/15 nH of the stray inductance can be reached. Figure 8 reports a comparison between two packages

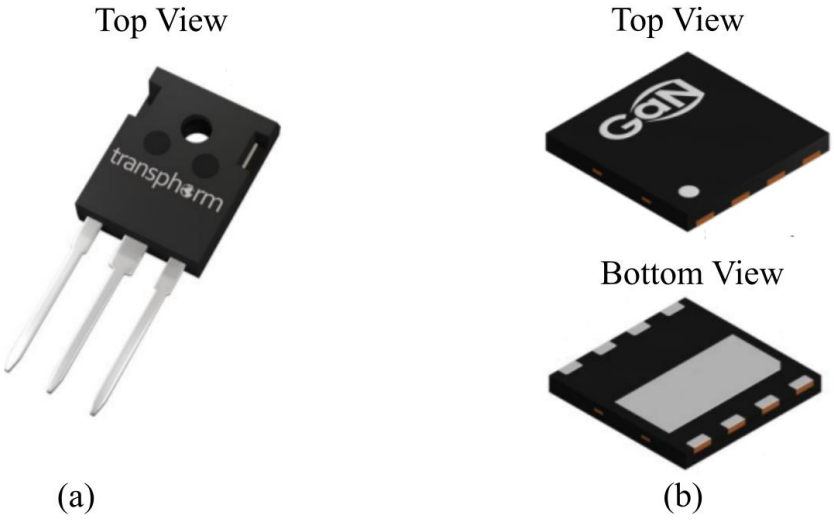

Figure 8 – Comparison of GaN FET TP65H050WSQA in TO-247 package (a), manufactured by Transphorm inc. [20] and E-mode Gan transistor GS-065-030-2-L in 8x8 mm PDFN package (b) manufactured by GaN Systems inc. [21].

for GaN devices, a TO 247 package and PDFN package, featured both by blocking voltage and operation current of 650V and 30A. From the layout point of view, the WBG devices require very short control loop with minimized connection lengths that can be achieved putting the gate driver closer to the power device. The same design

procedure is used to shorten the power loop together with the busbar technique, which is based on forcing the current flow in parallel power planes to minimize the stray inductance of power board. However this technique is featured by the issue of the introduction of parasitic capacitor due to the parallel conduction plane, which have to be taken into account in the design. In particular, this technique has to be avoided for the power planes connected to the power devices and its configuration (i.e power leg). The additional stray capacitors due to the busbar technique increases the output and the reverse recovery capacitors of devices, degrading the switching characteristics of the switch and consequently the related performances. Regarding the EMI problems, the high switching frequency of WBG devices causes a large variation of current and voltage, di/dt and dv/dt, together with the HF ringing of these characteristics due to the parasitic parameters and then the increase of the Electromagnetic interference emissions. The variation of voltage and current of WBG are much higher than the Si devices, requiring much efforts in the design of EMI filter to overcome this problem and avoid the degradation of system performances.

Along with the improvement in the field of power devices technology, the soft-switching technique are another way to reduce the power losses due to the commutations of power devices and enhance the efficiency. The label “soft” is used to highlight the nature of the commutation, in comparison with conventional commutations that are called hard switching. To study the commutations it is usually used the switching locus which is a curve on the current-voltage plane that represents the evolution of electrical characteristics during the commutations. Figure 9 (a) and (b) reports the switching locus for Turn-on and Turn-off in hard switching as well as in soft-switching conditions, respectively.

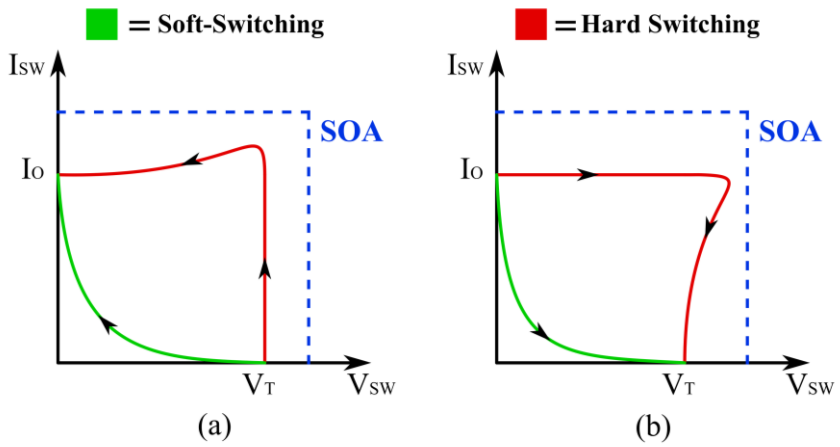

Figure 9 – Switching locus at Turn-on (a) and Turn-off (b) in case of Hard switching and Soft-switching

The aim of soft-switching is to minimize the area of commutations on the I-V plane, obtaining the drastic reduction of the power losses of the power devices. To achieve this aim, the commutations have been featured by one of the following conditions:

- Zero Voltage Switching: The commutations, Turn-on and Turn-off happen when the voltage across the power device is zero. This feature is achieved in many power converter topologies and in particular in Phase Shifted Bridge (PSB) and Series-Parallel Resonant Converter (LLC). In the switching path of the converter, the inductive energy stored in the equivalent inductor has to be large enough to charge and discharge the output capacitors of power switches. Consequently, the voltage across the power device to be to turned-on reaches zero voltage before its driving signal becomes high.
- Zero Current Switching: The generic commutation happens when the current that flows in the power device is zero. This happens at the turn-on of the power switches of PSB and LLC converters, when the antiparallel diode of devices goes in conduction thanks to the resonance on the leg. In this way the current flows in the diodes and the power switch can be turned-on with zero current as well as zero voltage.

1.2.2 Physical dimensions of power converter

The enchantments to the Efficiency conversion due essentially to the new devices based on WBG materials, produce effects on the dimensions (volume) and weight of

power converters. Moreover, the reduction of volume and the increase of efficiency of power converter provide an increase of the power density, which is another important feature of the architectures nowadays [22]. Especially the reduction of power losses allow the reduction of the volume and weight of the power converter, for the following reasons:

- Increase of switching frequency: the rise of the operation frequency of the power converter allows the reduction of the size of the passive component as magnetic components and capacitors. Figure 10 shows the results of two high frequency transformer designs based on switching frequency of 100 kHz and 1 MHz, respectively highlighting their dimensions and weights.

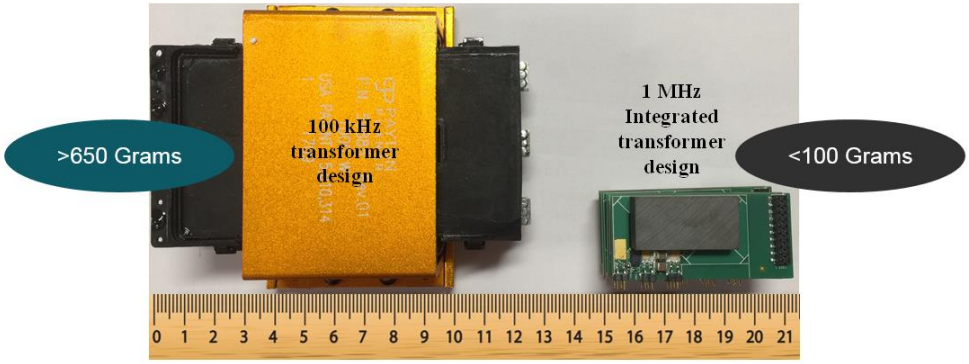

Figure 10 – Example of the reduction of volume and weight of transformer thanks to the increase of operation frequency of 10 times (picture taken from [23])

From the comparison of the above figure, it is very clear how the increase of 10 times of the frequency produce a reduction of the weight of almost six times and a 50% reduction of the section.

Additionally the increase of the frequency can reduce the values of passive components, necessary for power converter as EMI filter and capacitor bus link, since their size are inversely proportional to the switching frequency. In some cases the increase of frequency permits the use of components more reliable and efficient due to a particular technology that are performing for opportune values of the considered passive elements. In the design of power converter the choice of switching frequency is always a trade-off between the power losses and the volume of magnetic components and capacitors. This trade-off is due to the losses, especially the switching losses which are proportional to the switching frequency of the converter according to:

$$P_{Switching} = f_{switching} * \left(E_{on} + E_{off}\right) \quad (1.3)$$

Where E_{on} and E_{off} are the dissipated energies in the turn-on and turn-off of the power devices, respectively. So the switching rises linearly with the frequency, imposing a constraint to the reduction of the volume thanks to the increase of operating frequency. Anyway thanks to the WBG devices and the soft-switching topologies, this constraint is less effective facilitating the design of passive components.

- Reduction of size of heatsink: the cut of power losses allows the simplification of thermal design of the heatsink, providing the reduction of the heatsink volume and in case of forced ventilation the reduction of flow rate, to eliminate the heat generated by the converter. Moreover, in few particular applications the minimization of power losses allows the elimination of the heatsink since it is not necessary for the normal operation of the power converter.

A clear example of the benefit on the volume and weight due to the rise of switching frequency are the planar transformer, which are designed for high values of operation frequency and present very compact form factor. Instead an evident example of power converter with reduced heatsink are all solution based on GaN devices, which allow the achievement of very high value of efficiency and power density with very low and compact heatsink. Figure 11 reports the comparisons between the new Dell laptop charger based on GaN device and two older charger based on the Silicon.

Figure 11 – Comparison of Dell laptop charger 240W in GaN with older charger in Silicon of 90W (a) and 240W (b) (pictures taken from [24]

As observable from the above figure (a), the new 240W charger based on GaN of Dell laptop has similar dimensions of old 90W charger in Silicon but with 2.7 higher

power. Instead from the figure (b) it can be noted that the same charger based on GaN is smaller and lighter of the same power size based on Silicon, as a result of the higher performances of the WBG devices.

To conclude this paragraph, the physical dimensions of power converter and its power density are highly dependent on the efficiency and are interrelated, making complex the optimization of the design. However, as introduced before, the achievements in terms of power devices and topologies are simplifying the process for the researchers.

1.2.3 Reliability

Due to the introduction of more stringent requirements from application fields as automotive, avionic and then other applications, the reliability of power converter has become one of the most studied topic, to achieve the demanded quality as showed in [25] and [26]. To reach the quality target a complete study of each possible failure mechanism of single component of the system and the related failure rate were analysed, to identify the less reliable components used in the power converter. The results of this global study has recognized as the worst components, on the basis of their reliability issues, the capacitors and the power devices. However these latter, in the last years are becoming more reliable thanks to new manufacture technology and the introduction of new materials as Silicon Carbide (SiC). For example, with the SiC devices, high operation temperature can be reached without problems, reducing the influence of the temperature on the features of power devices and its reliability. This feature is due to the improvements of the related packages that, thanks to new materials technology allow to operate the power devices at high temperatures. Consequently, the capacitors have become the bottleneck of the reliability of power converter, as proved in [27], [28] and [29], requiring efforts in the design of architecture to reduce the failures due to them. The capacitors, in particular those one for DC link application, can fail for aspects as temperature, voltage, current, moisture, mechanical stress and material wear-out. The failures can be classified in the following two case on the basis of the topology:

- Sigle-event stress that provide catastrophic event: The failure is due to a single-event that is too stressful for the capacitor, determining its immediate failure.

- Wear-out failure due to long-term degradation: In this case the failure is due to effects that, cumulated in the time produce a slow degradation of the features of the capacitors, until the failure is reached.

For the analysis and prediction of capacitors lifetime the following equation is usually used, which allows the reliability estimation for constant operating conditions:

$$L = L_o * \left(\frac{V}{V_o}\right)^{-n} * e^{\left[\left(\frac{E_a}{k_B}\right)*\left(\frac{1}{T}-\frac{1}{T_o}\right)\right]} \quad (1.3)$$

Where L and L_o are the lifetime for using and testing condition, respectively. Instead V and V_o are the voltage for using and test condition while T and T_o are the temperature in Kelvin for the same cases. E_a is the activation energy, K_B is the Boltzmann's constant while n is the voltage stress exponent. The values of E_a and n depend on the technology and manufacturer of the capacitors.

The capacitors can present the following three failure modes [30], due to different failure mechanism as dielectric loss, self-heating, dielectric breakdown, electrochemical reaction and etc. :

- Open circuit.
- Short-circuit (in some case with a low resistance).
- Electrical parameters (Capacitance, ESR) change due to wear-out.

To conclude this paragraph on the reliability, Figure 12 reports the failure probability of all components and system in a DC/DC converter application.

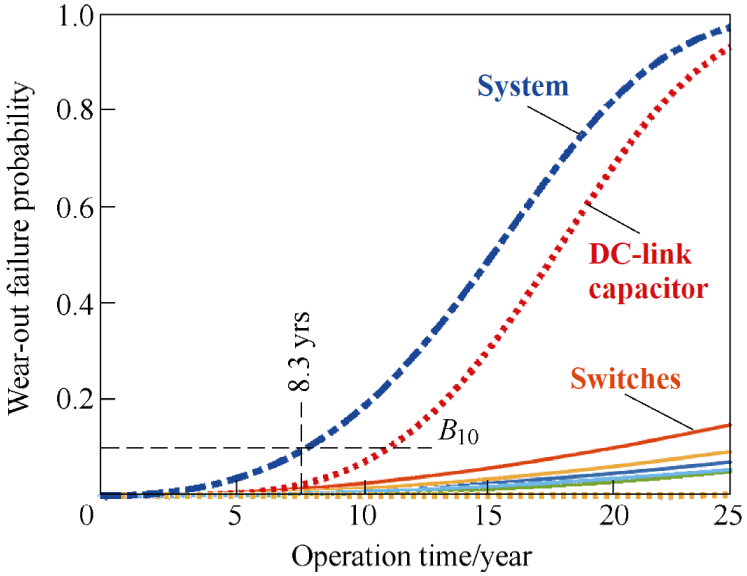

Figure 12 – Failure probability of components and system in a DC/DC converter application (picture is taken from [27]).

From the graph we can note that the DC-link capacitor has the worse failure probability and significantly influences the failure of the overall system.

1.3 Novel topologies for DC/AC insulated application

In the previous paragraphs the common and widespread architecture and modulation technique have been described, also showing how to improve the main features of these architecture. Now to complete this chapter the novel architectures, proposed to achieve better performances and/or reduce the problems of DC/AC insulated solutions, will be briefly introduced and described to complete the scenery of this application field. In particular only the innovations in the topologies, control technique and design have been studied, since replacing Si devices with WBG devices and/or improving the transformer technology can be considered as technological improvements of components.

The innovations of DC/AC insulated converter can be classified in the following two categories according to the nature of novelty:

- Control and design innovations: The aim of these kind of innovations is to reduce the stress of components as DC-link capacitors and power devices, through the use of an optimised design [31] and appropriate control techniques, as presented in [32], [33] and [34]. In this way features as overall reliability and efficiency of system can enhanced without variations on the common architecture used. In particular the main aim of these studies, is the optimisation of the DC-link capacitor to achieve the reduction of the capacitance and consequently use more reliable technologies.
- Topology innovations: Unlike previous category, the aim of these innovations is to enhance the features of power converters through the topological changes of the architecture, which obviously influence the behaviour of the system. Consequently, for the analysis of this solution a different point of view is required, since the differences with common architecture can be important. These new topologies are also oriented to the optimization of the DC-link capacitors but in a different way. Especially they are featured by the absence of these capacitors, which provide a particular and uncommon behaviour of relative voltage, called in literature Pulsating evolution. These novel power converters are called capacitorless to remark the elimination of these huge and bulky capacitors, that are the main responsible of reliability and power density reduction. To achieve the

pulsating evolution of the voltage passive or active resonant circuits can be used, as showed in [35], [36] and [37] where the concept of Resonant DC link converter is introduced. Moreover to provide a pulsating voltage to the Inverter stage a modified power converter can be used to have the requested features. In this way, in addition to the improvement of the reliability, the pulsating evolution can be used to achieve the soft-switching conditions for the inverter stage, with the consequent enhancement of the efficiency and the power density of the proposed architecture.

In conclusion, both the proposed solutions can provide novel and alternative architecture, based on different principles to the DC/AC insulated converter application. However from the standpoints of Power Electronics, the topological innovations are more interesting since they provide new architectures and allow the optimization of different features of the power converter. For these reasons this thesis and the related research are focused on the insulated architecture based on the Pulsating evolution of the voltage, oriented to the auxiliary power supply for railway applications.

CHAPTER 2. PULSATING DC LINK CONVERTER (PDLC)

In the conclusions of the previous chapter, the novel topologies in the DC/AC insulated converter application have been briefly presented, highlighting the inherent capabilities of these solutions and the differences with the traditional solutions. In particular from the research point of view, these novel topologies permit the achievements of the following advantages:

- Answer to the request of improvement of the reliability of the power converter, thanks to the elimination of bulky and large DC-link capacitor.
- Allow the enhancement of the efficiency thanks to the achievements of soft-switching conditions for one or more power stages.
- Provide different solutions for the different application fields that require insulated topology to convert DC source in AC voltages.
- Introduction of new modulation and control techniques for these topologies, based on common or modified techniques, to take advantage of the particular features of these novel architectures.

The architectures featured by Pulsating evolution of the DC link voltage can be classified, according to how the pulsating voltage is generated, in the two following categories:

- Inverter based on resonant DC link: In this solution a resonant circuit is interconnected between the DC source and Inverter stage, to provide the Pulsating evolution to the voltage. The topology of the resonant circuit can be passive or active, according to the desired performances. The passive solution consists in a capacitive-inductive resonant bank and requires a particular modulation technique to achieve the pulsating evolution of voltage. Instead in the active solution, one or more controlled switches are added to the resonant bank to achieve better performances and/or particular operating conditions (clamping the voltage) as proposed in [38], [39] and [40]. Figure 13 reports the schematic of Inverter based on resonant DC link and the evolution of the DC link voltage.

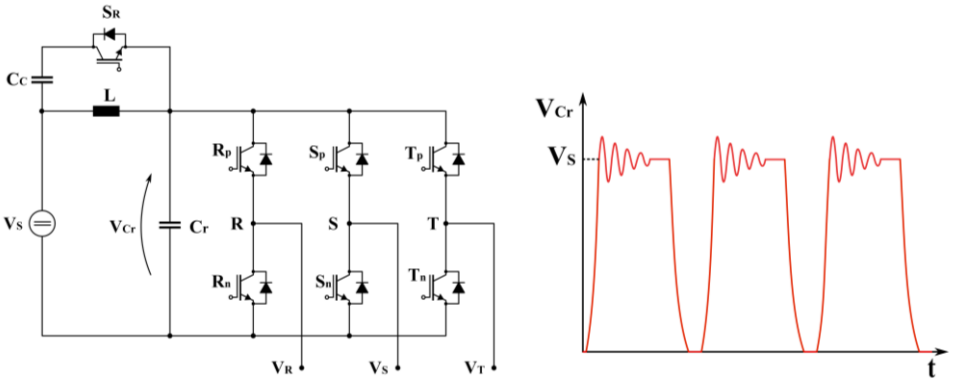

Figure 13 – Schematization of Inverter based on Resonant DC link (left) and pulsating evolution of the V_{Cr} voltage (right)

- Multistage architecture: This solution makes use of the common FDLC architecture, insulated DC/DC converter that feeds the Inverter stage excepts for the change of the first stage to obtain the pulsating evolution of the intermediate DC link. For this reason the architecture based on this principle are renamed Pulsating DC Link Converter (PDLC) to highlight the similarity with the traditional solution.

In Figure 14 the general schematizations of the solution previously described are reported:

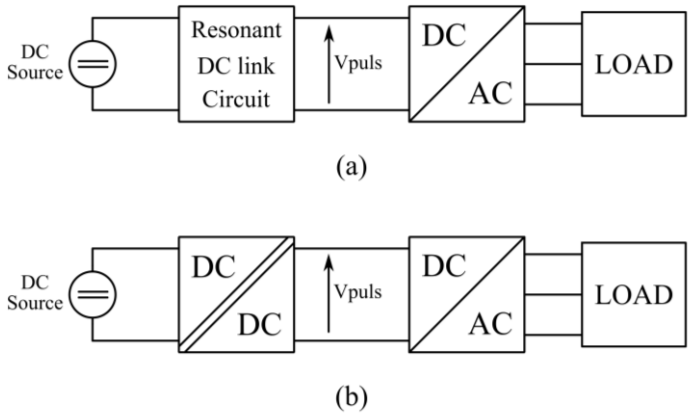

Figure 14 – Schematization of Inverter based on resonant DC link (a) and of multistage architecture PDLC (b)

From the figure above it can be observed that the solutions based on resonant DC link (a) requires another power stage to provide the galvanic isolation, between the DC source and the load. Instead the PDLC architecture (b) presents the same

schematization of the FDLC (see Figure 1) excepts for the absence of the DC-link capacitor.

The architecture based on the resonant DC link and the different solution for the resonant circuit have the following problems:

- As said before, this solution is not suitable for insulated DC/AC converter application due to the absence of galvanic isolation unless an insulated DC/DC converter is connected between the source and the resonant circuit. However this configuration degrades the overall reliability due to the necessity of large and bulky capacitor to stabilise the DC voltage.
- This architecture and in particular the resonance phenomena, necessary to achieve the pulsating voltage can be influenced by the parasitic parameters of the system, degrading the performances of the solution.

For these reasons and for the better performances achievable thanks to the multistage architecture, the core of this thesis is focalized on the complete study of all aspects of Pulsating DC Link Converter (PDLC) which is an evolution of the above architectures.

2.1 Pulsating DC link Converter (PDLC)

The multistage architectures based on Pulsating DC link principle are usually realised with two power stages connected in cascade as showed in [41] and [42], where two different versions of this topology are presented. The first stage is an insulated DC/DC converter, reviewed to provide a pulsating output voltage which is used to feed a two level Voltage Source Inverter (VSI), the most common solution for the second stage. Moreover the topology used for the first stage depends on the power level of the application and the desired performances.

Figure 15 reports the schematic of the proposed Pulsating DC Link Converter (PDLC), presented in [43], highlighting the different power stages that implement it.

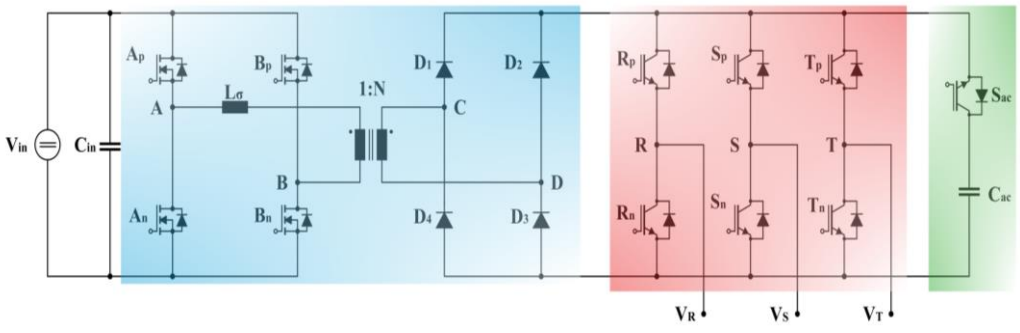

Figure 15 – Schematization of proposed Pulsating DC Link Converter (PDLC)

The proposed version of PDLC is made up of a Phase Shifted Full Bridge (PSB) featured by the absence of low-pass output filter and a two level Voltage Source Inverter through a Pulsating DC link voltage. The system includes an Active Clamp circuit which is necessary to clamp the overshoot voltage due to the resonance phenomena of PSB stage, as showed in [44] and [45]. The energy associated with the overshoots is stored in the capacitor C_{ac} and is supplied to the VSI stage, during the subsequent powering phases of PSB. In this way the energy related to the unavoidable resonance phenomena of the first stage is not wasted but is recovered to feed the VSI stage, improving the efficiency of the power converter. Thanks to the Pulsating DC link principle and this configuration, the proposed PDLC is featured by the following interesting characteristics:

- Increase of overall reliability thanks to the absence of the output filter of the PSB stage and especially of the large and less reliable DC-link capacitor which is, as anticipated previously, the bottleneck of the reliability of power converter.
- Improvement of the dynamic response of converter due to the absence of large and bulky components of the output filter of the PSB stage. This absence avoids the presence of large time constants which slows down the dynamic response of the converter especially during the converter transient and the start-up.
- Capability to achieve Zero Voltage Switching (ZVS) conditions for all the VSI switches exploiting the zero portions of pulsating DC link voltage. To achieve this aim it is necessary to use an appropriate modulation technique based on the synchronization of the operation of the two power stages. In this way the zero voltage portions of Pulsating DC link are distributed along the period, controlled by the operation of PSB stage, in correspondence of the commutations of the Inverter stage.
- Thanks to the elimination of the output filter of the PSB stage, which is usually implemented with bulky components and the reduction of power losses due to ZVS of the VSI stage, the weight and volume of the converter are reduced. Consequently the power density of this solution is increased thanks to the reduction of the size of heatsink and passive elements and, at the same time, the efficiency is increased.
- Limit the voltage overshoots on the Pulsating DC link due to the resonance phenomena of the first stage thanks to the Active Clamp circuit. This latter

allows the elimination of the voltage spikes and also permits the reuse of the energy associated to supply the Inverter stage and enhances the performances of PDLC. The role of the Active Clamp in the proposed topology is fundamental as presented in [46], where the interactions with the other power stages are analysed.

The evolution of Pulsating DC link voltage is represented In Figure 16, highlighting the zero portions for the commutations of the VSI stage:

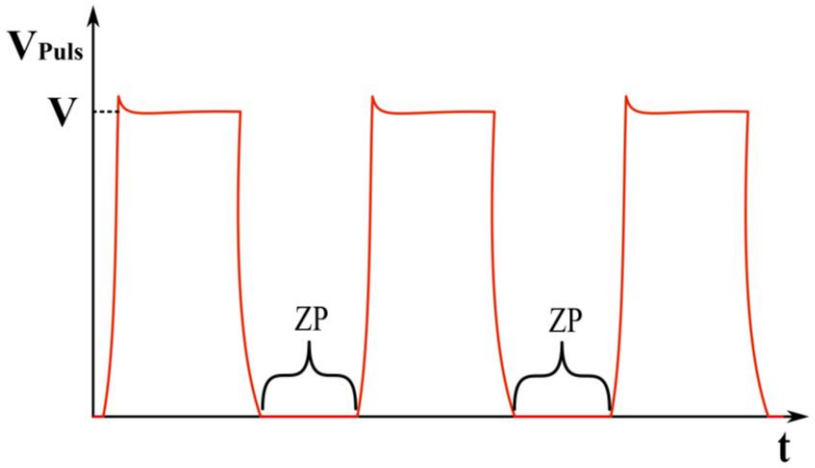

Figure 16 – Pulsating DC link voltage with the Zero Portions (ZP)

2.2 Comparison behaviour of VSI stage of PDLC with common 2 level and 3 level VSI

The VSI stage of PDLC architecture is featured by uncommon properties for a two level solution, due essentially to the Pulsating evolution of the voltage that is used to feed it. In particular the zero portions of pulsating DC link affect the evolution of the output voltages of VSI stage, requiring an accurate analysis of this latter to improve the quality at the output voltage. For this reason, in this paragraph, the inverter stage of PDLC is compared with a traditional two Level VSI stage and a three level T-Type solution, to analyse and show the differences between these solutions. To simplify the analysis, just one leg of the three phase VSI power stages and its operation are studied being it enough to perform the comparison between the output voltage in the different cases. The schematizations for each solution are represented in Figure 17:

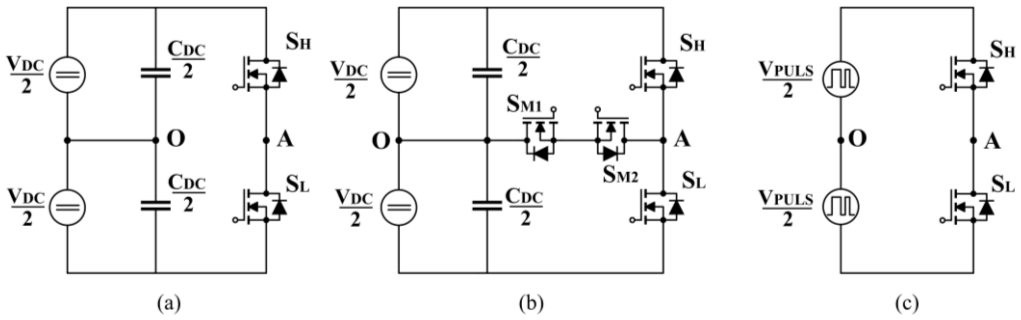

Figure 17 – Schematization of single leg of two Level VSI stage (a), three Level T-Type VSI (b) and of Pulsating VSI stage (c)

Observing the figure above it can be noted that the source of all solutions, DC for the topologies (a) and (b) and Pulsating for (c), are represented as two voltage generators connected to the common node O. Moreover in the two solutions based on Fixed DC link voltage, two capacitors are requested to ensure the symmetry of the voltages and avoid unbalance, which could affect the output voltages of the VSI stage. Instead the solution based on Pulsating DC link principle doesn't need the capacitors and practically can be implemented using a transformer with double secondary winding connected to two output rectifiers. These latter have to be connected in series to guarantee the requested voltage, allowing the simplification of the transformer design. This representation based on split voltage sourced of the input sources is widely used in the literature to examine the operation of VSI stage, using the common node O as the reference for all the voltages. To guarantee a correct comparison, all the legs of VSI stage are modulated with the same modulation technique, the sinusoidal PWM (SPWM). Specifically the parameters used for the SPWM are the following:

- The amplitude of modulating signal is less than the carrier signal, to avoid the nonlinear operating region of VSI stage and all the connected issues.
- The frequency of carrier signal is greater than the modulating signal, to shift all the harmonic components to high frequency;

Regarding the modulation technique used for the T-Type VSI solution it is necessary to provide more details about the control of the four power switches that implement the leg. To obtain the positive level on the output it is necessary to turn-on the high side switch S_H, instead for the negative level it is necessary turn-on the low side switch S_L while for the zero level both the middle switches have to turn-on (S_{M1} and S_{M2}). Practically to simplify the modulation of T-Type VSI, the switching states

reported in Table 1 are used, achieving a technique that is independent of the current direction.

Table 1 Switching states of three level Ttype VSI stage

State	Vpole	S_H	S_{M1}	S_{M2}	S_L
DC+	**+V_{DC}/2**	**on**	**on**	**off**	**off**
0	**0**	**off**	**on**	**on**	**off**
DC-	**-V_{DC}/2**	**off**	**off**	**on**	**on**

Moreover, the direct transitions from DC+ to DC- and vice versa are prevented because they produce additional power losses in the antiparallel power diodes of the middle switches as reported in [47], where the T-Type Inverter is analysed. To conclude this modulation technique is equivalent to the technique used for the three-level Neutral Point Clamped (NPC) VSI topology. To simplify the comparison, Figure 18, Figure 19 and Figure 20 report the signals used for the SPWM and the pole voltages for the three solutions, respectively.

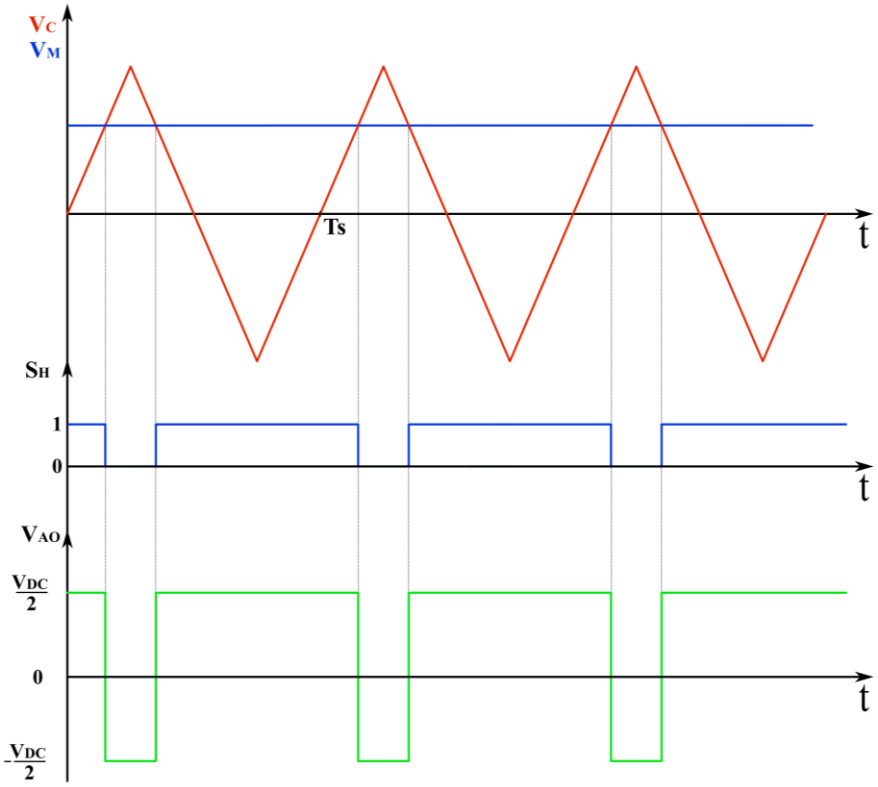

Figure 18 – Modulating and carrier signals (top), driving signal of high side switch(middle) and pole voltage of two-level VSI stage

Due to the high frequency ratio between the carrier and the modulating signals, just few periods of carrier are represented in the graphs to make operations easier to understand. Moreover in this reduced time interval, the evolution of modulating signal can be considered constant since it is slower than the carrier (50/60 Hz versus tens of kHz). In the case of the three-level T-Type VSI solution, see Figure 19, two portions of the evolution of different signals have been highlighted instead of one as for the other solutions. This action was strictly necessary to allow the visualization of all three levels of T-Type VSI in the same graph, without representing the complete period of modulating signals. In this way the loss of details of switching events, that could happen if we visualized the entire evolution of modulating signal is avoided, ensuring the correct analysis of the figure.

Analysing the pole voltage between the nodes A and O of Figure 18, we can observe that the voltage swells between the values $\pm\frac{V_{DC}}{2}$ according of the switching state of the analysed leg.

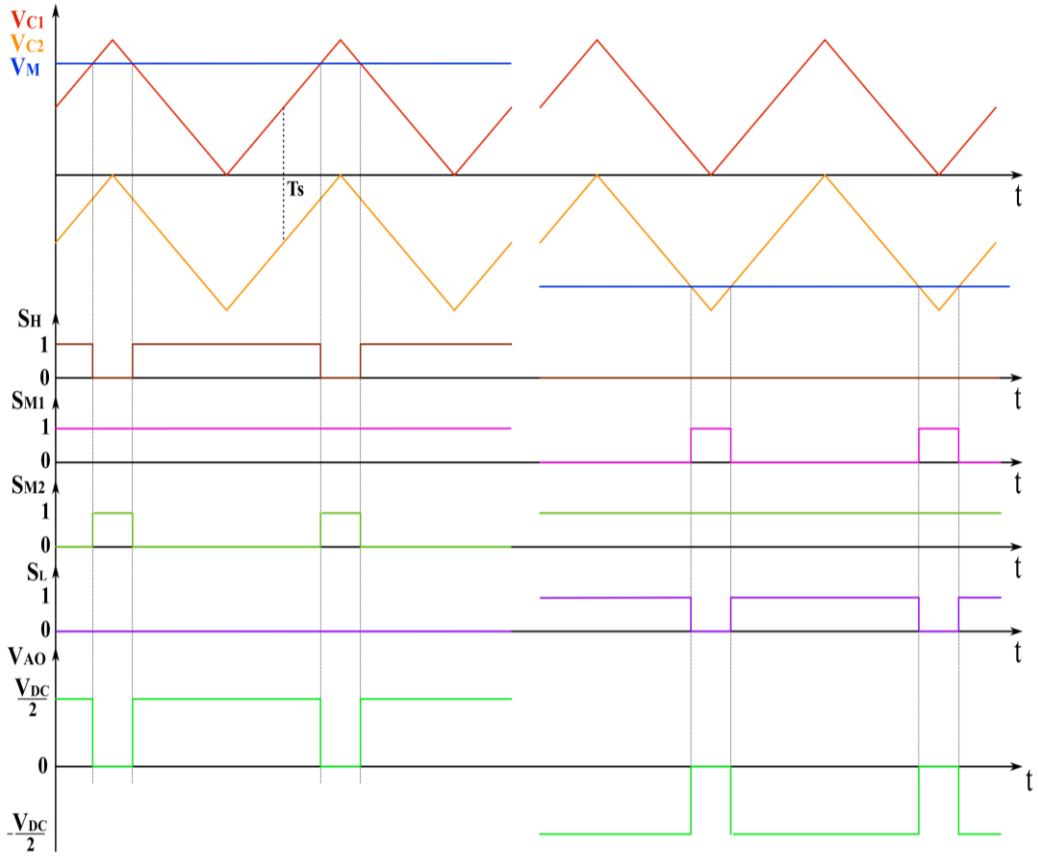

Figure 19 – Modulating and carrier signals (top), driving signals of leg switches(middle) and pole voltage of three-level Ttype VSI stage

Instead in the case of three level T-Type VSI the pole voltage has the additional zero level, which is distributed to improve the quality of the pole voltage. As Figure 19 shows, the zero level is always interleaved with one of the other two levels to avoid the direct transition between the other two voltage levels and consequently reduce the power losses. The behaviour of the pole voltage of the PDLC VSI stage is similar to the traditional VSI (see Figure 20), except for zero portions of Pulsating DC link which are also present on the output voltage.

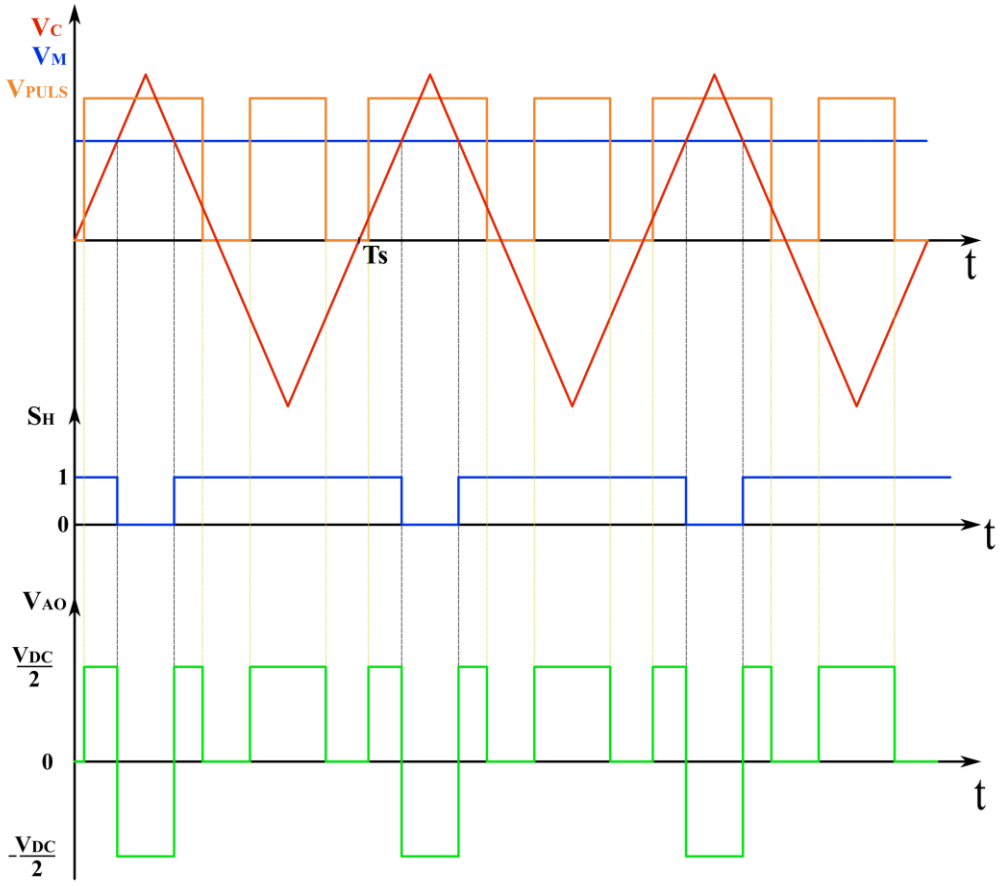

Figure 20 – Modulating, carrier signals and Pulsating DC link voltage (top), driving signal of high side switch(middle) and pole voltage of two-level VSI stage based on Pulsating DC link principle

Consequently the evolution of pole voltage is affected by the Zero portions, which are displaced along the period as function of the phase shift between the SPWM signals (carrier signal) and the pulsating DC link. So thanks to the introduction of ZP the pole voltage gains a third level (zero), as the T-Type VSI solution, without adding any power devices to the traditional configuration of two-level VSI leg. These third level

of Pulsating VSI stage is completely different from the one of three-level VSI solution for the following main reasons:

- It is provided and controlled by the first stage: In a three-level and more in general in the multilevel architecture, the additional levels are controlled and defined by the Inverter topology. Instead in the case of two-level pulsating VSI the third level is defined by the Zero portions of Pulsating DC link and particularly through the modulation technique used for the first stage. Varying the control parameters of the modulation technique, the width and the position of Zero portions can be modified to control the shape of the pole voltage. Therefore the additional level is achieved without using complex topologies, just requiring an appropriate modulation and control of the stage that provides the input voltage of VSI stage.
- Common to all legs: Due to the particular way of providing the additional level, this latter is common to all legs of pulsating VSI stage instead of being particularized for each leg as in traditional multilevel VSI. So we can see this additional level as homopolar component, that has to be distributed in right way to minimize the negative effects on the output voltages and achieve better performances of converter.

Comparing the pole voltages of the two level Pulsating VSI and three level T-Type VSI, we can observe that even if both are characterized by three level only the latter one permits the optimised distribution of them with traditional technique as the SPWM. This result is essentially due to the capability of traditional multilevel to control the distribution of the different levels through the modulation technique, as visible in Figure 19. Instead in the case of pulsating VSI, the further level is independent of the modulation technique and it is only controllable through the distribution of the Zero portions of the pulsating DC link. For this reason the modulation technique of the VSI stage has to take into account the evolution of the pulsating DC link and the position of ZP, to optimise the performances of the overall system. In particular the modulation techniques of the VSI stage and the first stage, which provides the pulsating DC link, has to be synchronized and designed to overcome the problem of absence of the control of the further level. The origin of this particular third level and the necessity to control it, are the consequences of the elimination of the capacitor from the intermediate DC link of multistage DC/AC converter. Without this capacitor, that was necessary to decouple the dynamics of power stages and permitted to use independent modulation techniques, the PDLC architecture requires an appropriate modulation technique to face the coupling between

the power stages. To conclude this paragraph we can say that the traditional modulation techniques cannot be used to control Pulsating DC link, due to their particular features, to achieve the same performances of the other topologies. For this reason the PDLC requires new and innovative modulation techniques to exploit the interesting features of this topology and compete with the other mature architectures. In particular overall and complex modulation techniques based on the synchronization of the power stages are required to control this innovative topology and take advantages.

2.3 Analysis of the origin of voltage oscillations across diodes in Pulsating PSB

As introduced previously, the first stage of PDLC is affected by undesired overshoot on the Pulsating DC link voltage, requiring passive or active solutions to limit this phenomenon. The overvoltage can reach very high amplitude, which can destroy the power diodes of the PSB rectifier due to excessive voltage that can overcome the SOA limits. During every energising phase of the stage, the input voltage is applied with alternate sign, to the medium frequency transformer providing the energy to the load. In these phases the power converter can be approximated as inductive-capacitive circuit, which is subjected to a voltage step with the amplitude equal to the input voltage. We are interested in the evolution of output voltage. Consequently, the output voltage can be analysed as the step response of a second order system, which is featured by voltage oscillations that can reach twice the input voltage, before damping to steady state value. To study this phenomenon and the main influence parameters, the circuit of Pulsating PSB reported in Figure 21 will be used.

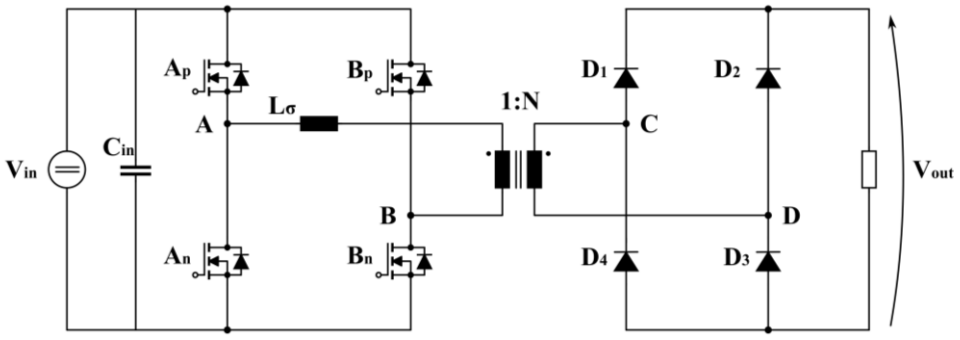

Figure 21 – Schematic of Pulsating Phase Shifted Bridge (PSB)

Before describing the power converter in the energizing phase, it is necessary to express the following considerations about the main components:

- During the conduction phase, the MOSFETs and power diodes will be modelled with their On-resistance. This simplification is appropriate for the MOSFET while for the power diodes it is valid only if we neglect the related Threshold voltage.
- In the interdiction/blocking phases, MOSFETs and power diodes will be modelled by their output capacitance C_{OSS}.
- For the medium frequency transformer, the model and all the considerations presented in [48] are applied to our analysis. In particular the self-capacitance effects of primary and secondary winding and the mutual capacitance effect between the windings, are modelled in the transformer equivalent circuit.

According to these observations and considering the energizing phase, where switches A_P-B_N are conducting, the equivalent circuit of the converter during energising phase of Figure 22 can be achieved.

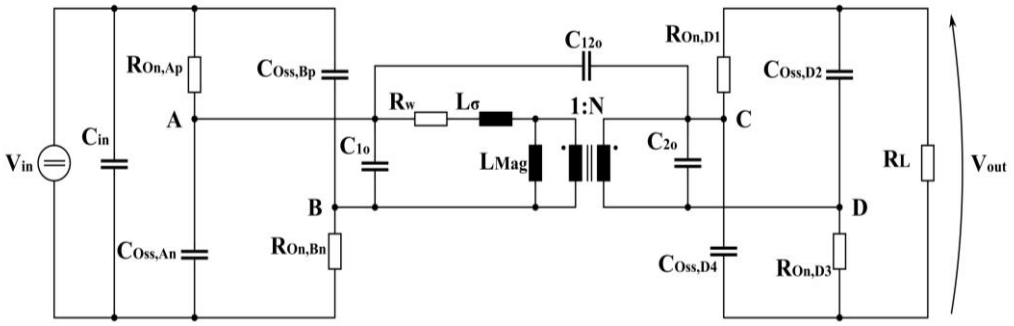

Figure 22 – Equivalent schematic of the Pulsating PSB during energizing phase

The resistive components of the equivalent circuit are very low and can be neglected since they give a marginal contribution to the analysis of the circuit and its oscillations. Moreover, also the mutual capacitance C_{12o} can be neglected. Indeed if we apply the Kirchhoff current law to a cutting surface including all the primary transformer parameters it is featured by zero net current. Consequently we can neglect he mutual capacitance and simplify the equivalent circuit of the transformer. So neglecting all the resistive components of the circuit and referring all the components to the primary side, the simplified equivalent circuit of Figure 23 can be obtained,

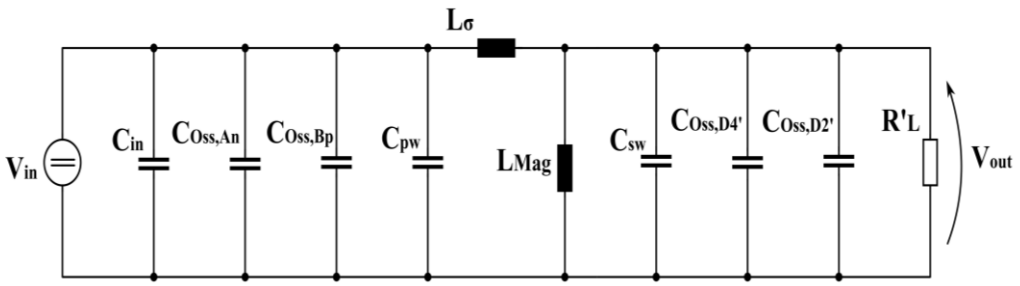

Figure 23 – Equivalent simplified schematization of the converter with all the secondary components referred at the primary

where the capacitors C_{PW} and C_{SW} include C_{1o} and C_{2o} on the basis of the following relationships:

$$\begin{cases} C_{PW} = C_{1o} \\ C_{SW} = N^2 * C_{2o} \end{cases} \quad (2.1)$$

Another simplification of the circuit is based on the observation that in medium/ high frequency transformer the value of leakage inductance is much smaller than magnetizing inductance, with negligible voltage drop across it. Consequently the capacitors C_{PW} and C_{SW} can be considered in parallel and the capacitive effects of transformer can be modelled through a lumped capacitor. This capacitor, named $C_{stray}$is equals to the sum of the two capacitors and is connected at the primary side . In Figure 24 the new equivalent simplified circuit is showed:

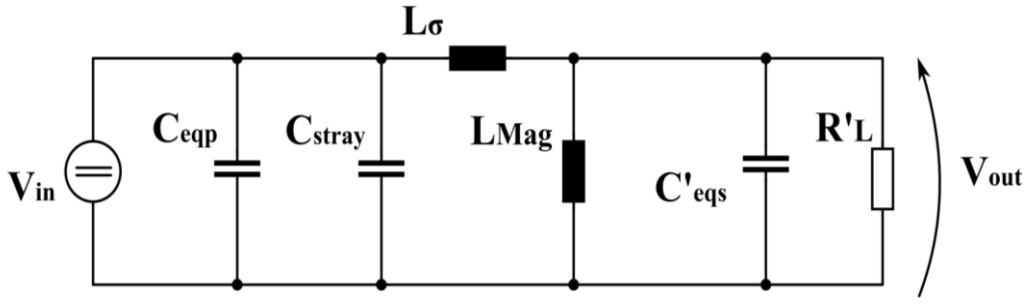

Figure 24 – Equivalent circuit after the simplification above medium frequency transformer model

The capacitor C_{eqp} is the equivalent capacitor of the primary side while C'_{eqs} is the equivalent capacitor of the secondary side, referred to the primary side. In particular these two capacitors can be calculated as:

$$\begin{cases} C_{eqp} = C_{in} \,//\, C_{OSS,An} \,//\, C_{OSS,Bp} \cong C_{IN} \\ C'_{eqs} = C_{OSS,D2} \,//C_{OSS,D4} = C_{OSS,D2} + C_{OSS,D4} \end{cases} \quad (2.2)$$

The capacitor C_{eqp} goes in parallel to capacitor C_{stray}, which is smaller than this latter and can be approximated with the input capacitor C_{in}. So the result of the parallel of capacitors is the capacitor C_{in}. Studying the circuit with this latter modification we can observe that the capacitor C_{in} is in parallel to the power supply and gives zero variations. Consequently the circuit becomes a parallel of leakage inductance, magnetising inductance and the equivalent capacitor of the secondary side, referred to the primary. Since the ratio between the two inductances is very high for a medium/high frequency transformer, we can neglect the magnetising one and obtain a simple LC circuit. Figure 25 reports the simplified circuit, necessary to study the step response of power converter during the energising phase:

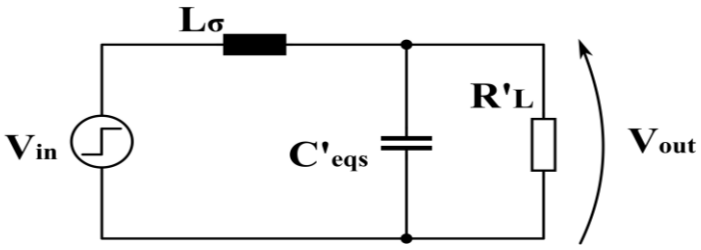

Figure 25 – Final equivalent circuit used to study the step response of the converter during energising phase

Applying a step voltage with amplitude V_S to the equivalent final circuit, the output voltage evolves as showed in Figure 26:

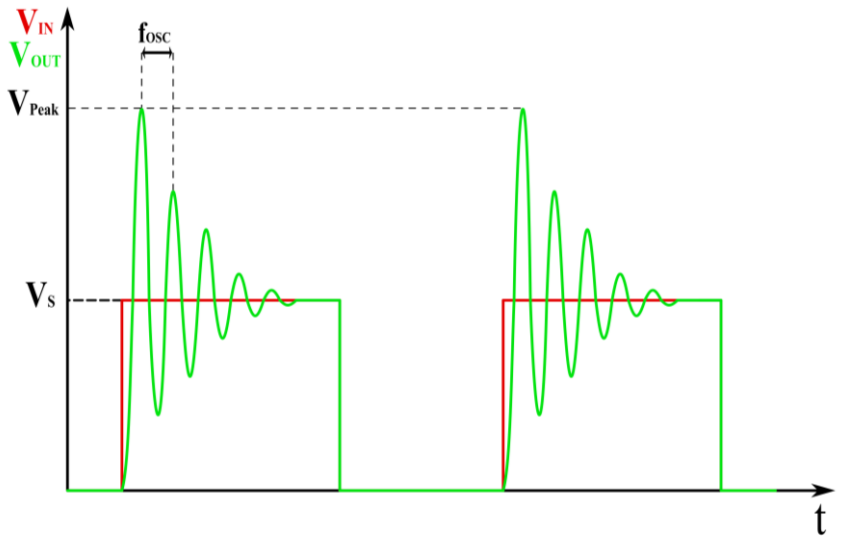

Figure 26 – Evolution of the output voltage obtained

From the figure we can be observe that the voltage is affected by the initial peak of almost two times V_S. The amplitude of subsequent oscillations decreases until the steady state value is reached. The oscillation is characterized by oscillation frequency f_{OSC} that can be estimated as:

$$f_{osc} = \frac{1}{2\pi * \sqrt{L_\sigma * C'_{SE}}} \tag{2.3}$$

Due to the very low value of leakage inductance and the equivalent capacitor of the secondary side, which is essentially the parallel of the output capacitor of two power diode, the oscillation frequency is in the Megahertz range. Besides the possibility of causing the failure of the power diodes due to an excessive overvoltage, the oscillations can give EMI problems to the power converter and especially to the communication and control circuits. Moreover, the voltage spikes give problems to the normal operation of the Inverters stage. For these reasons it is necessary to add a particular circuit to the power stage of the pulsating PSB which helps to limit the amplitude of the voltage oscillations. Another solution to solve the overshoot problem is to modify the topology of the PSB adding clamping power diodes or inductor and/or changing the configuration of medium frequency transformer, as reported in the papers [49], [50] and [51]. In this paragraph, these latter solutions are not investigated for brevity, due to their complexity and impact on the behaviour of the converter. Therefore the solution based on adding another circuit have been investigated, which can be essentially classified in the following way:

- RC Snubber: This solution consists in adding a series of capacitor and resistor in parallel to each power diode of the rectifier stage. The capacitor is used to reduce and control the peak of overvoltage while the resistor is necessary to dissipate the energy associated to the reduction of the overvoltage. Consequently the nature of this solution is passive and it is strongly necessary to find a trade-off between the reduction of overshoot and the power dissipated by the resistor.
- Active Clamp circuit: Instead this solution is active and consists of a capacitor in series to a power switch with the anti-parallel diode, whose anode is connected to the rectifier stage of PSB. In practice the power diode clamps the overvoltage due to the phenomenon previously described and store the associated energy in the capacitor, also called Clamp capacitor. Thanks to the power switch, this energy can be returned to the pulsating DC link to supply the load and improve the efficiency. Consequently, this

solution is more performing than the RC Snubber but is more complex and requires a control section.

In the two following subparagraphs the operations of the two solutions are described and then their features are compared, to highlight their advantages and disadvantages with the aim to define the best solution the PDLC topology.

2.3.1 RC Snubber

As said before, the RC snubber is a simple and low-cost passive solution to reduce the overshoot voltage across the power diodes, with the aim of avoiding excessive and dangerous overvoltage that can destroy the devices. To study the effects of RC snubber on the overvoltage, we use the equivalent circuit of Figure 25, which shows the cause of this phenomena and the influence parameters. If we analyse its frequency response, we can see that it is characterized by a lightly undamped response of second order low pass filter as visible in Figure 27, where an example of the frequency response is plotted. In particular the output assumes a very high value around the oscillation frequency, due to a reduced damping effect of circuit components.

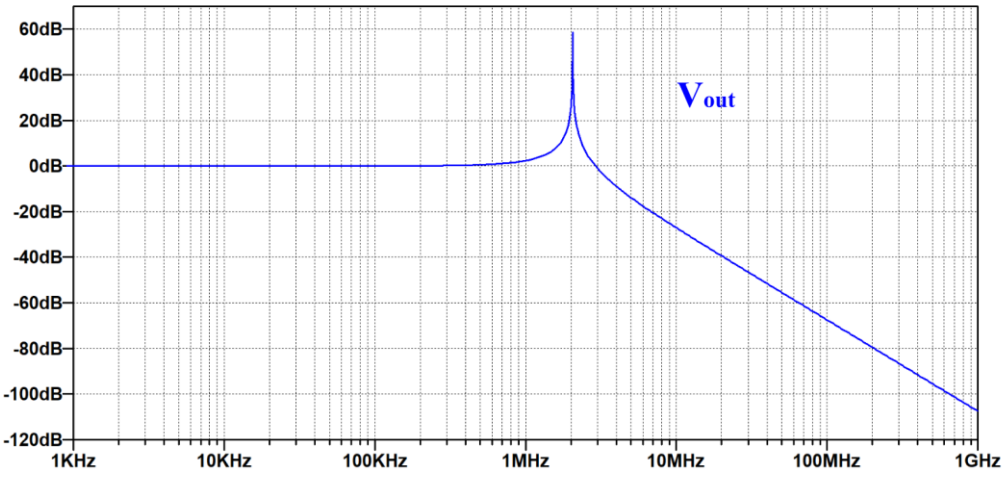

Figure 27 – Frequency analysis of simplified equivalent circuit of converter during energising phase

Adding a RC snubber in parallel to the circuit, with opportune values of resistor and capacitor, induces a reduction of the peak of the frequency response. So optimising the combination of the Snubber values, it is possible to minimize the overshoot. In Figure 28 the damped frequency response is compared with the undamped one, to show the effectiveness of the analysed solution.

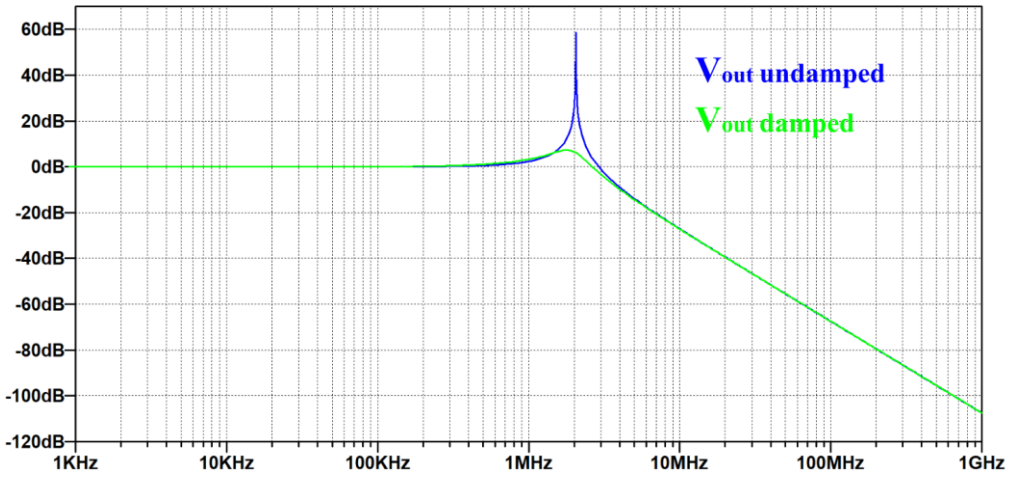

Figure 28 – Comparison of frequency analysis results of simplified equivalent circuit without (blue) and with (green) dumping network

As observable in the figure, the use of RC Snubber in parallel produces a decrease of the oscillation frequency due essentially to the introduction of another capacitor in the transfer function of the circuit. An easy and performing design procedure for power diode RC Snubber is provided in [52] and is used in this paragraph to describe all the aspects of this solution for the overvoltage. Figure 29 reports the simplified schematic of PDLC topology that highlights the first stage and in particular the RC snubber for each diode of the rectifier.

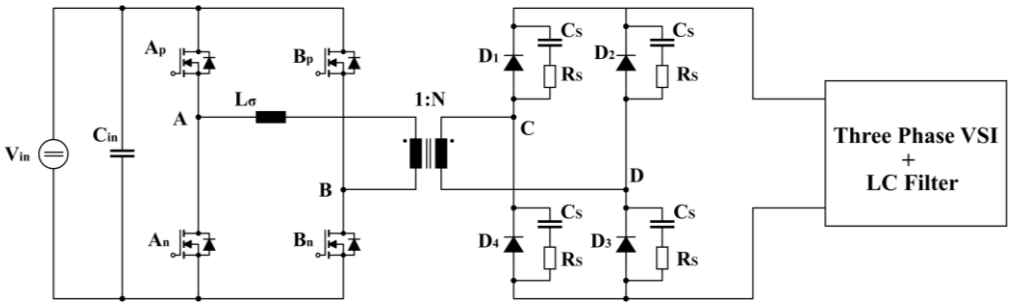

Figure 29 – Schematization of PDLC topology with RC snubbers on the output rectifier of the first stage

For completeness we have to design RC snubber considering all the parameters at the secondary side of the medium frequency transformer since the secondary voltage is the input of the resonant circuit, found before. Moreover in this way the turn ratio of the transformer is taken into account, it influences the peak of the overshoot voltage, especially in the cases where it is requested a secondary voltage higher than the primary one. This procedure helps to define the initial values for the RC Snubber,

which are used as input for the simulations. The value of the Snubber capacitor C_S has to be 3 to 10 times the value of C_{OSS} of the power diode while the value of R_S is related to the characteristic impedance of the circuit which is given by:

$$Z_O = \sqrt{\frac{L_\sigma}{Cs}} \tag{2.4}$$

Once the value of Z_O is found, R_S has to be chosen in the range between 1.5 and 2 times the value of this impedance Zo on the basis of the desired performances. With these two values the simulations are performed and the results will be used to improve the design. In particular the design is continued according to the following considerations:

- The peak of overvoltage can be minimized increasing the value of the Snubber capacitor as visible in Figure 30, where the effects on the output voltage of different values of Snubber capacitor are plotted on the same graph.
- The increase of C_S causes the increase of the power dissipated on the resistor R_S since they are due to the charge and discharge of the capacitance at every switching period, as stated in the following relationship:

$$P_{losses} = C_S * f_s * V_S^2 \tag{2.5}$$

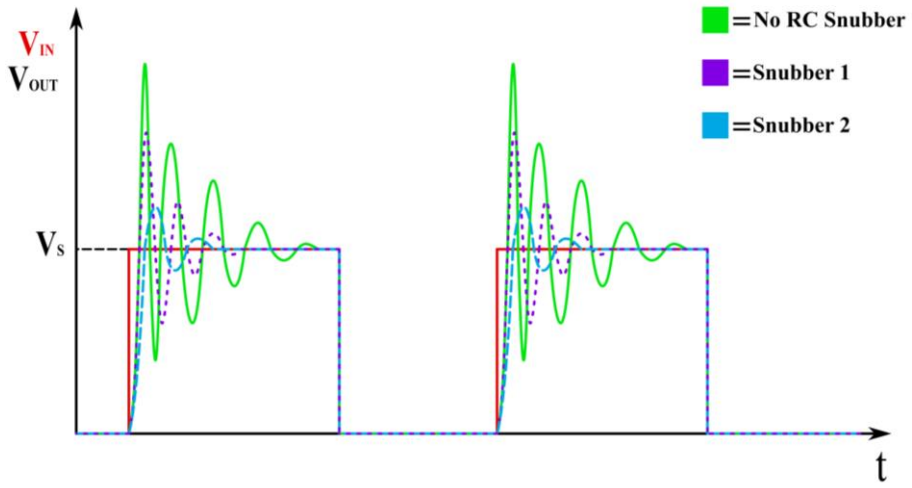

Figure 30 - Effects on the output voltage of different values of Snubber capacitor

Consequently it is necessary to find a trade-off of the value of Snubber capacitor which allows the reduction of overvoltage across the diode without excessive reduction of the power converter efficiency. To conclude, the RC snubber solution is usually designed in the worst case, to reduce the overshoot within the limits of the

SOA of power diodes, without exaggerating with the power losses. Moreover, the necessity to dissipate the energy associated with the resonance, makes this solution unsuitable for high power and high voltage applications, due to the high effects on the overall efficiency.

2.3.2 Active Clamp circuit

The previous solution is affected by an undesired energy dissipation on the Snubber resistor, related to the reduction of the voltage overshoot, that limits the achievable performances of this circuit. Instead the Active Clamp solution, [53] and [54], is based on performing operating principle which allows the overvoltage limitation without impacting on the converter efficiency. The operating principle is based on clamping the overvoltage and storing the associated energy in a reactive component, instead of dumping the resonant response of the circuit. To achieve this feature a simple circuit is used. It is composed of a power switch, an antiparallel diode and a Clamp capacitor. The power switch is connected to the output of diode rectifier in such way that the diode can go in conduction at the occurrence of the overvoltage overshoot on the DC bus. In this way the diode clamps the overvoltage and creates a unidirectional current path from the PSB stage to the Clamp capacitor. Thanks to this path the energy due to the overvoltage is accumulated in the capacitor, instead of being wasted as it happens in the passive solution. To reuse the energy accumulated in the Clamp capacitor, the role of the power switch is fundamental since during its conduction the capacitor is connected to the rails of the output rectifier. Thus the stored energy is added to the energy supplied by the PSB stage to the load, reducing the power losses and increasing the overall efficiency.

The just described operation requires the synchronization between the modulation of the first stage and the control of the power switches of the Active Clamp, to allow the reuse of the stored energy. Specifically, the turn-on and turn-off of this power switch has to be synchronized with the energising phase of the PSB, to permit to supply the load with the energy stored in the capacitor. Consequently this solution is featured by the following two operation phases:

- Passive: phase where the power diode goes in conduction, clamping the voltage overshoot and charging the clamp capacitor with charge dependent on the switched current. The energy stored in the Clamp capacitor can be expressed with the following expression:

$$E_{Cac} = \frac{1}{2} * C_{ac} * \left(V_{P,OV} - V_{SS}\right)^2 \tag{2.6}$$

Where $V_{P,OV}$ and V_{SS} are, respectively the peak of the overvoltage and the voltage at the steady state of the DC link. The energy, considered in this phase, is the inductive energy associated to the leakage inductance of the transformer. In particular in terms of power flow, this energy flows from the output of PSB stage to the Clamp capacitor. This passive operation of Active Clamp can also be called Clamping phase and/or charging phase due these characteristics.

- Active phase where the power switch is turned-on, creating a bidirectional path between the output of PSB stage (Pulsating DC link) and the Clamp capacitor. This path is used to give, the energy stored in the capacitor during the previous passive phase, back to the system. Consequently analysing the system from the energy point of view, the power flow in this phase is from the capacitor to the DC link. This active phase can also be called discharging phase, since the Clamp capacitor is discharged to supply the load.

Figure 31 reports the two operating phases of the Active Clamp circuit, connected to the PDLC topology, evidencing the power flow of the energy associated to the leakage inductance of the transformer.

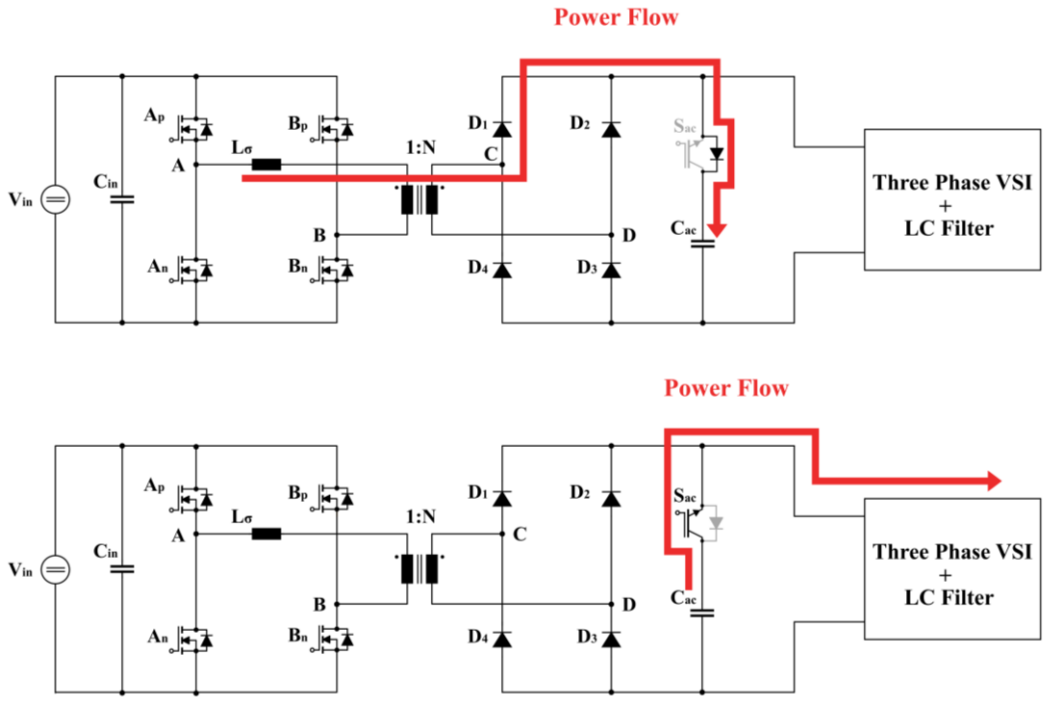

Figure 31 – Passive phase (top circuit) and active phase (bottom circuit) of the Active Clamp circuit of PDLC topology

The above figure graphically describes the fundamental role of the Clamp capacitor that accumulates the energy, due to the overvoltage phenomena of the PSB stage in the passive phase and supplies the load with this latter in the active phase.

2.3.3 Comparison of performances between RC Snubber and Active Clamp circuit

To conclude this chapter, the features and performances of the two analysed solutions for the overvoltage problem are briefly summarized and evaluated to evidence their main strengths and issues. To achieve this aim the discussed solutions are compared in terms of effectiveness, impact on the efficiency, complexity and reliability.

From the point of view of the effectiveness, the Active Clamp solution is extremely better than the RC snubber since it is based on clamping principle of the overvoltage which allows the achievement of desired performance without any trade-off. Instead the performances of the RC snubber are strongly reliant on the value of Snubber capacitor which is inversely proportional to the overvoltage peak and of the resistance, which is responsible of the damping of the voltage overshoot. However, the increase of the capacitor affects the losses of this solution, requiring an accurate design to find the optimal value to ensure a trade-off between the overvoltage and the losses. Consequently, the impact on the efficiency of the RC snubber is higher than the other solution due to the strong interconnection with the control of overvoltage peak which limits the overall performances of the solution. Conversely the Active Clamp solution is featured by a reduced impact on the efficiency due to the elimination of the wasted energy associated to the overvoltage. Moreover, the operation of the power switch is performed in soft-switching in both commutations thanks to the properties of the pulsating DC link and the synchronization with the energising phases of the PSB stage. In the next chapter the nearly lossless commutations of the Active Clamp switch are illustrated thanks to simulation results. Consequently, only the conduction losses of the Active Clamp circuit has to be considered in the estimation of the overall efficiency. In terms of complexity the RC snubber is better since it is based on simple and reliable components that don’t require a control unit to operate. Regarding the number of Snubbers, it is usually equal to the number of the diodes used to implement the output rectifier of the PSB stage even if the use of unique RC snubber, connected to the rails of DC link, is possible. However the implementation of this version requires a different design which takes in to account all the resonances and the consequent

losses have to be handled with only one snubber. Instead the Active solution is more complex due to the particular operating phases, which require an accurate control and the synchronization with the operation of the PSB stage. To conclude in terms of the reliability, both solutions present weaknesses that don't allow the identification of the best solution since they have similar limits. In particular the high number of requested components for the snubber (about eight) affects the reliability of this solution. In case of failure the overvoltage across one of the diodes is not dumped, causing the possible destruction of the component if it goes out of its SOA. Instead the reliability of the Active Clamp is reduced due to necessity of a control unit that, in case of failure, can bring an excessive charge of the Clamp capacitor due to the absence of active phases. Consequently the voltage across the capacitors can overcome their voltage limits, reducing the component life until their failure.

According to the results of the comparison of the two solutions, we can state that the best solution for the PDLC topology is the Active Clamp since it is featured by interesting and desired performances with reduced issues.

CHAPTER 3. ANALYSIS OF PDLC

OPERATING PRINCIPLE

In the previous chapter the PDLC architecture has been introduced and the main features of this topology have been presented, highlighting the aspects of efficiency and reliability. Then the voltage overshoot problem was analysed thanks to the equivalent models of the converter and the solutions to solve it were introduced and evaluated. This chapter is focused on the analysis of the operation of the PDLC that is presented and discussed, especially during the energising phases of the first stage, to analyse the evolution of the main electrical characteristics and the influence parameters as showed in [55]. In this way the relationships among the different components are evaluated to find out the main constraints of this topology and, consequently, to define the design guidelines. As discussed before, the Pulsating DC link voltage presents portions where the voltage is equal to zero, renamed for this Zero Portions (ZP), which can be used to allow the commutations of the VSI stage under ZVS (ZVT) conditions. Consequently we can define the following two main operation phases of the PDLC:

- Freewheeling phase: where the voltage applied to the primary side of the transformer is zero and consequently the intermediate link is featured by Zero portion.
- Energising phase: where the input voltage is applied to the transformer, permitting the supply of the VSI stage. In particular the shape of the pulsating voltage is defined thanks to the interactions between the PSB stage and the Active Clamp circuit. The switching pattern of the VSI stage has been defined in the previous freewheeling phase and it is held for the whole duration of the phase.

The schematic of the PDLC topology is reported in Figure 32. The VSI stage is represented as a simple block.

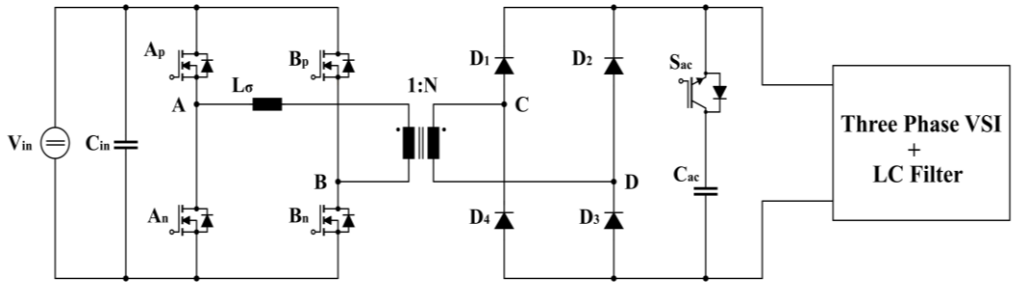

Figure 32 – Simplified schematization of the PDLC topology after the considerations about the role of VSI stage

Due to the invariance of the switching pattern of the inverter, during the energising phase, the VSI stage can be modelled as the equivalent impedance seen from the rails of the DC link, allowing the simplification of the PDLC circuit. In this way the analysis of PDLC can be reduced to the study of the equivalent representations of the PSB stage and the Active Clamp circuit during the energising phase. Considering the same hypothesis for the power devices in the energising phase, defined in chapter 2 and the simplification of the VSI stage, the circuit can be represented as in Figure 33:

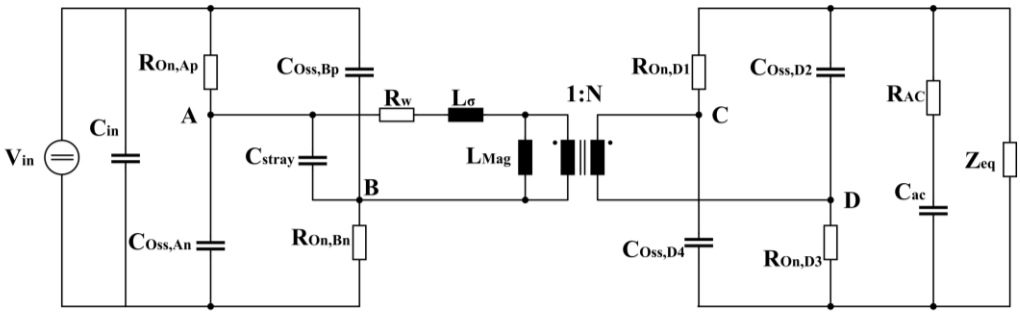

Figure 33 – Equivalent circuit of the converter during the energising phase (Ap – Bn)

where Zeq is the equivalent impedance of the VSI stage, the capacitive effects of the transformer are represented with the equivalent lumped capacitor C_{stray}, connected at the primary side of the transformer. We use the same schematization that we used in chapter 2 to characterize the overshoot of the Pulsating PSB stage. Neglecting all the resistive components associated with the power devices in the conduction phase, the circuit reported in Figure 34 can be obtained:

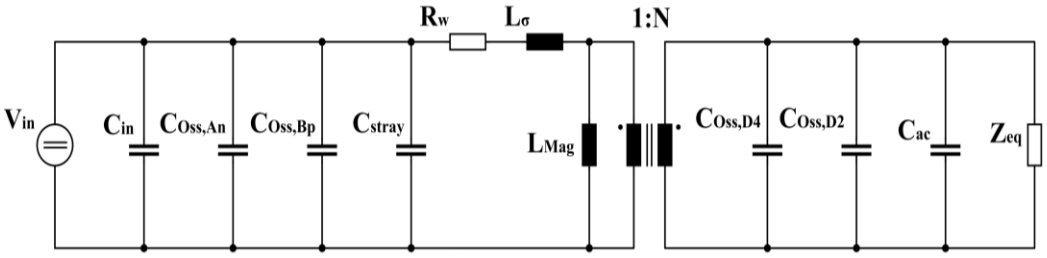

Figure 34 – Simplified circuit of the converter obtained neglecting the resistive components

Solving the parallel of the capacitors on both sides of the transformer, the equivalent simplified circuit of Figure 35 can be obtained. It describes the converter operations during the energising phase.

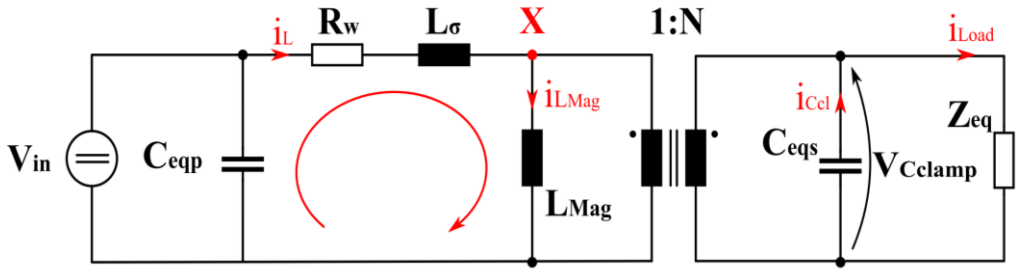

Figure 35 – Final equivalent circuit of the converter during the energising phase

C_{eqp} and C_{eqs} are the total equivalent capacitors at the primary and secondary side of the transformer, respectively. Their values can be obtained as:

$$\begin{cases} C_{eqp} = C_{in} // C_{OSS,An} // C_{OSS,Bp} // C_{stray} \cong C_{IN} \\ C_{eqs} = C_{OSS,D2} // C_{OSS,D4} // C_{ac} = C_{ac} \end{cases} \tag{3.1}$$

Due to the very low values of the output capacitance of the power devices and the lumped equivalent capacitor of the transformer, C_{eqp} and C_{eqs} can be approximated with the input capacitor C_{in} and Clamp capacitor, respectively. Figure 35 represents the operation of the Active Clamp during the active phase where the capacitor gives the stored energy back. Writing the Kirchhoff laws, current law at the node X and voltage law on the primary loop, the following system of equations can be obtained:

$$\begin{cases} V_{IN} - L_\sigma * \frac{di_L}{dt} - R_w * i_L - V'_{Cclamp} = 0 \\ i_L = i_{LMag} + C'_{Cclamp} * \frac{dV'_{Cclamp}}{dt} + i'_{Load} \end{cases} \tag{3.2}$$

Where i'_{Load} and V'_{Cclamp} are load current and the voltage at the secondary side referred to the primary side, respectively. Before to continue the analysis, it is necessary to provide the following observations:

- The load current can be expressed as a function of the voltage across the Clamp capacitor and the equivalent load reported to the output of the converter, as follows:

$$i'_{Load} = f(V'_{Cclamp}, Equivalent\ Load) \tag{3.3}$$

  The voltage across the Clamp capacitor is equal to the pulsating DC link voltage, during the energising phases.
- The magnetising current can be related to the input voltage if the voltage drops across the parasitic parameters of the transformer are neglected without huge errors. Specifically, the current can be expressed with the following relationship:

$$i_{LMag} \cong f(V'_{Cclamp}, L_{Mag}, f_{s,PSB}) \tag{3.4}$$

  where $f_{s,PSB}$ is the switching frequency of the PSB stage.

Putting in evidence the current i_L and the voltage V'_{Cclamp}, the state variables of the system, the following system of differential equations can be obtained:

$$\begin{cases} \frac{di_L}{dt} + \frac{R_w}{L_\sigma} * i_L = \frac{V_{IN} - V'_{Cclamp}}{L_\sigma} \\ \frac{dV'_{Cclamp}}{dt} = \frac{i_L - i_{LMag} - i'_{Load}}{C'_{Cclamp}} \end{cases} \tag{3.5}$$

which describes the dynamic behaviour of the converter during the energising phases of the PSB stage. From the system above, we can note that the dynamics of the state variables are strictly interconnected between each other hence the evolution of the voltage is influenced by the current and vice versa.

The system can be written in a general form as:

$$\begin{cases} i_L = f\left(V'_{Cclamp}, R_w, L_\sigma, V_{IN}\right) \\ V'_{Cclamp} = f\left(i_L, C'_{Cclamp}, i'_{Load}, L_{Mag}, f_{s,PSB}, V_{IN}\right) \end{cases} \tag{3.6}$$

which highlights the link between the state variables i_L and V'_{Cclamp} and the main parameters of influence that condition their evolution.

The closed form solution of this differential system is quite complex since it describes a time variant system whose solution is influenced by the operating phases of the Active Clamp. Consequently, the use of simulations is necessary to analyse the system. For this reason the entire operation of PDLC architecture has been analysed with LTspice circuit simulator, focusing the attention on the energising phase of the PSB stage. Thanks to the use of simulator and appropriate model of power devices the analysis of the PDLC is simplified, allowing a sufficiently accurate study of the electrical characteristics. Moreover, this powerful instrument can be used to perform

multi parametric analysis of the state variables, for different combinations of influence parameters, to find out the limits of the system. On these bases of the evolution of current and voltage, the design limits/criteria of the power stages and electrical transformer can be identified.

3.1 Simulation of the equivalent first stage of the PDLC architecture

In this paragraph the simulation results of the analysis of the PDLC architecture is presented and discussed, focusing the attention on the energising phases of the first stage and the consequent interactions between the main characteristics of the converter. In this way the constraints of the power converter are investigated with the aim to define the design guidelines for this topology. To achieve our aim the evolution of the primary current of the transformer and the pulsating DC link voltage, as well as the connection between them and with other parameters of the converter, are investigated. In this first simulations only the PSB stage and the Active Clamp circuit have been implemented and considered, since they are the main actors in the definition of the two chosen characteristics of our study. Moreover, as showed in the analytical study of the previous paragraph, the VSI stage does not play a role in the analysis of the PDLC architecture during the energising phases. Consequently to reduce the efforts of the simulation time and the complexity of the circuit, we didn't implement the VSI stage but we performed simulations using for Zeq (see Figure 33) both a resistive load and a current generator. In this way we analysed the first stage of PDLC architecture as it is usually done with the input stage of FDLC topology.

3.1.1 Simulations of the PSB stage with a resistive load

The simulation of the converter on a purely resistive load may seem too approximate but it is based on energy considerations. In particular from the energy point of view, this topology supplies the load only during the energising phases, defined by the PSB stage. Therefore closing the Pulsating DC link voltage on a resistive load allows us to achieve the same behaviour of VSI stage in terms of energy transfer from the DC source to the load. From the waveform point of view it is preferable to also consider the effect of the inductance of the output filter as it will be done in the next paragraph.

The simplified circuit of the PDLC has been simulated in LTspice ambient, where the real models of the power devices are available. The parameters and the characteristics of the simulated circuit are summarized in Table 2. All the achieved results are reffered to the simplified circuit of the PDLC which was reported in Figure 32. Before analysing and commenting the simulation results, the definition of the turn-on and turn-off of the power switch of the Active Clamp circuit and its syncronization with the PSB stage will be explained.

Table 2 Main specifications of Spice simulation of PDLC architecture

Input voltage	**600 V**
Power	**8 kW**
Switching frequency of PSB stage	**50 kHz**
Transformer turn ratio	**13/10**
Full Bridge switch model	**C2M0045170D**
Bridge rectifier diode model	**4 x C3D25170H (parallel)**
Load	**Purely resistive**
Input damping capacitor	**400 uF**
Modulation technique of PSB stage	**Traditional Phase Shifted modulation**
Magnetising inductance	**800uH**
Leakage inductance	**(6-12)uH**
Clamp capacitor	**(0.5-220) uF**

In particular the driving signal of the switch is syncronized with the driving signals of the PSB stage, in such a way that its commutations happen during the energizing phase of the PSB stage. In this way the stored energy in the clamp capacitor can be added to the energy of the Pulsating DC link to supply the VSI stage. To describe the operations of the Active Clamp circuit, Figure 36 reports the main waveforms of the active clamp during th energizing phase of the PSB stage for an input voltage of 600V and output power of 8kW. Figure 36 shows the synchronization of the driving signal of the Active Clamp switch and the energising phase of PSB stage as well as the two operating phases of the Active Clamp. Specifically the switch is turned-on during each energising phase when the pulsating voltage is high and is turned off when the phase is nearly to be finished. At the beginning, the current is negative since it flows through the diode due to the clamping of overvoltage on Pulsating DC link. After this phase, the currents starts to rise and flows through the switch, allowing the discharge of the Clamp Capacitor to supply the VSI stage.

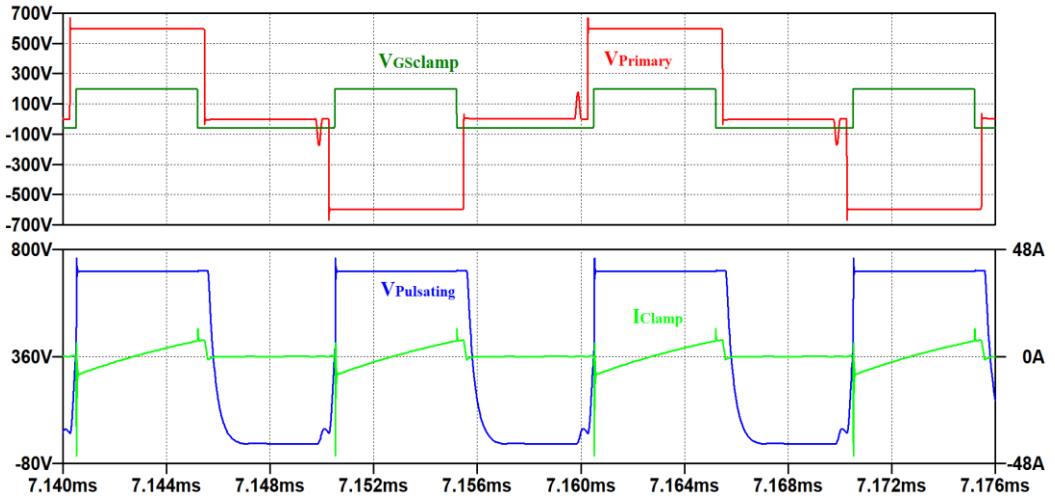

Figure 36 – Primary voltage of transformer (red), Gate-Source voltage of Active Clamp switch (dark green), Pulsating DC link voltage (blue) and current flow in the Active Clamp circuit (green) for input voltage of 600V

From the above figure, we can note that the primary voltage of the transformer is affected by voltage spikes due essentially to the turn-off of the PSB switches for which the ZVS condition is not satisfied.

The details of the commutations of the Active Clamp switch are shown in Figure 37 which confirms its good performances. In particular, it is worth to outline that both the commutations of the switch are achieved in ZVT conditions, thanks to interaction and synchronization between the two power stages. In particular the switch is turned on in ZVZCT conditions since the commutation is performed when the voltage across the switch is zero and the current flows in the antiparallel diode.

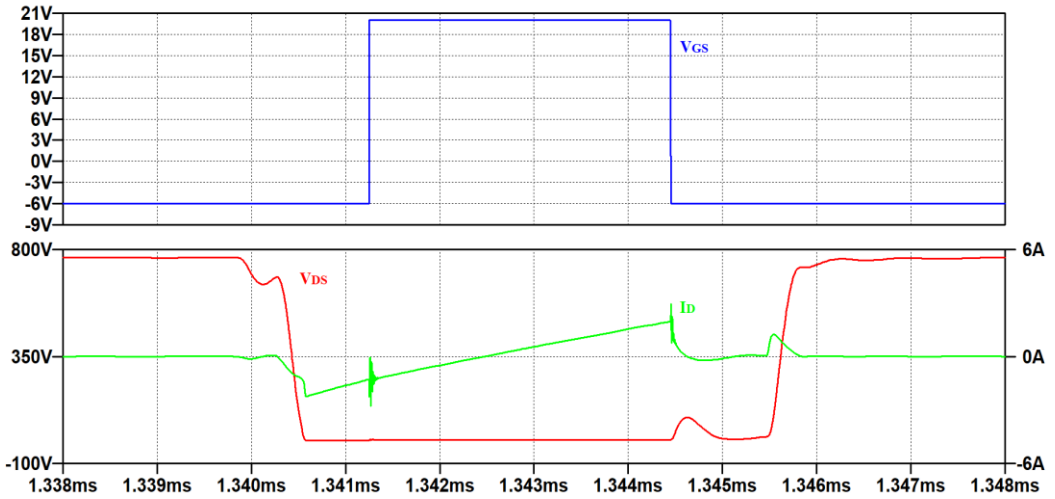

Figure 37 – Detail of commutations of the Active Clamp circuit

3.1.2 Simulations of the PSB stage with a current generator

A second set of simulations has been performed considering a current generator instead of the resistive load at the output of the PSB stage. In fact, the resistive load alone is not sufficient to describe well the behaviour of the converter in which, during the energizing phases, the inductance of the output filter plays a fundamental role. As will be described below, the VSI stage during the energizing phases will always have at least one switch on since the switching of these switches occurs during the subsequent free circulation phases of the PSB stage. Consequently at least one of the filter inductances is connected to the pulsating DC link and therefore to the PSB stage ending up in parallel with the magnetization inductance. Since the value of the inductance is high and the current ripple is negligible, a current generator can be inserted at the output of the PSB to account for the effects of the VSI stage.

An equivalent current generator of 15 A has been used in the simulations which were performed for different values of the Clamp capacitor. The values of the previous analysis have been used for the other parameters. In particular, the leakage inductance has been fixed to 6 µH. Voltage and current in the primary side of the transformer and the Pulsating DC link voltage are reported in **Errore. L'origine riferimento non è stata trovata.**, Figure 39 and Figure 40, for Clamp Capacitor of 1 µF, 30 µF and 220 µF, respectively.

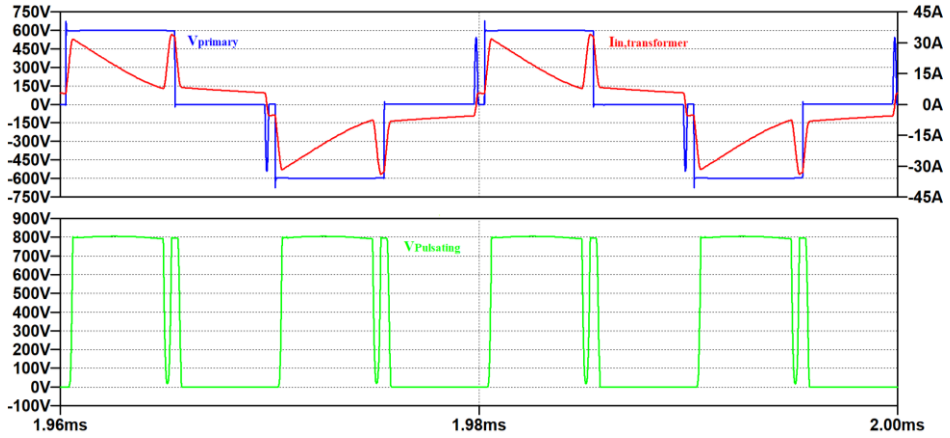

Figure 38 - Detail of the voltage (Blue) and Current (red) on the primary of the transformer and the Pulsating DC link voltage (Green) obtained for VIN= 600 V and Cac = 1 µF

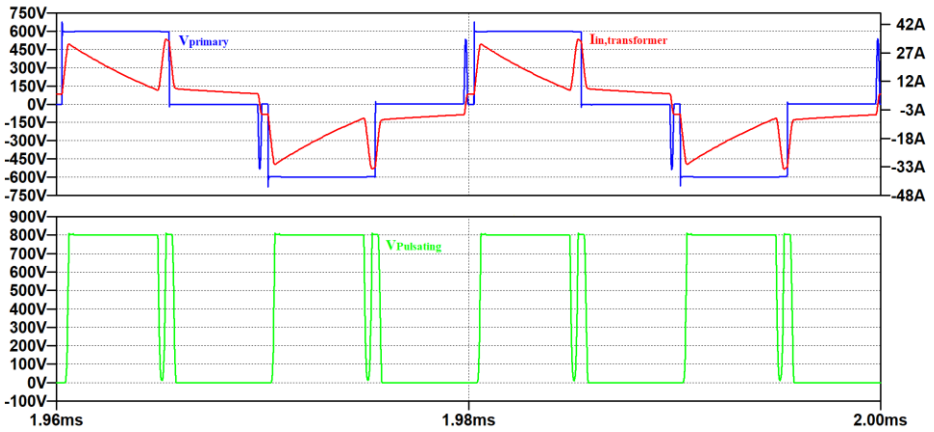

Figure 39 – Detail of the voltage (Blue) and Current (red) on the primary of the transformer and the Pulsating DC link voltage (Green) obtained for V_{IN}= 600 V and C_{ac} = 30 μF

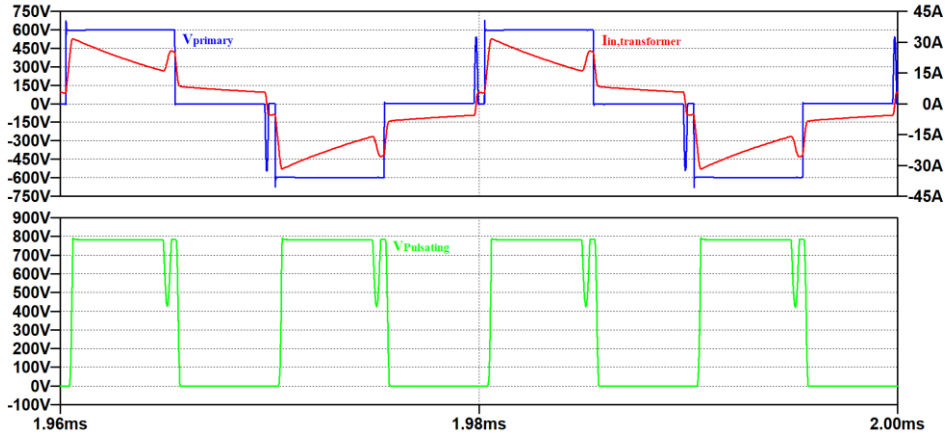

Figure 40 – Detail of the voltage (Blue) and Current (red) on the primary of the transformer and the Pulsating DC link voltage (Green) obtained for V_{IN}= 600 V and C_{ac} = 220 μF

From the comparison of the above figures we can observe that the current in the transformer are practically independent of the Clamp capacitor. Regarding the Pulsating DC link voltage, the increase of the capacitor causes the reduction of the depth of the voltage dip due to the turn-off of the switch of the Active Clamp which causes a resonance between the leakage inductance of the transformer and the clamp capacitor. Moreover, the clamp capacitance influences the evolution of the voltage as shown in Figure 41, where details of the voltage waveforms are reported for different capacitance values.

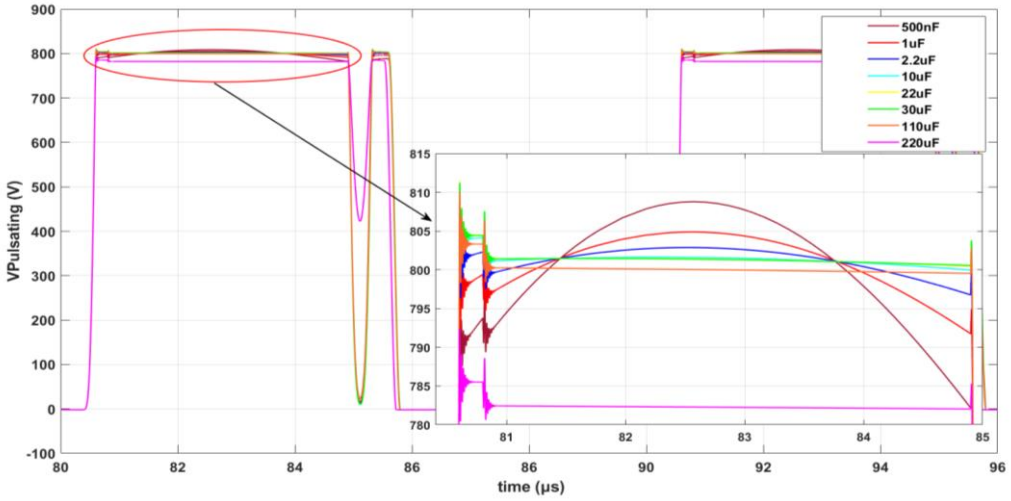

Figure 41 - Evolution of Pulsating DC link voltage and detail for different values of the Clamp capacitor

We can note that low frequency and high frequency oscillations are observed on the voltage waveforms. The former are due to the resonance between the clamping capacitance and the magnetic inductance of the transformer (see Figure 35). The amplitude of these oscillations decreases with the increase of the clamping capacitance. They become more evident for capacitance lower than 10µF. Instead, high frequency oscillations are due to the resonance between the clamping capacitor and the stray inductance of the circuit. Their amplitude also reduces with the increase of the clamping capacitance.

3.1.3 Simulations of the entire converter with ideal semiconductor devices

To conclude the analysis of the behaviour of the PSB stage and to verify the correctness of the models described in the previous sections, simulations of the entire converter have been performed. In these simulations we were not able to use the LTSPICE models of the power semiconductor devices due to the very time consuming simulations and to numerical instabilities experienced during the simulations which caused convergence failures in the largest part of the simulation runs. So we were forced to use ideal diodes and switches for the semiconductor devices of both PSB and VSI stages. The schematic of the circuit used for the simulation is reported in Figure 42 where AC output filter and load are highlighted.

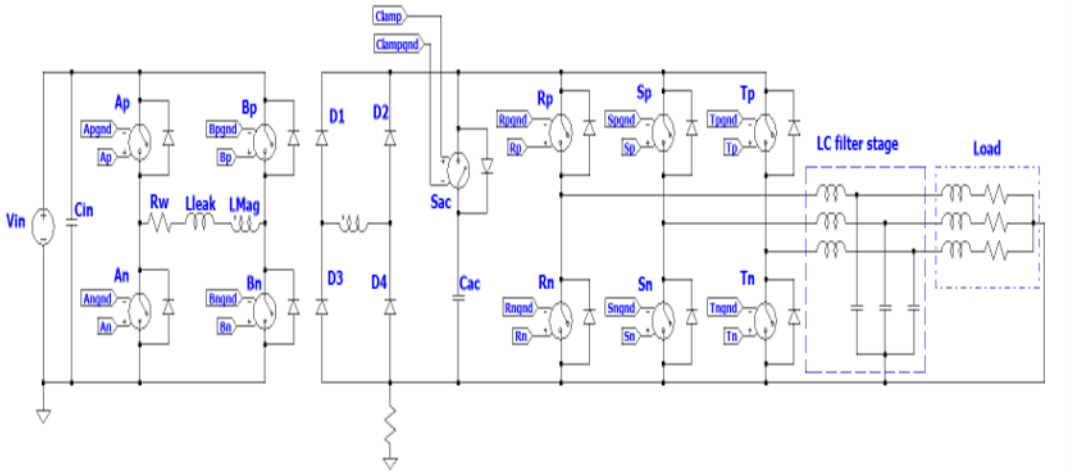

Figure 42 - LTspice schematic used for the simulation of PDLC topology

Power devices and diodes of the PDLC topology have been represented in the schematic with simple switches while the transformer has been modelled with the conventional model, neglecting its capacitive effects. A three-phase star-connected LC low-pass filter has been connected between the three-phase bridge and three-phase ohmic-inductive load also star-connected. Figure 43 reports the voltage and current on the primary side of the transformer and across the low side switches of the legging and leading legs of the PSB stage. We can note that the ZVS condition is achieved for the turn-on of the leading leg while the stored energy is not enough to guaranty ZVS switching of the legging leg.

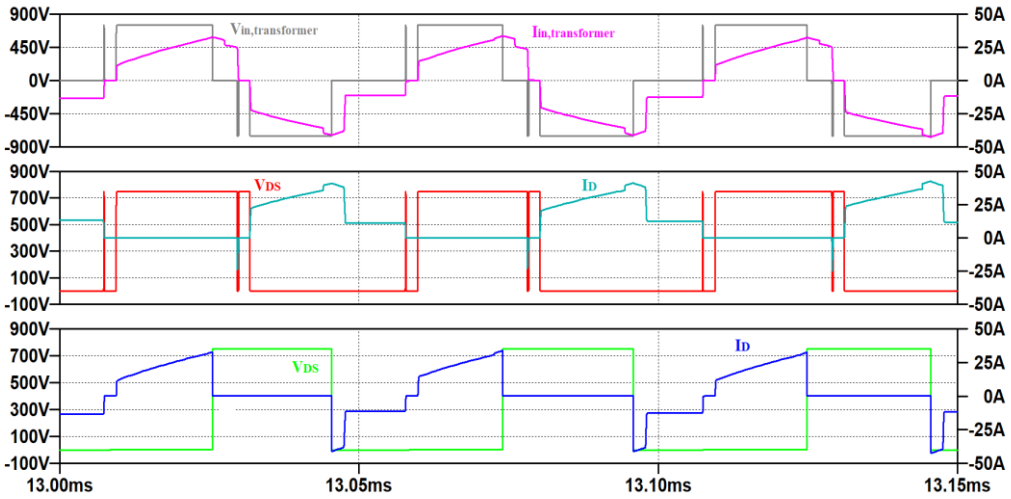

Figure 43 – Detail of voltage and current on the primary side of the transformer (top plot), Drain-Source voltage and Drain current of low side switch of legging leg (middle plot) and of low side switch of leading leg (bottom plot) in case of entire converter with ideal switches

To verify which modelling of VSI stage is the best solution for the simulation with the real models of the devices, Figure 44 and Figure 45 report the same waveforms of Figure 43 obtained for current generator and resistor as load, respectively.

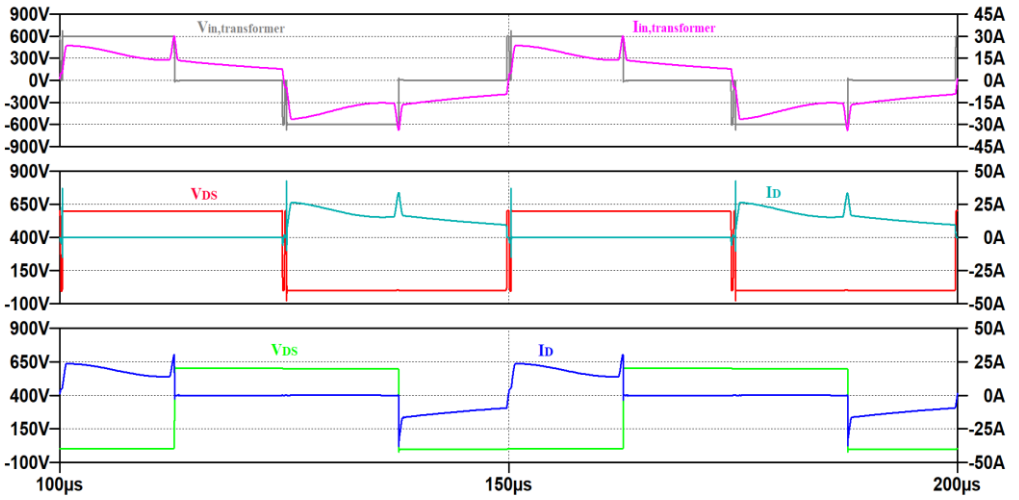

Figure 44 – Detail of voltage and current on the primary side of the transformer (top plot), Drain-Source voltage and Drain current of low side switch of legging leg (middle plot) and of low side switch of leading leg (bottom plot) in case of PSB stage loaded with a current generator

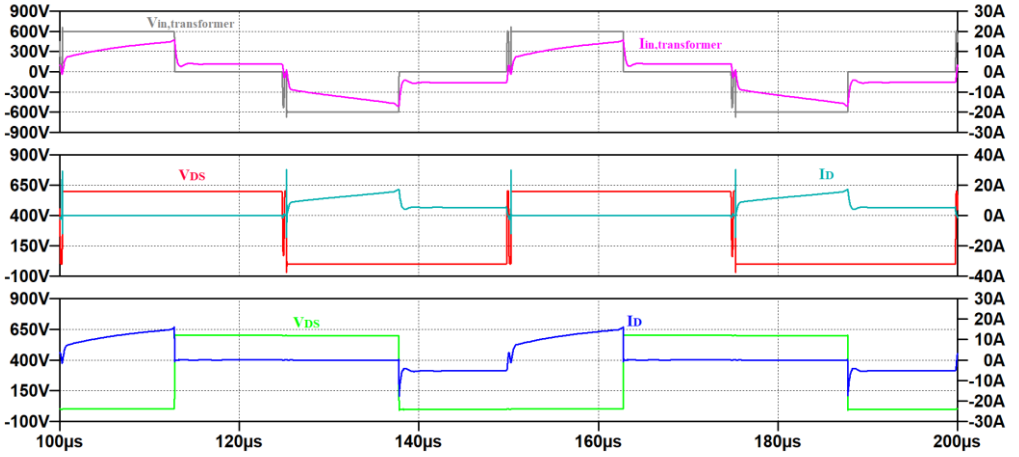

Figure 45 - Detail of voltage and current on the primary side of the transformer (top plot), Drain-Source voltage and Drain current of low side switch of legging leg (middle plot) and of low side switch of leading leg (bottom plot) in case of PSB stage loaded with a resistor load

Comparing the three above figures, we can recognize how the evolutions of the waveforms obtained for the PSB converter with the resistive load are much closer to those of the entire converter than those obtained for the converter loaded with a current

generator. In fact these latter waveforms exhibit different current slopes and much larger current peaks compared with those of the entire converter. The better results of the resistive loaded PSB converter are particularly true if we want to determine the power losses of the semiconductor devices as it is done in the next section. So, considering the impossibility of using the LT-SPICE model of power devices in the entire converter circuit, we decided to continue running the simulations on the converter where an equivalent load resistor is used to account for the VSI stage.

Before analysing the results of the multi-parametric analysis of the simplified converter, some considerations about the influence parameters need to be done. The number of these latter is considerable (about eight parameters) and the influence among them is very strong, involving the primary current of transformer and Pulsating voltage. This makes the analysis quite complex and difficult. Moreover in this scenario, we have to consider that few influence parameters are limited by other features of the converter, as efficiency and volume, which reduce the degrees of freedom of the analysis. For these reasons in our analysis we imposed the values of several influence parameters, according to other design considerations, and have analysed the evolutions of main characteristics of converter for different combinations of the chosen influence parameters. The main analysis we have performed is the study of the voltage overshoot for different values of the Clamp Capacitor and the interaction with the primary transformer current. This study has been made for different values of the leakage inductance of the transformer to evaluate its effects on the overshoot voltage and on the evolution of the primary current.

3.1.4 Analysis for different combinations of Clamp capacitor and leakage inductance of the transformer

The aim of this study is to evaluate the influence of the value of the Clamp capacitor on the evolution of Pulsating DC link voltage and in particular on the initial overshoot. For this reason the leakage inductance of the transformer is fixed to 6uH while for the capacitor a wide range of values (from hundreds of nF to hundreds μF) has been used. Figure 46 shows the evolution of the Pulsating voltage for different values of Clamp capacitor and the detailed zoom of the initial overshoot voltage.

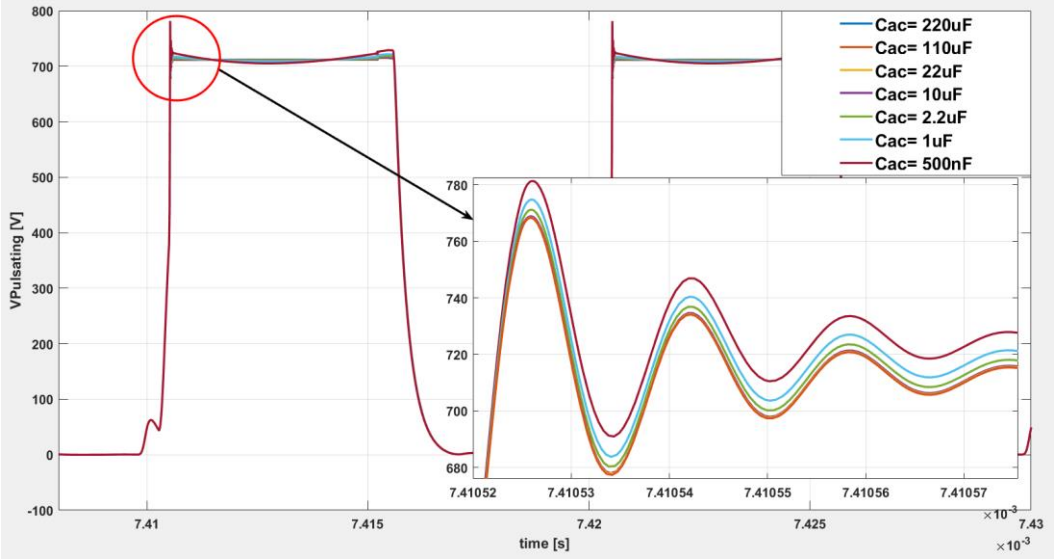

Figure 46 – Evolution of Pulsating DC link voltage and detail of the voltage overshoot for different values of the Clamp capacitor

Analysing the detailed zoom of the overshoot, we can note that a drastic reduction of the value of the capacitor provides a limited increase of the voltage peak from 768V to 780V. So the weak invariability of the peak, with respect of the Clamp capacitor, permits the minimization of the value of capacitor with the following advantages:

- Reduction of the weight and volume of the power stage.
- Further improvement of the dynamic response of the considered PDLC architecture thanks to the elimination of bulky and large components.
- Possibility to use more reliable technology of components, which are strongly dependent on their values.

Moreover, the weak dependence of the peak voltage with the capacitor permits its design, to optimise other features and/or parameters of the converter. This is the case of the value of the transformer leakage inductance, which can be optimized thanks to the appropriate choice of the capacitor. To see the effects of the Clamp capacitor on the leakage inductance, the voltage and the current of this latter have been analysed together the Pulsating DC link voltage for two different values of the capacitor, namely 80µF and 300µF. The obtained waveforms are reported in Figure 47 .

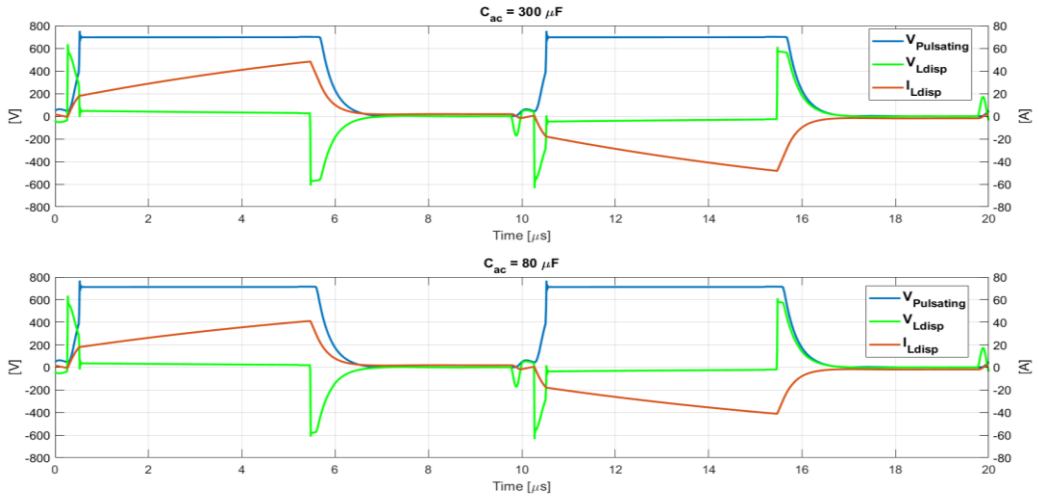

Figure 47 – Waveforms of pulsating DC link voltage (blue), voltage across (green) and current (red) in the leakage inductance of the transformer for two values of Clamp capacitor, namely 80uF and 300uF.

Comparing the two cases of the above figure, we can observe that the current peak is increased from 40A to nearly 50A when the Clamp capacitor is changed from 80µF to 300µF. Instead the peak voltage of the initial overshoot of the pulsating voltage is feature by a slightly reduction due to the increase of the capacitor. On the basis of the achieved results the investigation, on the link between the values of leakage inductance and Clamp capacitor, was continued with several simulations where many combinations of the parameters have been tested. The results of this study are reported in Figure 48 where the current peak of the primary side of the transformer (left plot) and the overvoltage peak of the Pulsating DC link voltage (right plot) are reported as function of Clamp capacitor, for two values of leakage inductance, namely 6 µH and 12 µH. The overvoltage peak is calculated as the difference between the peak of initial overvoltage and the flat values that is reached by the Pulsating DC link after the evolution dumping.

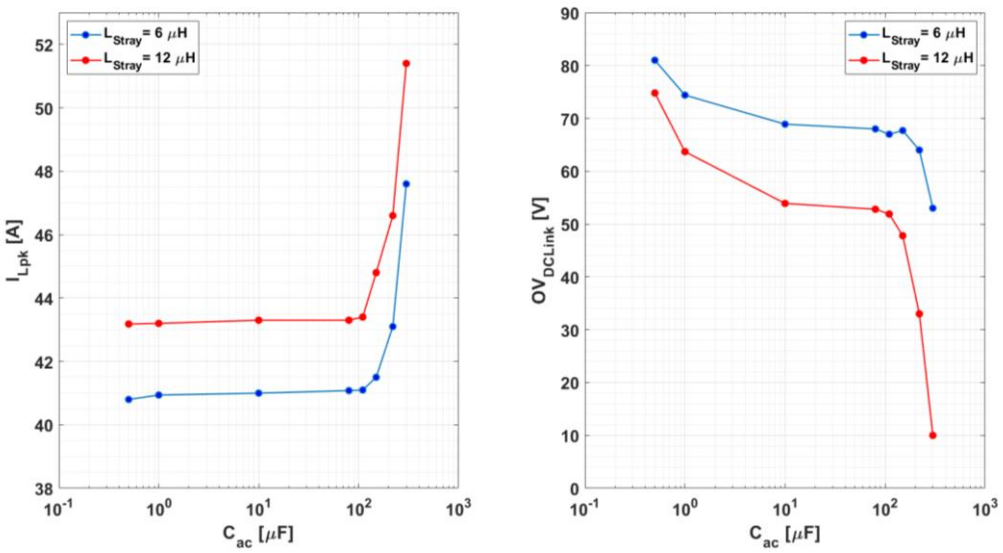

Figure 48 – Peak values of the primary current of the transformer (left side) and overvoltage values of Pulsating DC link voltage (right side) vs Clamp capacitor for two values of leakage inductance, namely 6uH and 12uH.

Analysing the evolution of the peak current, we can clearly see that the rise of this latter is proportional to the increase of the value of the leakage inductance. Moreover the peak current is practically constant up to hundreds of μF while for larger values of the capacitor it increases significantly. On the other hand, the evolution of the peak overvoltage shows how the capacitor as and the inductor can be used to control the peak. For example, for capacitor values greater than one hundred μF the reduction of the peak is very good while in the range 500nF-100μF the reduction is still reasonable in comparison with the flat value of Pulsating DC link voltage. Instead the value of the leakage inductance allows the shift of the evolution of characteristics reported in the figure. In particular the reduction of the inductance permits the reduction of the current peak but causes the increase of the overvoltage. On the contrary the increase of the inductance allows us to limit the overvoltage peak. Consequently, a trade-off between the values of the leakage inductance and the Clamp capacitor, needs to be found, allowing to achieve the best performances for both quantities. Analysing the different trends of Figure 48, we can observe that the area between the two values of leakage inductance represents the design surfaces for the characteristics. Practically these two areas define the limits for our design, according to the parameters and condition used in the simulations. Moreover, we can note that the design surface is strongly dependent on the difference between the two values of the leakage inductance, which define the extension of the surface. For example using two very close values of the inductance,

produces a reduction of the design surface, proportional to the difference of the two values, which reduces the degrees of freedom of the design. Further constraints on the choice of the leakage inductance are due to the following considerations:

- Definition of ZVS conditions for lagging leg of PSB stage: The achievements of soft-switching conditions for the leg that commutates after a freewheeling phase of the PSB stage, are defined by the stored energy in the leakage inductance of transformer. However due to the low value of this inductance and consequently of its stored energy, it is requested a high value of the current to satisfy the ZVS conditions for the lagging leg. Consequently this latter has to be designed to ensure the ZVS conditions for the turn-on of the power switches for a restricted range of current.
- Efficiency of electrical transformer: The leakage inductance is always a parasitic parameter which accounts for the stray flux in the transformer. The rise of this lumped value causes the increases the voltage drop on the primary side of transformer with the consequent reduction of the operating voltage.

Due to the different type of characteristics, current peak and overvoltage peak and their scale, it is not easy to draw a single surface reporting on the same plot both quantities. Therefore in the definition of the surface and consequently of the design guidelines of this converter, the trends of the current and overvoltage have to be evaluated individually. The optimum design surface can be defined as the area delimited by the values of leakage inductance, which permits the minimization of the current peak and voltage overshoot at the same time. Observing the behaviour of the characteristics reported in Figure 48, we can recognize three distinct operation regions which can be classified as a function of Clamp capacitor in the following way:

- $C_{ac} < 10\mu F$: In this region the current peak achieves the global minimum value while the overshoot voltage reaches the global maximum values.
- $10\mu F > C_{ac} < 100\mu F$: In this intermediate region both the characteristics of converter have low values (local minimum values) thanks to the flat evolution of peak current and overvoltage. Consequently the range of C_{ac} corresponds to the optimal design surface, defined before.
- $C_{ac} > 100\mu F$: Instead in this region we have the opposite behaviour of the first one. In particular the increase of the capacitor over hundreds of μF, provides the achievements of the overvoltage global minimum value while

the current peak rises until it reaches the maximum value in the simulation range.

Figure 49 depicts primary current peak and overvoltage in the same conditions of the previous figure, but the optimal design surfaces are highlighted.

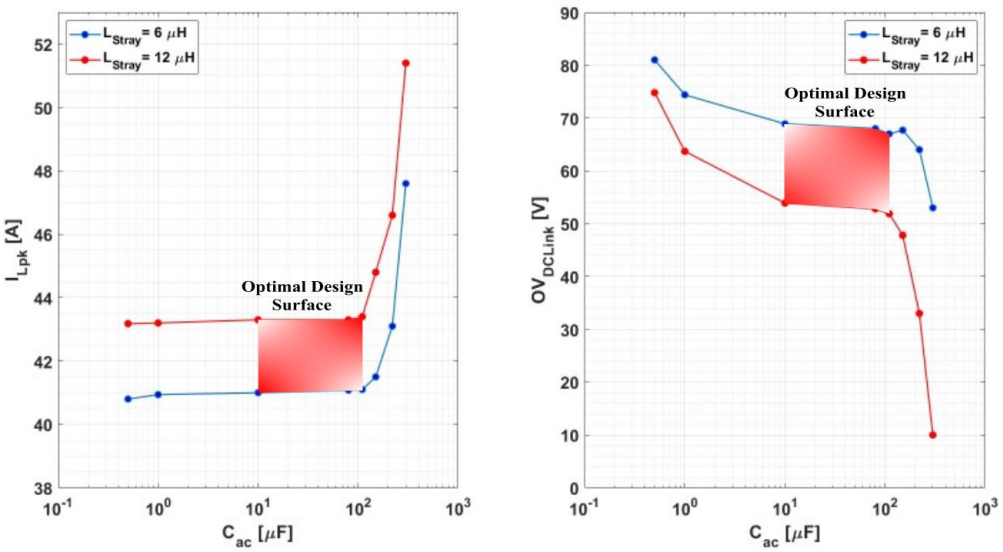

Figure 49 – Evolution of the Peak values of the primary current of the transformer (left side) and overvoltage values od Pulsating DC link voltage (right side) vs Clamp capacitor, with the optimal design surface highlighted.

As shown in the above figure, the design of Clamp capacitor can be simplified as the research of minimum value in the range of the evidenced surface, since the dependence of current peak and overvoltage is characterized by a nearly zero slope. Thanks to this simplified design rule, other design aspects of the converter can be enhanced as the dynamic response, reliability and volume reduction. Instead the design of leakage inductance is related to the definition of the ZVS range of the Pulsating PSB stage and is analysed in the next chapter.

3.1.5 Effects of the leakage inductance and Clamp capacitor on the power losses of the Pulsating PSB

Thanks to the results of the first study performed in the previous paragraph for different combinations of the main influence parameters and related observations, the optimal design surface has been defined as well as a simplified design law for the Clamp capacitor. To complete the multiparametric analysis of the first stage of the PDLC topology, the power losses of the Pulsating PSB stage were estimated and analysed to evaluate how they are influenced by the different combination of leakage

inductance and Clamp capacitor. In particular the losses were evaluated for the same ranges of capacitor an inductance, used in the previous analysis, for two different values of switching frequency of the Pulsating PSB stage. In this way another influence parameter of the main characteristics of the converter is introduced and used in the definition of the design guidelines of the system. To conclude, this analysis was focused on the semiconductor losses of the converter leaving aside the transformer losses, which would require accurate designs for the different test conditions. Table 3 reports the simulation results achieved for a switching frequency of 50 kHz while the Table 4 reports the results for switching frequency of 20 kHz. The tables report also the peak and RMS value of the current at the primary side of the transformer.

Table 3 Results of the losses analysis of the Pulsating PSB stage for a switching frequency of 50kHz

Cac (uF)	L_σ= 6uH			L_σ= 12uH		
	I_{Lpk} (A)	I_{LRMS}(A)	Losses (W)	I_{Lpk} (A)	I_{LRMS}(A)	Losses (W)
1	40,8	22,8	201,7	43,2	23,4	202
10	41	22,7	200	43,3	23,4	198,5
33	41	22,7	200	43,1	23,3	198,1
110	41,1	22,7	200,2	43,3	23,4	198,3
220	43,1	23,7	206,5	46,6	25,2	210
300	47,6	25,9	221	51,4	27,9	230,5

Table 4 Results of the losses analysis of the Pulsating PSB stage for a switching frequency of 20kHz

Cac (uF)	L_σ= 6uH			L_σ= 12uH		
	I_{Lpk} (A)	I_{LRMS}(A)	Losses (W)	I_{Lpk} (A)	I_{LRMS}(A)	Losses (W)
1	39,4	23,1	129,8	44,6	23,8	138,8
10	41,3	23	128,3	45,8	23,6	135,1
33	41,5	23	127,9	45,8	23,6	134,6
110	41,5	23	128	45,8	23,6	134,5
220	41,7	23,1	128,6	46,7	24,1	138,7
300	42,7	23,6	132	49,8	25,6	147

By observing and comparing the results of the above tables, it can be seen that the power losses are practically constant as the Clamp capacitor varies with the exception of the value of 300uF, which causes a significant increase of the losses (close to 10% of the total). This behaviour can be explained, observing the values of the currents at

the increase of the capacitor which are practically constant up to C_{ac}=300μF. Therefore the increase of the current, especially the RMS value, due to the capacitor causes a rise of the conduction losses of the converter. The switching losses can be considered approximately constant for assigned value of frequency and inductance, since the energy contributes due to the variation of capacitance are insignificant. For completeness we can note that the variation of current and power losses are zero in the range of the values that defined the optimal design surface, in the previous analysis.

Figure 50 reports converter power losses vs the values of Clamp capacitor extracted from Table 3 and Table 4.

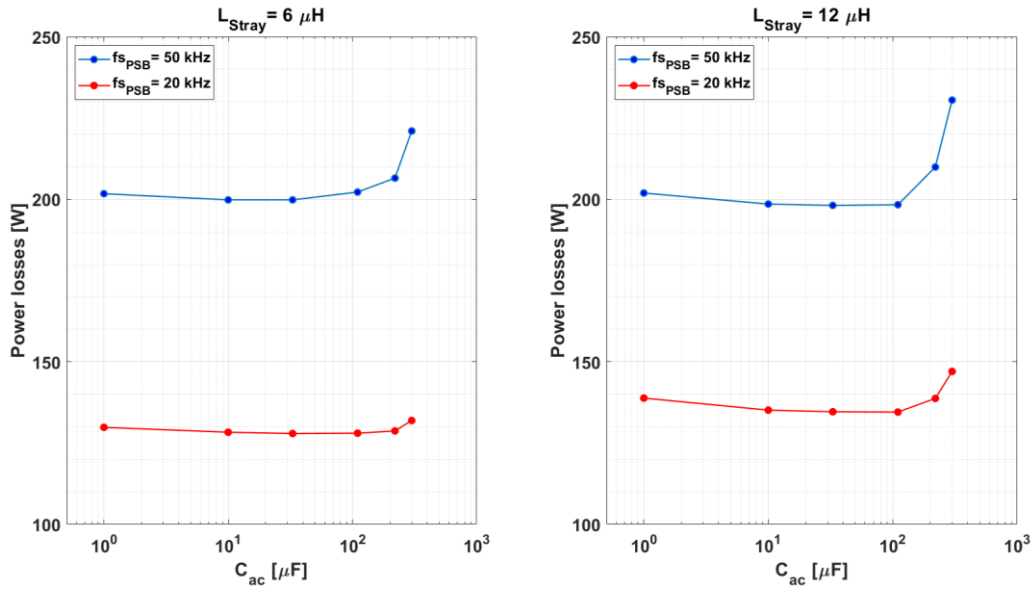

Figure 50 – Power losses of the Pulsating PSB stage vs the Clamp capacitor for two values of switching frequency, respectively 20kHz and 50kHz, for two values of leakage inductance of 6uH and 12uH

We can appreciate how the losses are strongly dependent on the value of switching frequency of the Pulsating PSB while the effects due to the leakage inductance are quite limited. In particular doubling the values of leakage inductance produces slight increase of the losses (about 10W for 20kHz), which becomes negligible at the rise of the operating frequency. Consequently, as expected, the choice of switching frequency has to be made on efficiency consideration, taking into account that its rise allows the reduction of the transformer size.

3.2 Analysis the Pulsating PSB stage and comparison with the FDLC PSB stage

Let's continue the analysis of the characteristics of the Pulsating Phase Shifted Bridge focusing the attention on the commutations of the power switches and on the definition of the ZVS range for both the legs. In this study only the operating phases of the PSB stage are considered, since the contribute of the Active Clamp is provided only during the energising phases. Consequently this stage, in particular the relative capacitor, doesn't participate to the definition of the commutations of the legs of the PSB stage and the relative ZVS ranges. To achieve this aim the different operating phases of the considered converter have been compared with the ones of classical PSB stage, to highlight the differences and continue to provide design suggestions for this innovative topology. As introduced briefly in the first chapter, a conventional PSB stage is featured by ZVS condition for the turn-on of all the switches, thanks to the resonance between the output capacitors of the leg and the equivalent inductance of the stage during the commutation. Moreover, the energy stored in the inductor has to be greater than the energy stored in the capacitors, to zero the voltage across the switch that we need to turn-on. From a literature review of this topic, the commutations of PSB stage are featured by the following two different behaviours, according to the operating phase they come after:

- Commutation after an energising phase: In this commutation all the inductances of the PSB stage (magnetising, leakage and output filter) give a contribution, providing an extend ZVS range for the switches of this leg. Thanks to this wide ZVS range and the consequent minimization of the switching losses at the turn-on, this leg is called Leading leg.
- Commutation after a freewheeling phase: Instead in this commutation just the leakage inductance gives a contribute, reducing the ZVS range for the power switches due to the low values of this parameter. For this reason the design of the PSB stage and in particular the choice of leakage inductance, are performed to ensure an adequate ZVS range for this leg. Due to the limited ZVS range for the power switches, this leg is renamed Lagging leg.

The concepts of Leading and Lagging legs can easily be extended to the analysis of pulsating PSB stage, since from the topological point of view the two converters are similar, excepts for the absence of output filter in the pulsating one. In any case the operations of the two converters are identical because the pulsating DC link is connected to the VSI stage where, at any time, at least two switches of distinct inverter

legs are in the on state and connect the output AC filter to the DC link. Consequently, the role played by the filter inductance of the conventional PSB is assumed in the Pulsating PSB by the inductance of the VSI output filter. To take this into account the schematics of the pulsating DC link reported below still include the inductor L_{ACF}, the capacitor C_{ACF} of the output filter as well as the generic load. The on resistance of the conducting switches of the VSI stage are neglected.

As it is done for the conventional PSB stage, the analysis of the pulsating PSB stage starts with an energising phase. Let us consider the energising phase where the switches A_p and B_n of the main diagonal are in the on state. The equivalent schematic of the analysed converter during their energising phase is represented in Figure 51.

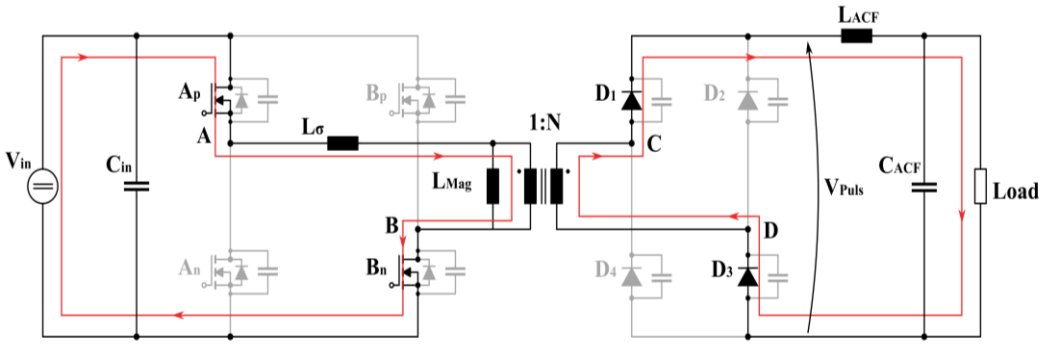

Figure 51 – Energising phase of the Pulsating PS , triggered by the secondary diagonal

During this phase the input voltage is applied to the primary side of the transformer, producing the rise of the input current according to the differential equation supplied in the previous paragraph. On the secondary side of the transformer the primary voltage is applied multiplied by the turn ratio of the transformer. The voltage is applied to the load and equivalent AC filter, thanks to the conduction of the diodes D1 and D3, which have negligible voltage drop. So this phase is very similar to the equivalent operation phase of traditional PSB stage, thanks to the equivalent AC filter of the inverter stage. The subsequent operation phase starts when B_n is turned-off, triggering the resonant commutation of the leg where the output capacitances of the switches play a fundamental role together with the inductances of the power stage. Figure 52 depicts the equivalent representation of the Pulsating PSB during the resonant commutation of the Leading leg.

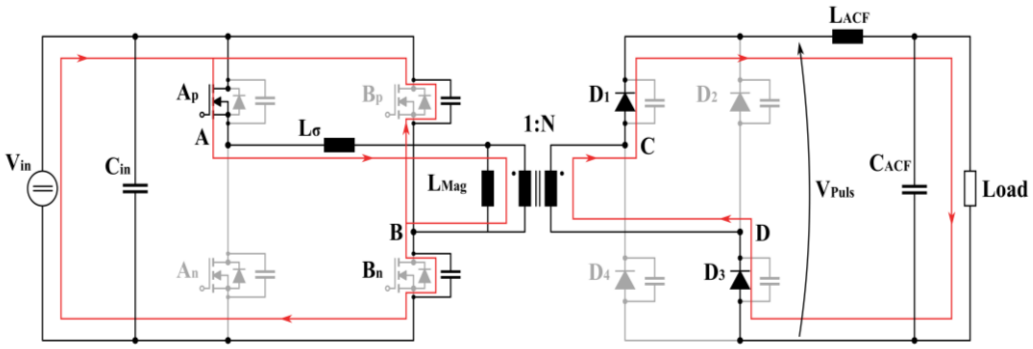

Figure 52 – Resonant commutation of the Leading leg of the Pulsating PSB

Since this commutation happens after the energising phase of PSB, this leg can be considered as the Leading leg as said before. The resonant transition, which defines the ZVS conditions for the turn-on of the high side switch of the leg ($B_{p)}$ is based on resonant LC circuit where the two parameters are the equivalent capacitance and inductance of the circuit in this phase. In particular observing the circuit reported in the above figure, the equivalent capacitance C_{eqv} is equal to the parallel between the output capacitances of the switches and the output capacitance of the diodes in the off state referred to the primary, neglecting the stray capacitance of the transformer. Instead the equivalent inductance is equal to the series between the leakage inductance and the parallel of the magnetising and filter ones. To achieve the ZVS condition the following relationship has to be verified:

$$\left(L_\sigma + L_{Mag}//L_{ACF}\right) * i_{op}^2 \geq C_{eqv} * V_{op}^2 \qquad (3.7)$$

where i_{op} and V_{op} are the current and the voltage considered in this operation phase. This inequation is the same of conventional PSB stage where the AC filter inductance substitutes the filter inductance of the PSB stage. At the end of the resonant commutation phase, the output capacitor of B_n is completely charged while the capacitor of the high side switch has reached the zero voltage, allowing the conduction of the antiparallel diode. The next phase, also called passive freewheeling, is featured by the freewheeling of the current through the high side switch A_p and the antiparallel diode of switch B_p. Figure 53 refers to the operations of the converter during the freewheeling phase when the current flows through the diode antiparallel to B_p.

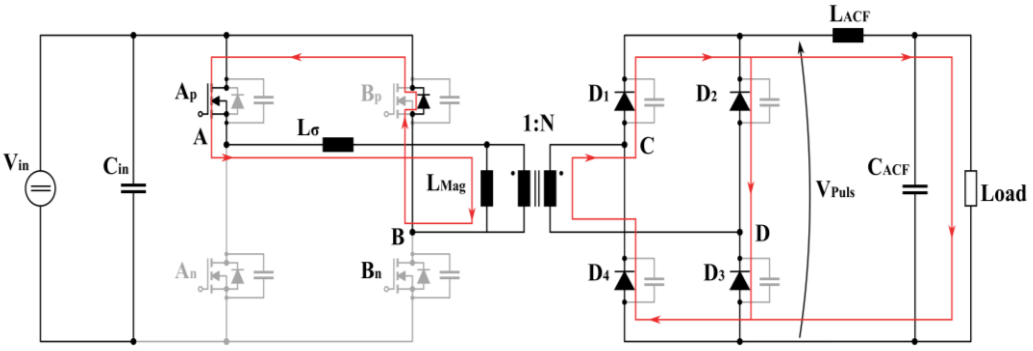

Figure 53 – Passive freewheeling phase of the analysed converter

As it happens in a conventional PSB stage, the current through the L_{ACF} keeps the diodes D1, D2, D3 and D4 in conduction and then the DC link voltage is zero. It is important to note that in this phase the switches of the VSI stage are commutated at zero voltage. The current can flow through the turned-on switch of the VSI stage at the onset of the subsequent energising phase, imposed by the pulsating PSB stage only if the current on the equivalent inductor is zero. The duration of the freewheeling phase is equal to the dead time between the turn-off of the low side switch and the turn-on of the high side switch, which will happen in the next phase. When the high side switch is turned-on, in ZVZCS condition thanks to the diode, the phase called active freewheeling starts as showed in the schematization of the Figure 54.

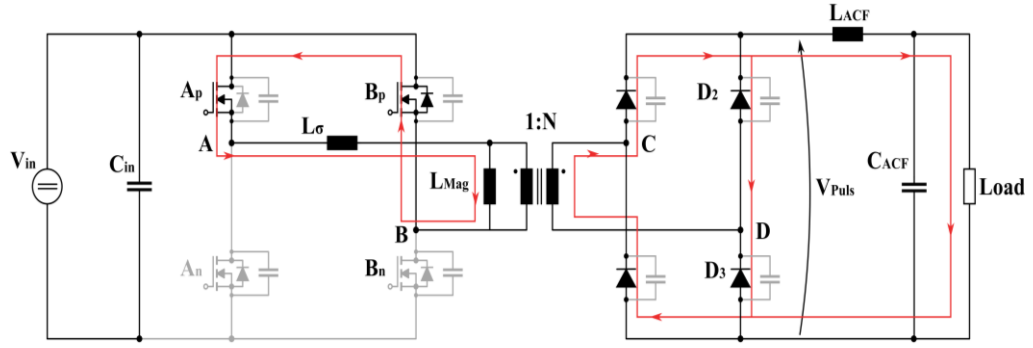

Figure 54 – Active freewheeling phase of the analysed converter

Then the high side switch A_p is turned-off, starting another resonant commutation which, this time happens in the Lagging leg of the PSB as depicted in the equivalent schematic of Figure 55. As for the other leg, a resonant transition takes place. It is based on a LC resonant circuit which have the same equivalent capacitance of the other leg but the equivalent inductance is only equal to the leakage inductance of the transformer, since the magnetizing one is short-circuited.

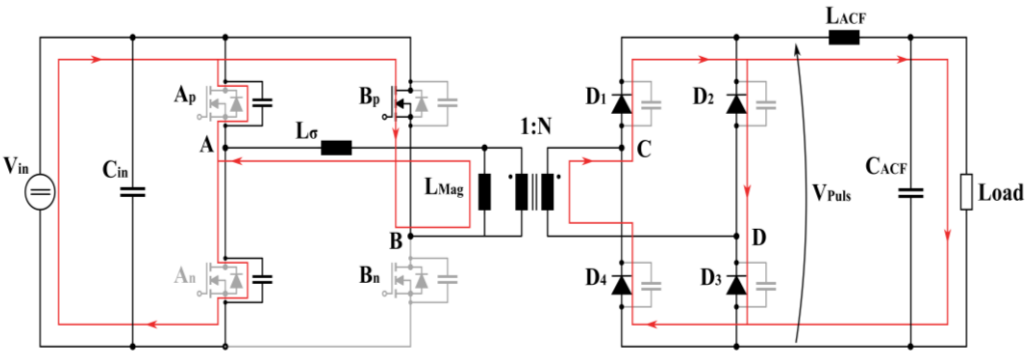

Figure 55 – Resonant commutation of the Lagging leg of the Pulsating PSB

Consequently the ZVS range of this leg is defined by the following relationship, which is the same of the conventional PSB stage:

$$L_\sigma * i_{op}^2 \geq C_{eqv} * V_{op}^2 \tag{3.8}$$

As for the conventional PSB, the Lagging leg has worse ZVS performances due to the value of leakage inductance which allows the achievement of soft-switching only for high values of current. Instead, for light loads, the energy stored in the inductance is not enough to complete the discharge-charge process of the output switch capacitors of the leg, causing the capacitive turn-on of the switch. Consequently the switching losses of the leg are increased due this inefficient switch commutation. If the inequation 3.8 is satisfied, the passive regeneration phase can start with the conduction of the antiparallel diode of switch A_n. This phase ends when the switch is turned-on, passing to the active regeneration which must be delayed in the case of loss of ZVS condition due to low output current. Figure 56 and Figure 57 represent the passive and active regeneration phases of the Pulsating PSB, respectively.

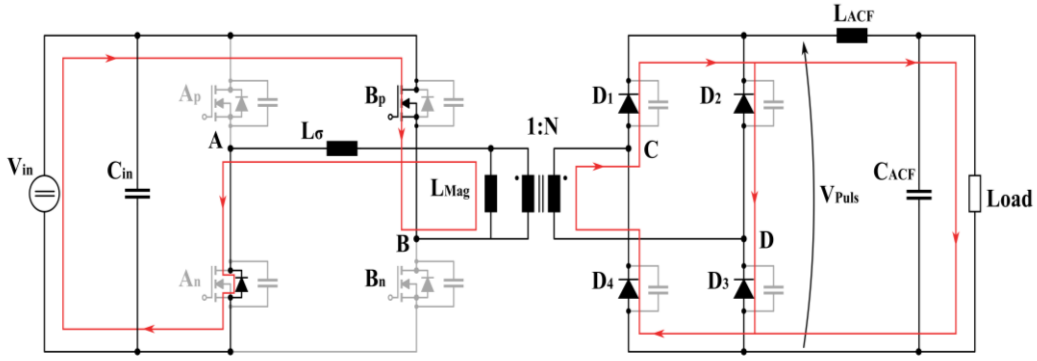

Figure 56 – Passive regeneration phase of Pulsating PSB

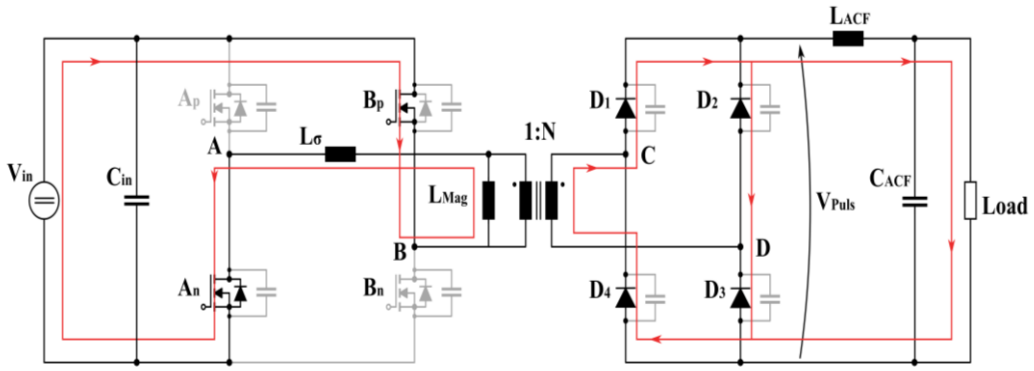

Figure 57 - Active regeneration phase of Pulsating PSB

With both the switches A_n and B_p turned-on (secondary diagonal), another energising phase takes places and the input voltage with negative sign is applied to the primary side of the transformer, assuring the periodicity of the transformer voltage and a zero DC component in the transformer current. Consequently the load is supplied thanks to the conduction of the power diodes D2 and D4, which rectify the input voltage. The schematization of the converter during the second energising phase is represented in Figure 58.

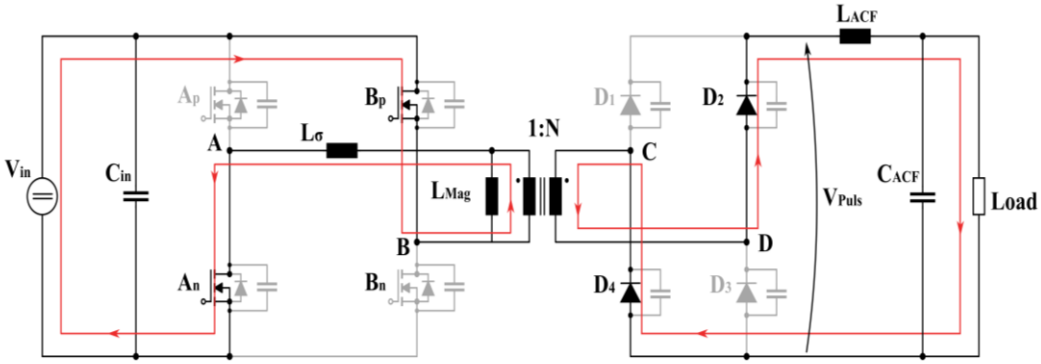

Figure 58 – Energising phase of the Pulsating PSB, triggered by the secondary diagonal

In conclusion the operating phases of the pulsating PSB are very similar to the conventional PSB stage, for which the role of filter inductance is assumed in the pulsating PSB by the output filter inductance of the VSI stage.

3.3 Final overview of design guidelines

In the previous paragraphs the attention was focused on the particular operation of the first stage of PDLC, Pulsating PSB stage and the interaction with the Active Clamp circuit. Moreover the several working phases of the first stage were presented and described, and it was found that they are very similar to the conventional PSB stage. Thanks to these analysis based on the LTspice simulation, the limits of the main features of the PDLC topology have been identified together with the trade-off between the main influence parameters. In this paragraph all the results achieved in the definition of the design guidelines, will be briefly discussed and combined to provide the complete design horizons for the PDLC topology. Moreover further consideration and details on other features as efficiency, volume and power density will be proposed to complete the discussion of this topic. The study of the overvoltage and current peak for different combination of leakage inductance and Clamp capacitor, has showed how it is strictly necessary find a trade-off to optimize the analysed characteristics. This is essentially due to the opposite effects that the variations of inductance and capacitor have on the evolution of overvoltage and current peak. To simplify the definition of design limits it is necessary define the optimal design surface, which represents the combinations of parameters that allow the minimization of both characteristics. This surface, delimited by the optimal ranges of the values of inductance and capacitance represents the first step of the design from which the others parameters will be designed. In particular the range of possible values of leakage inductance can be used to study the extension of the ZVS range for the lagging leg for different load conditions. In this way the optimal value of inductance can be found to guarantee an adequate ZVS range for the leg of the Pulsating PSB without significant effect on the performances in terms of current peak and overvoltage. Instead to design other parameters, like magnetising inductance and switching frequency of the PSB stage, it is necessary to analyse the losses of the converter. In particular the increase of this inductance, induces the increase of ZVS range of the Leading leg of the converter but at the same time causes the increase of volume and weight of the transformer for given frequency value. It has also an effect on the turn ratio of the transformer. Instead the rise of switching frequency allows the reduction of the dimensions of the transformer but can cause the reduction of the ZVS range since the reduction of volume of transformer affects the value of transformer inductance and then of its stray inductance. So another trade-off has to be found to complete the design of the converter.

CHAPTER 4. MODULATION TECHNIQUE FOR PDLC ARCHITECTURE

In the previous chapters the operation of the PDLC topology has been presented and discussed as well as its interesting features, highlighting the main differences with the more common and widespread FDLC solution. In particular, the absence of the intermediate low-pass filter in the architecture allows the improvements of main features as reliability, dynamic response and efficiency of VSI stage, thanks to the ZVT conditions that are provided by the ZP of the Pulsating DC link voltage. Unfortunately, as previously said the operations of the two power stages that constitute the PDLC are strongly coupled, since the fundamental action of large intermediate filter capacitor is absent. Consequently the power stages cannot be operated with independent modulation techniques, as it is usually done with the FDLC topology but more complex modulation techniques are requested. Furthermore the widespread modulation techniques for PSB and VSI stages, as Phase Shifted Modulation, Sinusoidal PWM and Space Vector Modulation cannot be used unless they are deeply modified to obtain the features of PDLC topology. Another issue due to the absence of the intermediate filter capacitor, showed in detail in chapter 2, is that the Zero portions of the Pulsating voltage affects the pole voltage of the VSI stage and consequently the line to line voltages, causing the increase the voltage distortion. This quality degradation of the output voltage is practically due to the undesired introduction of third voltage level which unfortunately is common to all the phases and is controlled by the first stage, acting as a voltage homopolar component.

Regarding the design of the transformer turns ratio we have to say that it is strongly influenced by the type of modulation technique which define the number of ZPs and their duration. These latter “modulate” the Pulsating DC link voltage and consequently cause the reduction of the RMS value limiting the usable DC link for the generation of output voltages. Another parameter that influences the design turn ratio is the ratio between the switching frequency of the two power stages, which is responsible of the amount of the ZPs. Compared with the design of turn ratio for FDLC architecture, the one of PDLC has to be greater to compensate the effects of the ZPs on DC link voltage.

For the above reasons the modulation techniques have to be thought to minimize the effects due to the coupling between the power stages and to achieve a good quality of the output voltages. Moreover, these techniques could be designed to achieve other interesting features as the optimal operation of the Active Clamp and the reduction of switching losses of VSI stage exploiting the commutations during the ZP of the Pulsating DC link voltage.

The interactions between the operations of the PDLC power stages, due to the absence of decoupling element/stage, require the introduction of the synchronization between the operations of the power stages. This characteristic is fundamental for the modulation techniques of the PDLC topology since it permits the control of the position of ZP, avoiding the degradation of the output voltage quality. To achieve this aim, the power stages can be modulated with techniques based on synchronised modulation references or techniques based on the same common modulation references, combining them in different way according to the topology of the stage.

In this chapter the main modulation techniques for the proposed PDLC architecture are presented and evaluated, highlighting the operating principle and its effects on the main features of the converter. In the first paragraphs the main operating principles of modulation will be classified and discussed then the more interesting techniques will be reviewed and compared. In particular different modulation techniques have been analysed including two based on the ZVT of the VSI stage switches, which are proposed and analysed in this thesis work.

4.1 State of the art of modulation techniques for PDLC topology

As previously introduced the PDLC topology needs a unique and global modulation technique, based on the synchronization between the operations of the power stages, to achieve the optimisation of the overall performances of the topology. Consequently the modulation techniques have to be conceived looking at the topology as a single and complex converter, which have to generate AC voltages using an intermediate DC link featured by pulsating evolution. In comparison with the FDLC topology, this is a huge difference since in this latter the power stages and their operating phases are unrelated and independent, allowing the analysis of the single stage. Accordingly the single stage and its working phases can be optimised thanks to common and mature modulation techniques, without requiring particular modifications.

The modulation techniques for the PDLC architecture can be classified, on the basis of the operating principle in the following categories:

- Approximately independent modulation techniques of the power stages: This technique is based on using traditional modulation techniques for the power stages, which are synchronized and characterized by an appropriate phase shift between the carrier signals. This latter feature is fundamental to place the ZP along the voltage period in such a way that their effects on the output voltages are minimized. Furthermore the number of ZP and their width influence the performances of this technique, requiring the introduction of limits on both these two parameters to avoid reduction of performances.
- Technique based on common references for the modulation of both stages: in these techniques the same modulating references are used to define the modulation logic of both power stages. In particular the modulating references of VSI stage are combined in such a way, to define a new reference for the modulation of the first stage that is strongly connected to the operation of the inverter. In this way, not only the synchronization of the operations of the power stages is achieved without effort, but the generation of the Pulsating DC link can be defined to optimise the desired features of the output voltages of the VSI stage. This is an interesting feature of this techniques that will be exploited in the follow paragraphs to show the effects on the modulation technique used for the VSI stage.
- Techniques based on accurate placement of ZP to achieve the ZVT conditions for the VSI stage commutations: To achieve ZVT conditions for the VSI stage, the first stage is modulated to synchronize and displace the ZP of Pulsating voltage in correspondence of the commutations of the VSI stage. Consequently the commutations of all the switches of the Inverter stage are performed with zero voltage applied to the intermediate link, providing ZVT conditions. For this reason in these techniques the driving signals of the first stage are generated after the generation of the VSI signals, since these latter define and influence the modulation pattern of the first stage.

To conclude this classification, we can note that even if the operating principles are completely different, the first two kinds of techniques are featured by the same main aim which is the reduction of the effects of the ZP on the output voltages. In the

following paragraphs it is showed, how these two techniques minimize the effects of the ZP with different principles that provide the same optimal distribution. Instead the last type of technique is completely different from the previous ones, since it is aimed at the reduction of the switching power losses of the VSI stage thanks to appropriate use of the ZPs of the Pulsating DC link.

4.1.1 Approximately Independent Modulation technique

This modulation technique is based on the premise that the power stages of the PDLC can operate as independent converters as presented in [56], using traditional modulation techniques and control schemes. However due the coupling between the power sections of the topology and the pulsating evolution of the DC link, the two modulation techniques have to interface to reduce the effects of the ZPs on the output voltages. To achieve this aim, the introduction of appropriate phase shift between the carrier signals of the two techniques, is essential to ensure the best placement of the ZPs along the evolution of the output voltages. Before analysing the placement of ZPs and the parameters of converter that influence this placement, it is necessary to review few concepts about the three phase VSI stage which can simplify the following analysis. In particular the output phase voltages of VSI stage under PWM is featured by two voltage level, while the line to line voltages present a further voltage level (zero), achieving three levels. According to these features, the Ideal Portion, IP, can be introduced as the voltage portion where all the line to line voltages are zero due to the equality of the phase voltages. Moreover, these particular portions are placed in correspondence of the vertexes of the carrier signal of the second stage. Considering the homopolar nature of the ZPs, as demonstrated in chapter 2, the IPs are the best solution for the placement of the ZPs since they permit zeroing the effects on the line to line voltages. However the output phase voltages are affected by the ZPs, requiring an optimisation of the phase shift between the carrier signals, as showed in [57] to reduce the effects on the quality of the voltage. The parameters that influence the location of the ZPs are the following two:

- The ratio between the switching frequencies of the first stage and the second stage, called P. The switching frequency of the first stage defines the number of the ZPs while the other one define the number of IPs. It is obvious that the number of ZPs cannot be greater than the number of IPs, otherwise the effects of additional portion are not limited. Consequently the value of the ratio P has to be less than the unity to ensure the exact distribution of the ZPs in the ideal portions.

- The width of the Zero Portion. The increase of this latter reduces the effectiveness of the use of the IPs, increasing the degradation of the quality of the output voltages. For this reason this parameter has to be reduced to acceptable values, compatible with the operation of the first power stage which is essentially due to the dead time between the switches of the leg.

Figure 59 depicts the effects of the ZPs on the output voltages, phase and line to line, highlighting the role of IPs and the limit about the value of P. In particular the output voltage are obtained for the case of ratio P =1.

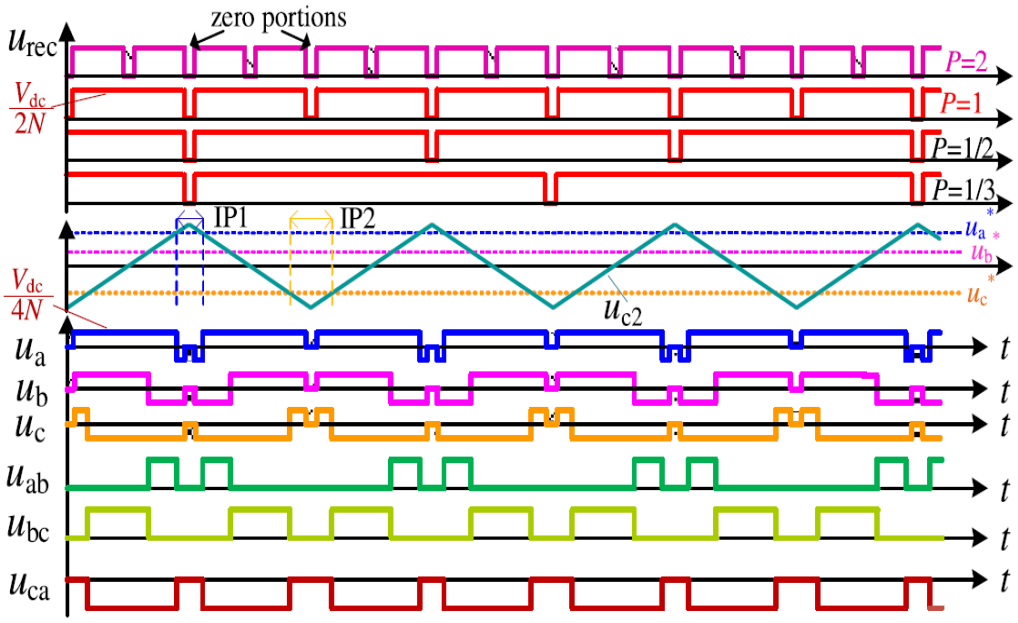

Figure 59 – Example of the effects of ZPs on the output voltages, phase and line to line for different values of the ratio P (photo taken by [56])

The above figure shows the fundamental role of the IPs in the reduction of the effects of the ZPs on the output voltage for values of P that are less than or equal to one. Instead in case of P greater than one, there aren't enough IPs to place all the ZPs, with the consequent degradation of the output voltage due to the effects of the portions in excess. Consequently the value of P is the main constraint in the design of this modulation technique, which influences both the power stages.

4.1.2 Techniques based on common modulation references for both the power stages

The power stages of the PDLC topology are controlled with modulation techniques that have in common the same modulation references, which are used in different ways

to achieve the desired performances for each power stage. In particular the common modulation references, which are usually used in these techniques, are the ones of the VSI stage due to the main role of this stage and the difficulties to control this stage with a combination of references of a DC/DC power stage. To control the first stage, these references are mixed in such a way to obtain a particular modulation reference which takes in account the dynamic of the modulation of VSI stage. In this way the interaction between the two modulation techniques is exploited to improve the features of the single technique as the reduction of switching losses. In the following subparagraphs, two different techniques based on the presented operating principle are reviewed and discussed. In particular they make use of the same particular modulation technique for the VSI stage while two different versions are used for the first stage. They provide different effects in the global technique.

4.1.3 Discontinuous Pulse Width Modulation technique

This modulation technique exploits the ZPs of the Pulsating DC link as the free-wheeling portions for the modulation of the VSI stage, as proposed in [58]. To achieve this aim a particular Sinusoidal PWM technique, called 120° Discontinuous PWM (DPWM) is used. It is based on the commutation of single leg for switching period while the other two are clamped at high or low voltages. This particular operating principle allows the reduction of the switching losses of the VSI stage of three times, since just one leg is commutated at the switching period. The definition of the driving signals of the legs is based on the results of the comparison of the voltage references. Specifically, considering the high side switches of the three legs of VSI stage, the modulation logic keeps high the switch relative to the maximum voltage reference and keeps low the one relative to the minimum voltage. Instead the switch related to the last references, which is located between the others two, is modulated at the switching frequency. Figure 60 reports the modulating references and the driving signals of the high side switches of the three leg, obtained with the operating principle just introduced.

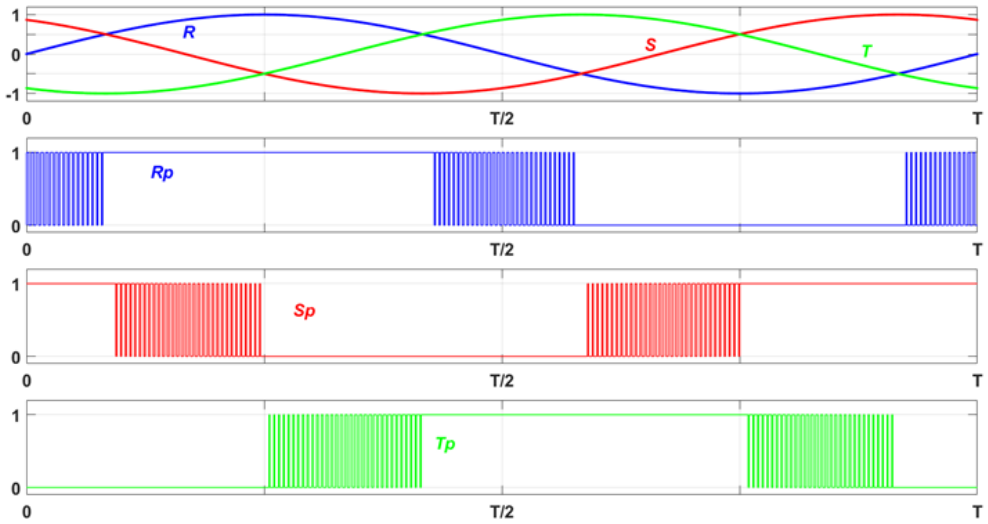

Figure 60 – Modulating references and driving signals of the 120° Discontinuous SPWM

Regarding the modulation of the first stage and the definition of the shape of Pulsating DC link, the sinusoidal references of the VSI stage are compared with triangular carrier signal. The results of these comparisons are combined to distribute the ZPs of the DC link, along the output voltages in optimal position where the effects of these latter are minimized. Consequently this technique achieves the same aim of the previous modulation technique, using a different operating principle that has an impact on the single modulation of the power stage. Figure 61 reports the logic schematics, extracted from the paper [58], which shows the implementations of the operating principle previously described.

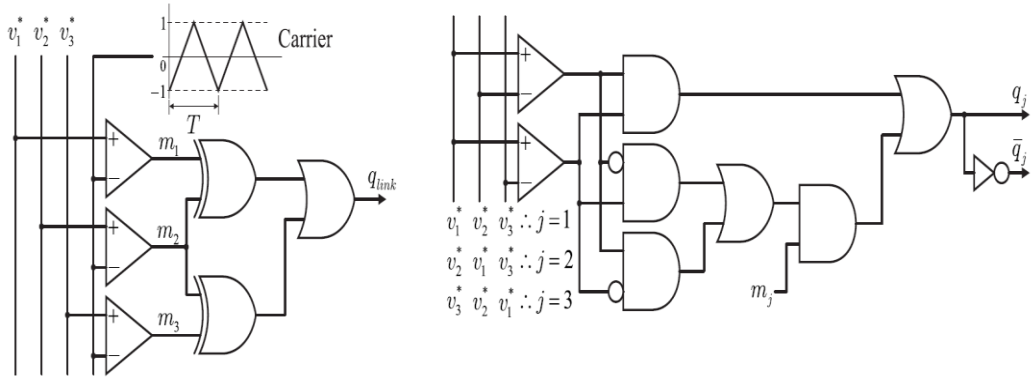

Figure 61 – Logic schematics for the modulation of the first stage(left schematic) and for the VSI stage (right schematic)

From the two schematic of the above figure, we can note that they not only share the modulating references but also the carrier signal, which is necessary to modulate the only leg that is commutated in the discontinues PWM of the VSI stage. It is worth to note that in the scheme on right, the signal m_j is the result of the comparison between the carrier signal and the modulation signal. Consequently, it is avoided to report the carrier signal in this scheme.

Instead Figure 62 reports a detail of one switching period of Figure 60, to show the operation of the VSI stage. Moreover, together with the driving signals of the Inverter stage, the Pulsating DC link voltage is depicted to highlight the positions of the ZPs.

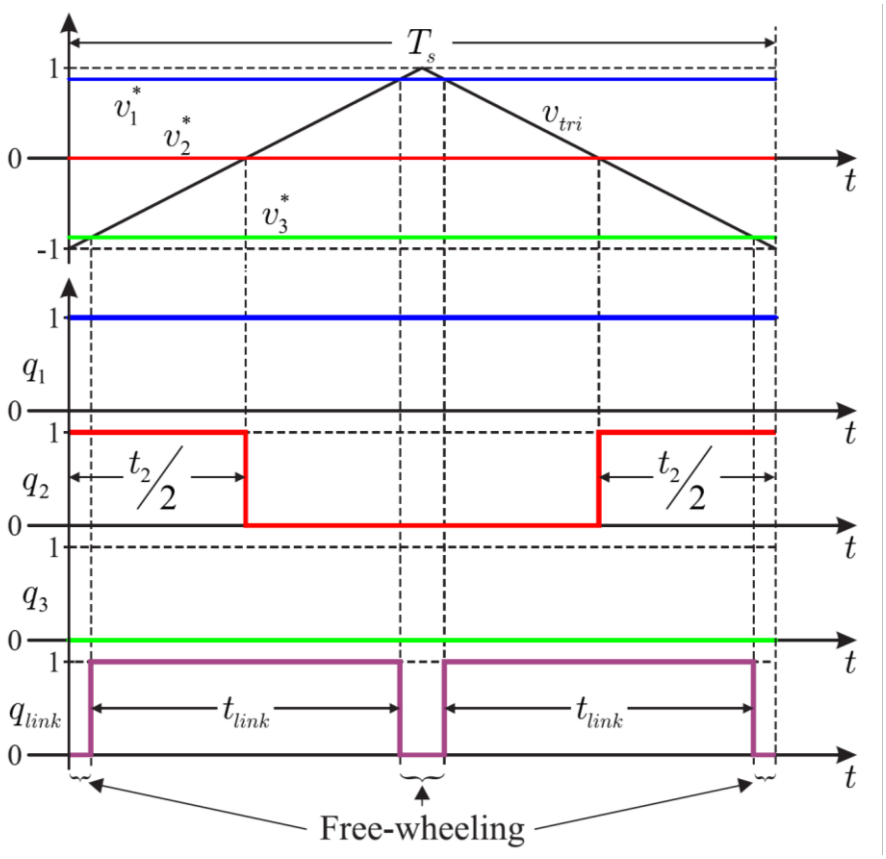

Figure 62 – Detail of the generation of driving signals (q1, q2 and q3) for the VSI stage and the relationship with the pulsating DC link (qlink). (photo taken by [58])

The above figure presents the operating principle of the VSI stage and shows the commutation of just one leg at the switching period. Moreover it presents the evolution of the carrier signal and Pulsating DC link, called q_{link} in the figure, and shows that this modulation technique has the same principles seen in the previous chapter for the placement of the ZPs of the voltage. Consequently this modulation technique allows the reduction of the effects of the ZPs on the quality of the output voltages, as well as

the reduction of the switching losses of the VSI stage thanks to the discontinuity of the PWM.

4.1.4 Single reference six pulsed modulation technique

This modulation technique presented in [59], also called Single reference six pulsed modulation makes use of a different technique for the modulation of the first stage while for the VSI stage uses the same discontinuous PWM technique analysed before. However in this case the driving signals are obtained by the comparison of triangular carrier signal with a modified sinusoidal references, which are characterized by two clamping phases, one high and the other low defined to reduce the number of commutations. Regarding the single reference for the first stage, it is achieved calculating the maximum value of the modulating references without modifications, expressed in absolute value for all the fundamental period of the voltage. In this way the voltage reference is featured by a frequency equal to six time the fundamental frequency, which is compared with a carrier signal to define the logic modulation of the first stage. Table 5 reports the switching state of each leg of VSI stage for the six different sectors of the voltage reference.

Table 5 Switching state of VSI stage under the Discontinuous PWM

	T1	T2	T3	T4	T5	T6
Leg S	V_{ab}/V_{cb}	1	1	V_{ac}/V_{bc}	0	0
Leg R	0	0	V_{bc}/V_{ac}	1	1	
Leg T	1	V_{cb}/V_{ab}	0	0	V_{ca}/V_{ba}	1

Figure 63 shows the equivalent modulating references used for the discontinuous PWM and the single voltage reference for the first stage together with the driving signals for the high side switches of VSI's legs.

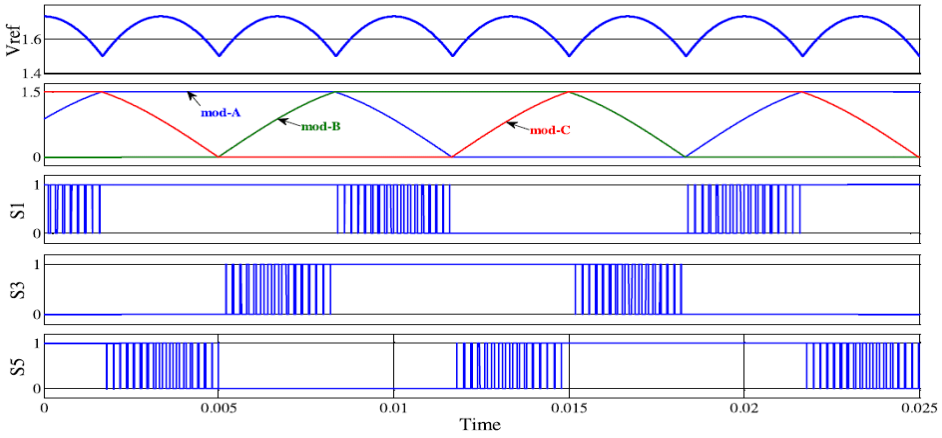

Figure 63 – Equivalent modulating references for the first stage (first plot), for the VSI stage (second plot) and the driving signals for the high side switches (figure taken from [59])

4.1.5 Techniques based on the soft-switching of the VSI stage

The modulation techniques presented in this paragraph are aimed at the reduction of the power losses and consequently the increase of the efficiency of the PDLC topology, thanks to the achievement of soft-switching conditions for the VSI stage. To reach this aim, these techniques are based on the synchronization of the commutations of the switches of the Inverter stage with the positions of the ZPs of the pulsating DC link, to guarantee that all the commutations happen when the voltage of DC link is zero. Consequently, all the commutations of the VSI stage are performed in ZVT thanks to this original use of the ZPs. The presented feature requires that the modulation logic of the first stage is completely dependent and coordinated with the modulation technique of the VSI stage. In this way the first stage defines the position and width of the ZPs on the basis of the implemented switching pattern of the Inverter stage, achieving the ZVT condition. This feature could be assimilated to the main one of previous modulation techniques, based on the use of the same references for both the power stages but the effects of the VSI stage on the driving pattern of the first stage are more stringent.

A first example of such a kind of modulation technique has been presented [43] by the researchers of “Laboratorio di Elettronica Industriale - G. D’Angelo” of the University of Cassino and Southern Lazio.

This modulation technique is based on a particular use of the ZPs of the Pulsating DC link which is completely different and innovative compared to the other analysed techniques. In particular the considered modulation technique, is thought and implemented to ensure the synchronization between the commutations and the position

of ZPs, providing the ZVT conditions for all the switches of VSI stage. To accomplish this aim the operations of the first stage, responsible of the generation of Pulsating voltage, are completely determined and controlled by the modulation technique of the VSI stage. Consequently the switching frequencies of the two sections of this technique are strictly related, imposing a constraint on the design of both the power stages and the achievable features. The switching frequency of the first stage is not assigned but is obtained as a result of the particular operating principle which causes the frequency to become twice the frequency of the Inverter stage.

The algorithm of the modulation technique starts from the three phase PWM necessary to obtain the three phase output voltage. To modulate the VSI stage, the analysed technique uses a traditional Sinusoidal PWM technique which is slightly modified to be suitable for the desired feature of the PDLC topology. Specifically the implemented SPWM technique is featured by the following two adjustments:

- The driving signals are controlled to eliminate the pulses with width less than few microseconds (2/3us), to avoid unrealizable commutations for the IGBTs that are used in the stage. Consequently the control causes the clamping high or low of the driving signals in correspondence of the peak of the modulating references. Moreover, the number of commutations of each switch are reduced, allowing the reduction of the relative switching losses.
- To avoid simultaneous or nearly simultaneous commutations of the legs, which can give problems to the particular operating principle of the analysed technique, the modulating references are pre-distorted with a step. This step is added in proximity of the crossing points of the references, altering the shape of these latter in such a way that simultaneous commutations of the switches are avoided. Figure 64 shows the modulating references of the VSI stage, after the application of the predistortion technique.

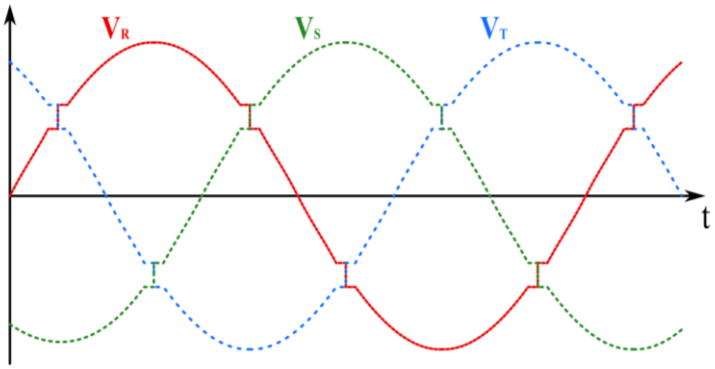

Figure 64 – Pre-distorted modulation references of the VSI stage to avoid simultaneous commutations

Once the modulation logic has defined the PWM gate signals of the VSI switches, it generates the driving signals for the PSB switches in order to guaranty a Zero voltage Phase of the PDC-Link during which the VSI switches are switched. That means that before each turn on and turn off the VSI switches one switch of the PSB stage is turned off to cause a freewheeling phase which is closed by the turn on of the other PSB switch right after the commutation of the VSI stage is accomplished. In other words, to guaranty ZVT of the VSI stage, the modulation logic is designed to ensure that each commutation of the VSI switches is preceded by the commutation of a switch of the PSB stage and followed by a commutation of the other switch in order to realize a ZP on the DC link. In this way the power stage can be controlled to start the ZP of the Pulsating voltage before the change of the switching pattern of the VSI stage. Figure 65 depicts the operation of the modulation technique.

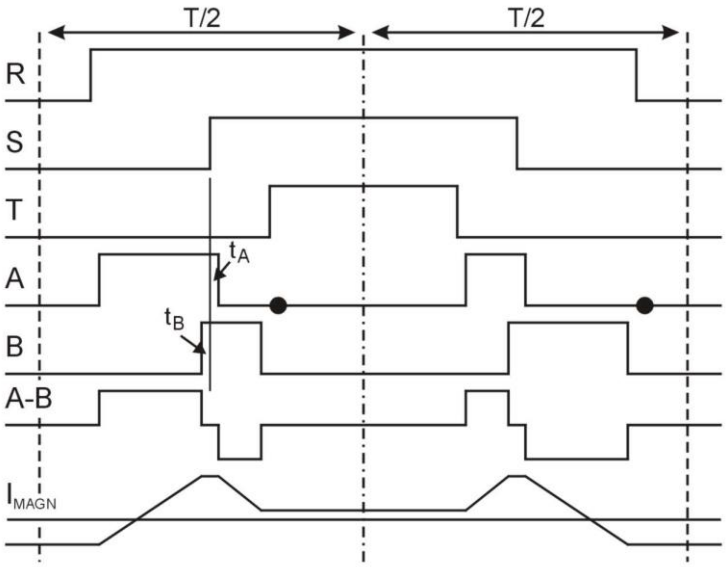

Figure 65 – Operations of the analysed modulation technique

In particular, the first three waveforms of Figure 65 represent the control signals of the high side switches of R, S and T phases, respectively. Fourth and fifth waveforms refer to the control signals of high side switches of legs A and B of the PSB stage, respectively. Sixth and seventh waveforms are the idealized waveforms of voltage and magnetising current of the transformer, respectively. The dead times of the switches of each leg are neglected in the figure. The control signals of the VSI stage are conceived to be symmetric with respect to their central time at each period of the VSI PWM. Figure 65 refers to a complete cycle of a VSI switching period where the R phase requires more energy than the S phase which in turn requires more energy than the T phase. The cycle starts with the energising phase involving the R phase. Before the turn-on the S switch, the low side switch of the B leg is turned off to close the previous energising phase and to cause a freewheeling phase which is closed by the turn-off of the high side switch of the A leg. Then a new energising phase is started involving the S phase which is closed when the switching of the T phase is requested. Before the turn-on of the T switch, the high side switch of B leg is turned off to cause a new freewheeling phase where T switch is switched at zero voltage. In summary we can say that every single commutation of the VSI leg is anticipated by a change of the switching pattern of the first stage, which provides the ZVT conditions for the commutation of the VSI stage. It is worth to note that the symmetry of R, S an T control signals guaranties that the energising phase of each VSI stage is followed by an energising phase with the same duration but opposite sign involving the same leg. This is very important to avoid a DC components of the magnetising current which could saturate the transformer core. To conclude the description of the modulation algorithm we have to say that the Active Clamp is turned on right after the start of each energising phase and it is turned off before its end, in such a way to limit the voltage overshoot, as discussed in the previous chapter. The control signals of the active clamp is omitted in Figure 65 to simplify the figure.

4.2 Proposed modulation technique

The modulation technique presented in this paragraph was originally conceived by the researchers of the “Laboratorio di Elettronica Industriale” of University of Cassino. It has been analysed and characterised in this work. Like the technique described in the last section of the previous paragraph, the technique is conceived to exploit the ZPs of the DC link to achieve ZVS of the VSI switches [60]. In addition two different independent switching frequencies can be used for the PSB and VSI stages. This is an

important feature of the proposed modulation technique. In fact the switching frequency of the first stage can be increased to reduce the transformer's dimensions while the frequency of the second stage is designed to fulfil harmonic constraints on the output voltage. Consequently, the limit on the ratio between these two frequencies prevents the trade-off between the features of the stages since the frequencies ratio is discretized, minimizing the possible design combinations. Instead the proposed modulation technique [60] combines soft-switching of the VSI stage, with the possibility to use unrelated and independent switching frequencies for the modulation of the power stages. Consequently, the constraints due to the ratio of the frequencies and its effects on the design are eliminated, allowing the optimization of the operation and features of each single power stage of the topology. As the previous technique, even this one starts with the modulation of the VSI stage and then it defines the switching patterns of the first stage, which are strongly influenced by the operation and commutations of the VSI stage. Therefore the proposed modulation technique generates the driving signals for the VSI stage using a Discontinuous Pulse Width Modulation (DPWM), the same one used in the previous paragraphs. In this way a good distortion of the output waveforms can be ensured and all the interesting features of the Pulsating DC-link architecture can be exploited. Afterwards the driving signals for the PSB stage are provided taking in account the main parameters of this power stage (i.e switching frequency and deadtime) and the control signals of the VSI stage (synchronization of the power stages). Thanks to this implementation based on the results of the VSI modulation, the technique ensures that all the commutations of VSI stage take place during the freewheeling phases of PSB stage (ZVT conditions). Figure 66 shows the normalised modulating references, in the top plot and all the driving signals of the power stages of the PDLC topology. The order of the signals in the representation is not casual but it is due to how the proposed modulation technique provides them chronologically.

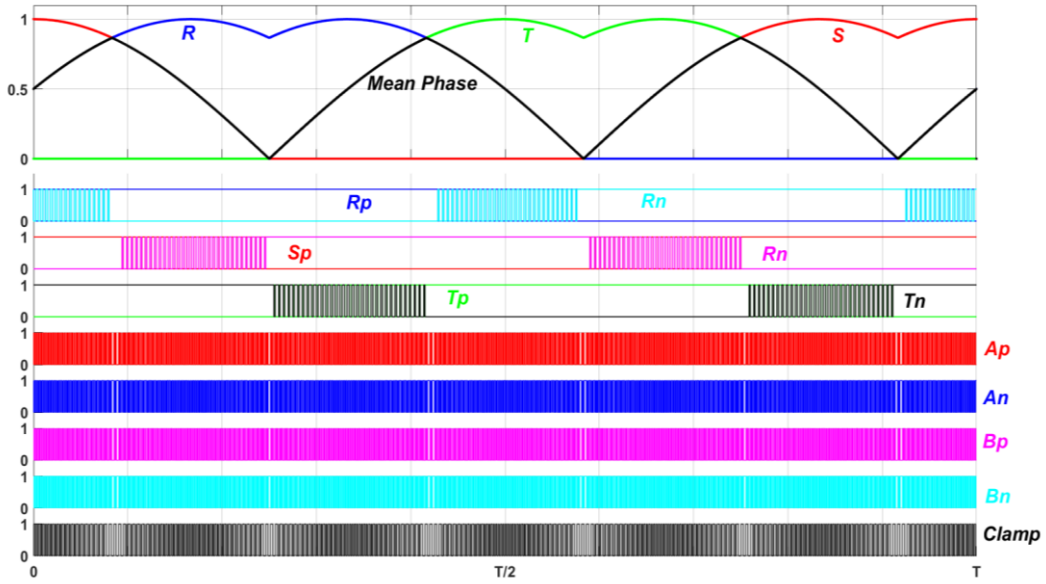

Figure 66 – The operating principle of the proposed modulation technique

To provide more details about the modulation operating principle, Figure 67 reports a zoom of all the driving signal of the topology in the time interval highlighted with a red rectangle in the normalised modulation references plot.

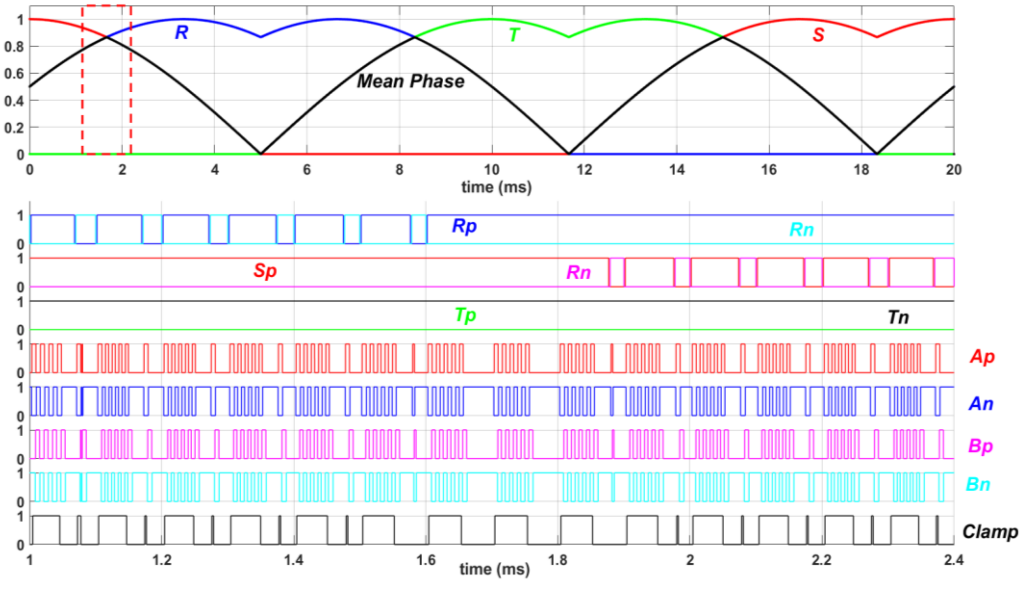

Figure 67 – Details of the operating principle in the time interval highlighted in the top plot

The output period (=20ms) is subdivided in six intervals. In each of them one phase of the VSI is requested to supply the larger voltage, the second one the intermediate voltage and the third one can be kept to zero voltage (low side switch in the on state) exploiting the symmetry the three-phase voltage to get the proper sinusoidal voltage

at the corresponding output terminal. Consequently, the DC-link must supply energy only to the first two VSI phases. The modulation logic keeps the high side switch of the larger voltage phase in the on state during the whole interval in which the phase is requested to supply the larger voltage. Instead the high side switch of the intermediate voltage phase is commutated at the frequency of the VSI stage, fs_{VSI}. When this latter switch is on the energy is transferred to both larger and intermediate voltage phases; when it is off the energy is transferred only to the larger voltage phase. The modulation procedure computes the time durations E1 and E2 of these two energizing phases starting from the modulating signals of Figure 67 taking into account a modulation index which can be varied to regulate the output voltage. The operation principle is depicted in Figure 67. Initially and up to 1.6ms, Sp (the high side switch of the S phase) is in the on state during the time interval for which the S phase holds the larger voltage. Afterword, Rp is on because R becomes the larger voltage phase. It is worth to note that during each time interval only the switches of the intermediate voltage phase are commutated at the frequency of the VSI stage, fs_{VSI}, whereas the other switches are commutated with a frequency comparable with the line frequency. This helps in further reducing the switching losses of the VSI stage for which the turn-on is at ZV as discussed below. To reduce the voltage area across the primary side of the transformer, the time durations E1 and E2 of the PSB powering phases can be subdivided in several time intervals in such a way to increase the frequency seen by the transformer and to reduce its magnetizing inductance, and then, its volume and weight. As usual the PSB switches are commutated with 50% duty cycle. The shift between the two PSB legs is computed in order to subdivide the energy to be supplied to the VSI stage in several pulses. The number of this pulses must be even to permit the complete demagnetization of the transformer during each powering phase. This number can be used to get a trade-off between the distortion of the output voltage and the switching losses of the PSB stage as demonstrated below. It is worth to outline that the proposed modulation procedure is conceived to cause a free-wheeling phase of the PSB before each powering time interval in such a way to zero the voltage on the DC-link and to allow ZVT of the VSI switches commutated between two subsequent powering phases. This feature of the modulation can be observed in Figure 68, where a further detailed zoom (comparable with two switching periods) of Figure 67 is provided and the ZVT conditions for the VSI switches are highlighted. Moreover, the clamp switch Sac is turned on during the first pulse and turned off during the last pulse of each powering phase in such a way to recirculate the energy transferred to Cac during the voltage overshoot.

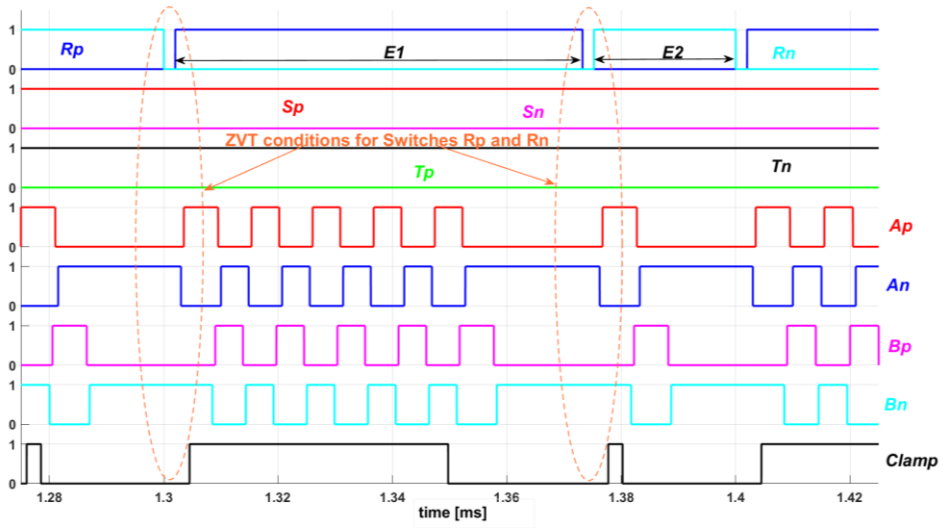

Figure 68 – Detailed zoom of the driving signals of all the switches.

To conclude, it is worth to note how the operation of the Active Clamp in the proposed technique is quite different from the one analysed in the previous paragraph. Consequently, due to this different use of the circuit the analysis performed in the section 3.1 is no more applicable, requiring a further investigation. For this reason in the following paragraph, the proposed operation of the Active Clamp is investigated and the effects on the power converter features are provided thanks to the use of simulation tool.

4.2.1 Details of the operation of the Active Clamp circuit

In the modulation technique described in section 4.1.5, the Active Clamp circuit is synchronised with the energising phase of the PSB stage in such a way that the clamping capacitor is connected to the pulsating DC link only during the energising phase. Instead, in the latter modulation technique, the switch of the Active Clamp circuit is turned on during the first energising phase and is turned off during the last energising phase, consequently the clamp capacitor is connected to the pulsating DC link during all the intermediate energising phases of the VSI switches. This means that, during these energising phases, the first stage of the PDLC acts as an isolated DC/DC converter with a capacitive output filter, which holds up the voltage on the Pulsating DC link during the energising phases. The value of the capacitor strongly influences the dynamic response of the PDLC since this capacitor must be charged/discharged at the variation of the rail voltage. In particular, large currents are requested during the start-up phase of the converter to charge the clamping capacitor until the steady state

value of the PDC link voltage is reached. The current in the clamping capacitor is limited by the stray inductance of the circuit which includes the stray inductance of the transformer that represents its largest contribution. The peak current in the clamping capacitor becomes reasonably small when its steady state voltage is reached and the voltage across the stray inductance is minimized. It is worth to note that the PSB switches are still soft switched thanks to the energy stored in the stray inductance. The minimum load current at which ZVS are possible in the considered case is larger than the minimum current necessary for the soft switch of the previous case where the switching of the PSB switches can exploit the energy stored in the large inductance of the output filter. The problem would be solved if the clamp switch were turned on only during the energizing phases and therefore at double the frequency of the switches of the PSB stage. This would be possible if we used the much faster SiC MOSFETs with lower rated current considering the low currents involved in the charge and discharge of the clamp capacitor.

In our case we preferred to operate the active clamp switch at the frequency of the VSI stage in order to exploit the advantages of a lower frequency of the VSI stage.

Figure 69 represents the schematic of the PDLC equivalent circuit during the high frequency energising phases:

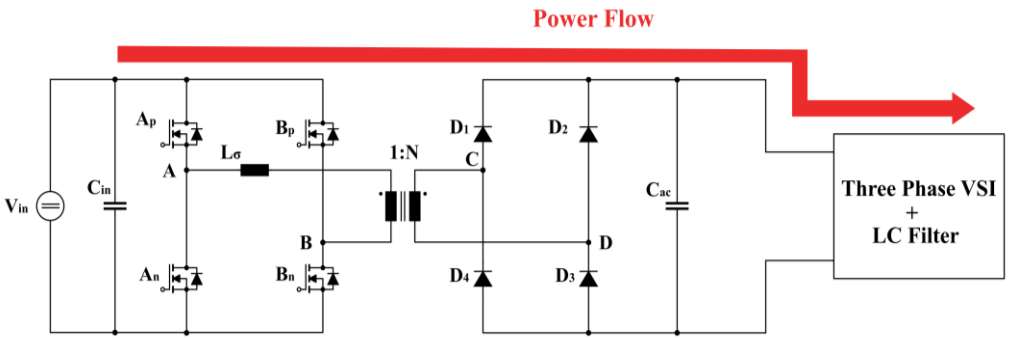

Figure 69 – Equivalent schematic of the PDLC during the energising phases

To investigate the effects on the converter of the new operation of the Active Clamp, LTSpice simulation has been performed in different test conditions, using the schematic circuit already used for Figure 42. Figure 70 reports the waveforms of the driving signals of the leg R of the VSI stage, the voltage on the primary side of the transformer and the Pulsating DC link voltage for P_{OUT}= 10kW, V_{IN}= 600 V, fs_{PSB} = 60kHz (PSB switching frequency), fs_{VSI} = 10kHz (VSI switching frequency) and C_{ac} = 220 μF.

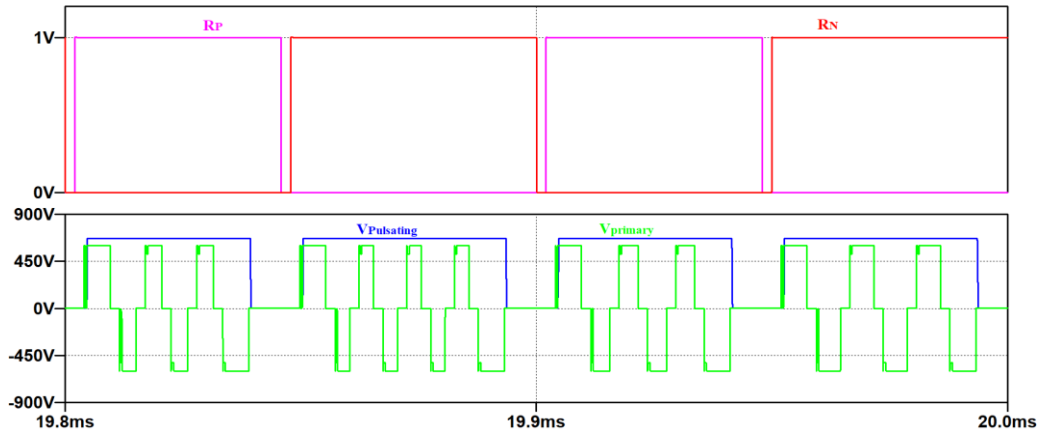

Figure 70 – Detail of the driving signals of the VSI leg R (top plot), Pulsating DC link voltage (blue) and voltage on the primary of the transformer for P_{OUT}= 10kW, V_{IN}= 600V, fs_{PSB}= 60kHz and fs_{VSI}= 10kHz.

We can note that the commutation of the leg R (mean phase) happens in the ZPs of the Pulsating DC link voltage which are only two for period of VSI stage thanks to the operation of the Active Clamp. Moreover, another effect of the operation of Clamp is that the frequency of the Pulsating DC link is set to twice the frequency of the VSI stage, even if the PSB stage is working with higher switching frequency (60 kHz).

As introduced before, the role of the Clamp capacitor in the proposed technique is different from the one analysed in the previous section. Connected to the output of the first stage for the entire energising phase, the Clamp capacitor acts as an output filter capacitor and participates to the energy transfer from the source to the load. In particular, this capacitor is charged when the PSB stage provides the energy pulses and it supplies the load, during the short freewheeling phases between two consecutive energy pulses. To show the behaviour of the Clamp capacitor, Figure 71 reports the waveforms of voltage and current in the capacitor, the Pulsating DC link voltage and the current on the primary side of the transformer in the same test conditions of the previous figure.

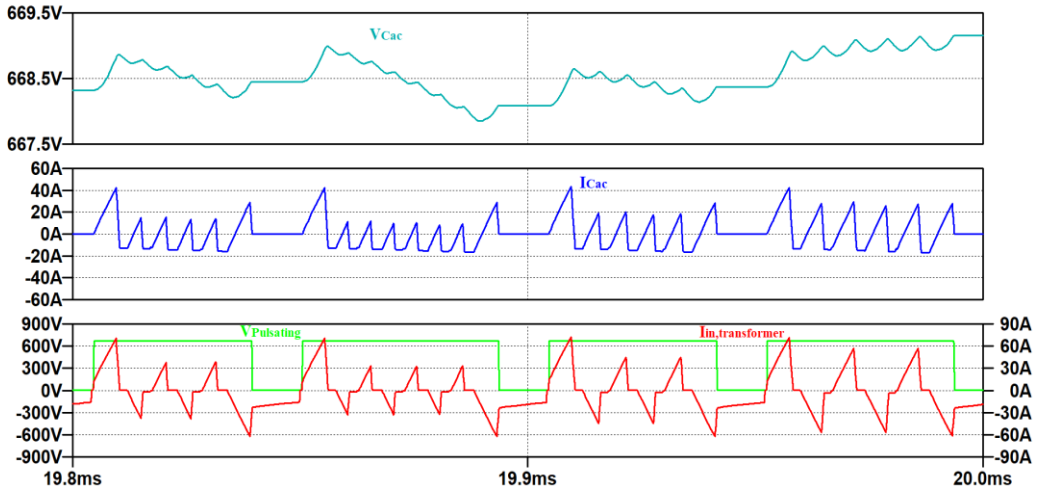

Figure 71 – Detail of the voltage(top plot) and the current on the Clamp capacitor (middle plot), the current on the primary of the transformer and the Pulsating DC link voltage (bottom plot) for P_{OUT}= 10kW, V_{IN}= 600V, fs_{PSB}= 60kHz and fs_{VSI}= 10kHz.

We can note that in every energising phase, the first and last pulses have higher current peaks than the intermediate ones. This is due to the larger width of these two pulses, since the active Clamp switch is switched during these two pulses. Moreover, these two wider pulses allow a faster charge of the capacitor, permitting the reduction of the current peaks of the intermediate pulses.

Figure 72, Figure 73 and Figure 74 report the waveforms of the Pulsating DC link voltage and the current on the primary side of the transformer in the same test conditions of the previous figure, for values of the Clamp capacitor of 500nF, 5µF and 220µF, respectively.

Figure 72 - Detail of the current on the primary side of the transformer(red) and the Pulsating DC link voltage (green) for P_{OUT}= 10kW, V_{IN}= 600V, fs_{PSB}= 60kHz, fs_{VSI}= 10kHz and C_{ac}= 500 nF.

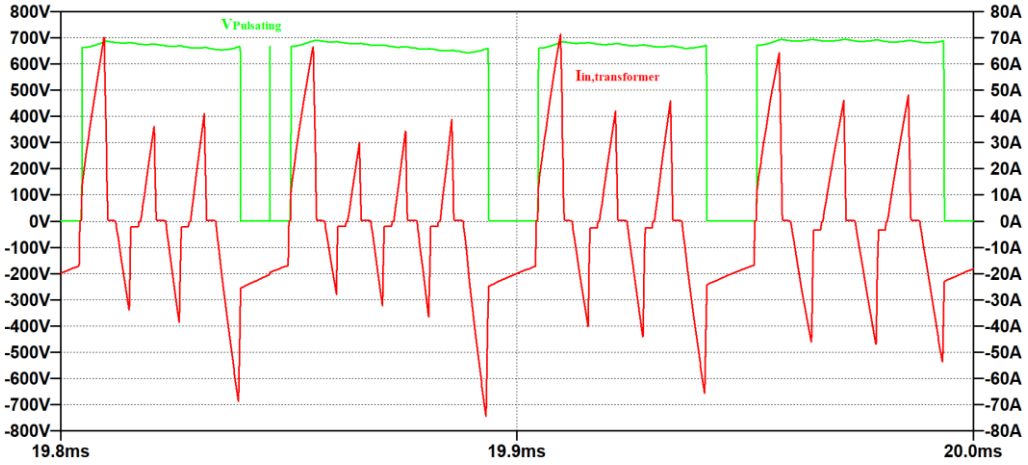

Figure 73 – Detail of the current on the primary side of the transformer(red) and the Pulsating DC link voltage (green) for P_{OUT}= 10kW, V_{IN}= 600V, fs_{PSB}= 60kHz, fs_{VSI}= 10kHz and C_{ac}= 5uF.

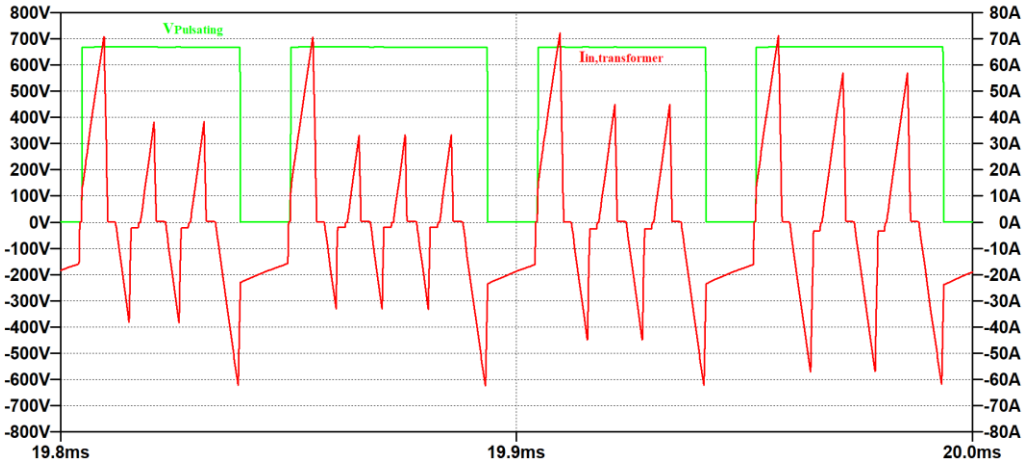

Figure 74 - Detail of the current on the primary ide of the transformer(red) and the Pulsating DC link voltage (green) for P_{OUT}= 10kW, V_{IN}= 600V, fs_{PSB}= 60kHz, fs_{VSI}= 10kHz and C_{ac}= 220 uF.

The comparison of the last three figures indicates that the variation of the Clamp capacitor involves the following two aspects:

- The reduction of the clamping capacitor causes a reduction of the stabilizing effect on the Pulsating DC link voltage during the energising phases, showing a voltage transient due to the charge and discharge of the clamping capacitor. These voltage transients don't affect the output voltages and the load, since they happen at high frequency that are filtered by the three-phase output filter.
- The value of the Clamp capacitor influences the current peak of the current on the primary of the transformer. In particular the reduction of the capacitor produces a decrease of the peak since it needs less current for the charging.

Consequently, the sizing of the Clamp capacitor can be used to get a trade-off between the steady state characteristics and the dynamic performances (start-up and transient) of the converter.

4.2.2 Predistortion technique of modulating references

As showed before the proposed modulation technique and its implementation is mainly reliant on the demanded power from electrical load. For low output power the pulsating evolution of DC link voltage affects the quality of output voltage causing a distortion for which some harmonics, especially at low frequency, can overcome the pollution limits. This lack of the technique can be significantly reduced by the predistortion of the modulating signals adding to the sinusoidal reference a weighted sum of harmonics components. Thanks to this weighted predistortion, the output voltage distortion can be compensated to comply with the harmonic pollution limits. To find the compensating components and the related weights a recursive procedure, based on the harmonic analysis of the output voltage, has been implemented. At each step, a frequency analysis of the simulated output voltage is performed to compute the weight factors for the compensation of the harmonic components, that will be used in the subsequent step. The recursive procedure is repeated until the best combination of the harmonic weights are found and consequently the distortion is minimized. Figure 75 shows the flow chart of the procedure used for the implementation of the predistortion technique of the modulating signals.

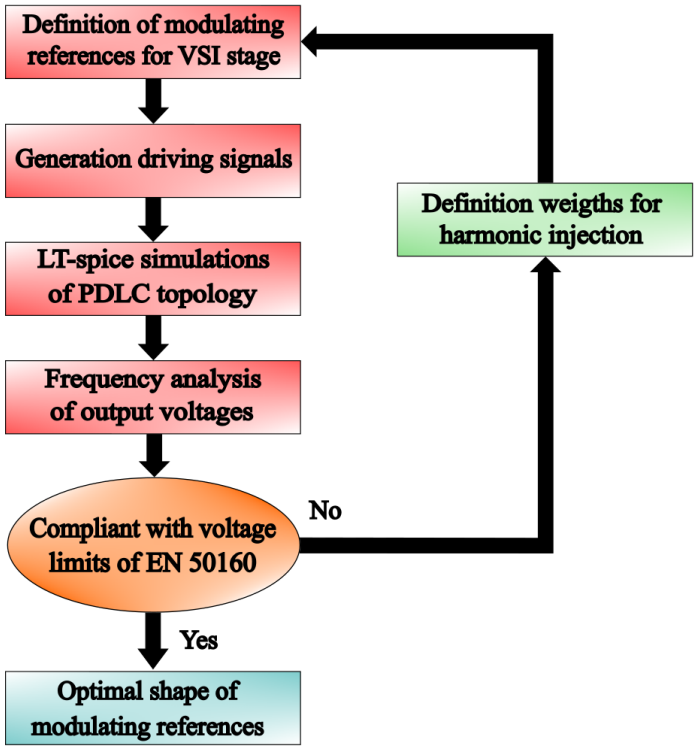

Figure 75 – Flow chart of the iterative procedure used for the identification of the voltage harmonics and the relative weights, necessary for the predistortion technique

The operation of harmonic injection is performed adding algebraically the uncompliant harmonics modulated in amplitude through the weights to the modulating references of the VSI stage. The harmonic considered in this analysis are the odd harmonics at very low frequency as the 5^{th}, 7^{th}, 11^{th} and 13^{th}, which present strict harmonic limits.

This method can be applied to different values of output power to achieve best distortion performances of the converter in all the power range. Figure 76 depicts the effects of the predistortion technique on the normalised modulating references, comparing them with the references without the harmonics injection.

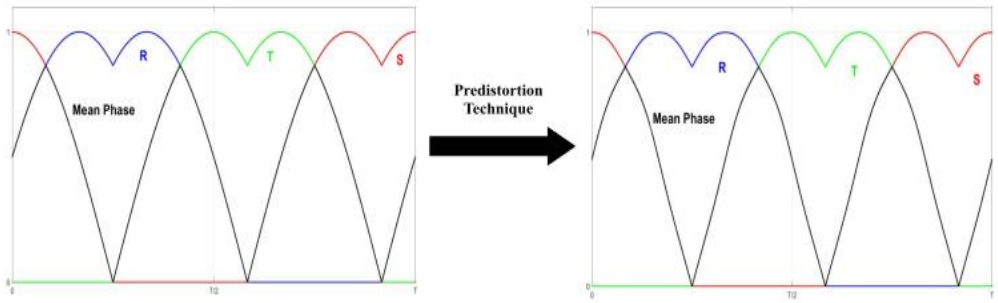

Figure 76 – Normalised modulating references (on the left) and references after the predistortion technique

To demonstrate the features of the proposed modulation technique and the benefits of the predistortion, LTSpice simulation has been performed in different test conditions. Figure 77 and Figure 78 report the waveforms of line to line output voltage without (solid blu lines) and with the predistortion of modulating signal (dashed red lines) for fs_{PSB} = 60kHz. The test conditions are: P_{OUT}=4.1kW, V_{IN}=700V, and P_{OUT}=14kW, V_{IN}=600V, for Figure 77 and Figure 78, respectively. We can observe that the injection of weighted harmonics in the modulating signals allows us to improve the shape and the quality of the voltage in both cases.

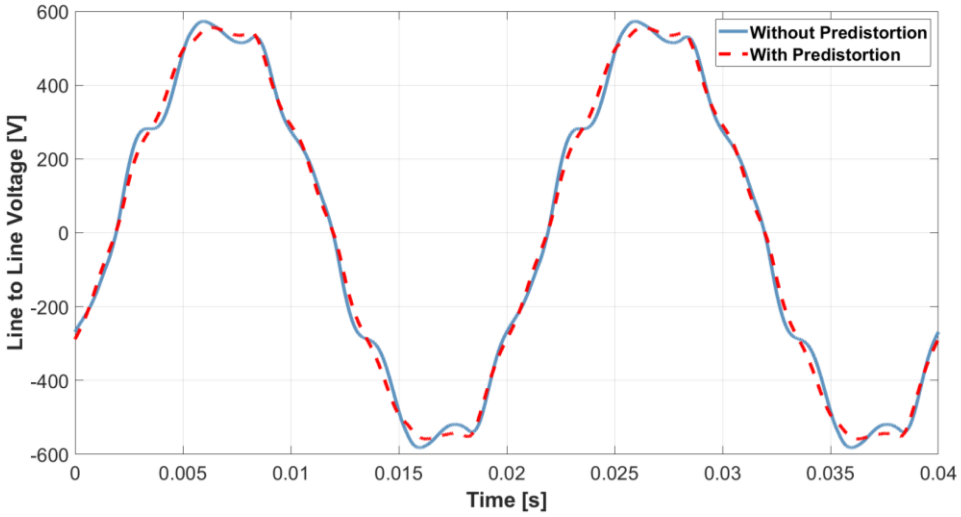

Figure 77 – Output voltage of PDLC for resistive load of P_{OUT}=4.1kW, V_{IN}=750V and fs_{PSB}=60kHz with and without predistortion.

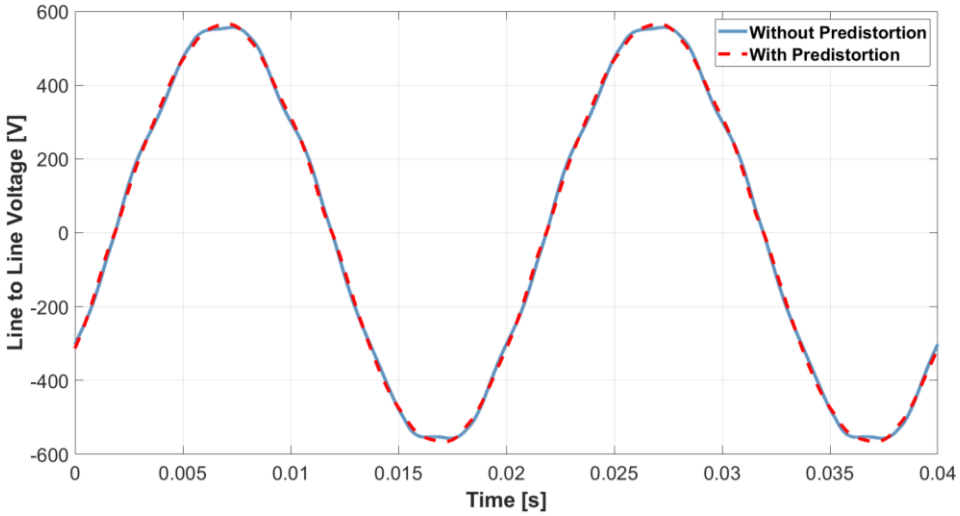

Figure 78 – Output voltage of PDLC for resistive load of P_{OUT}=14kW, V_{IN}=600V and fs_{PSB}=60kHz with and without predistortion.

In particular, in the low output power case, the predistortion permits the reduction of the undesired low frequency oscillation around the peaks of the waveforms. To complete the study of the effects of the predistortion, the analysis of the output voltage has been performed for different values of PSB switching frequency. In Figure 79 and Figure 80 the simulated Total Harmonic Distortion, THD, is reported as a function of the switching frequency of the PSB stage, fs_{PSB}, in the cases without and with predistortion, for two values of resistive output power, namely 5kW and 15kW.

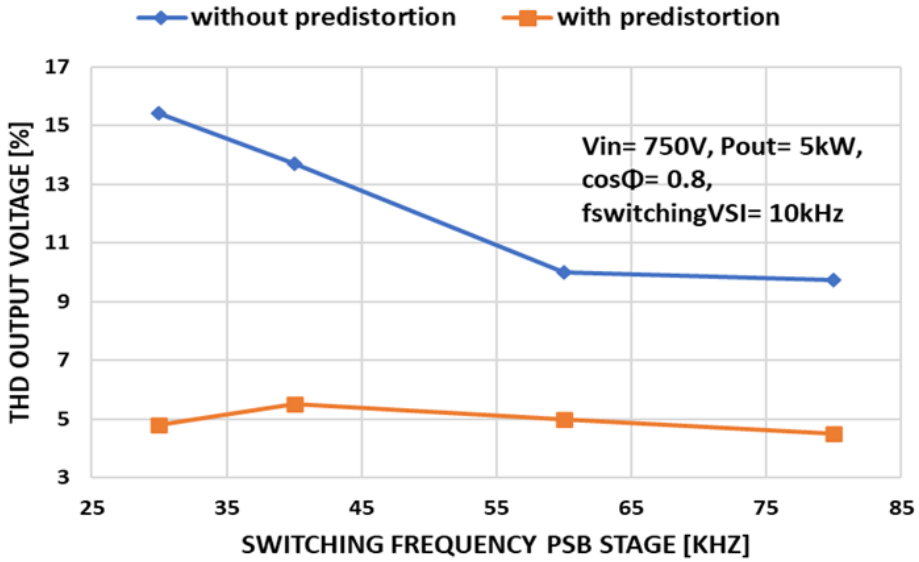

Figure 79 – THD obtained by LTspice simulations vs. PSB switching frequency in the cases without (blue) and with (orange) pre-distortion, for resistive load of P_{OUT}=5kW.

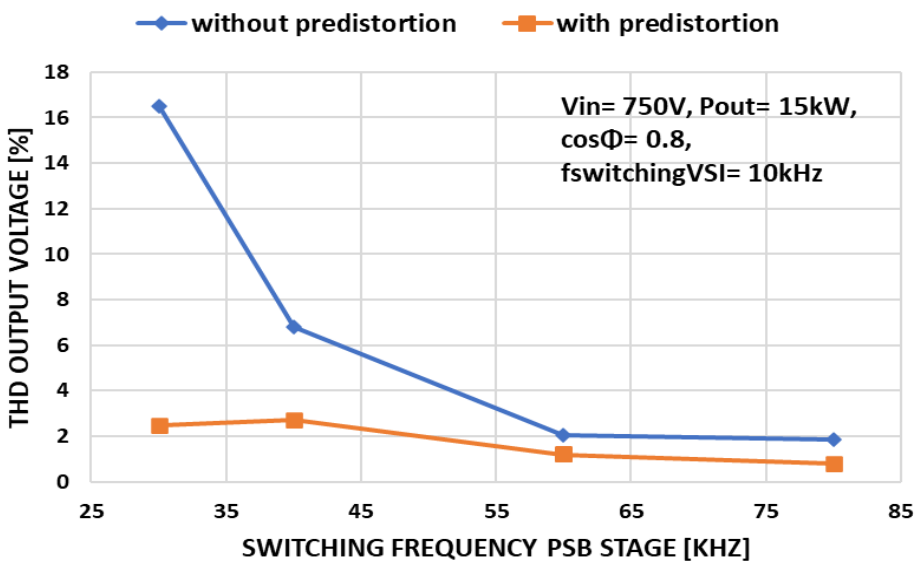

Figure 80 – THD obtained by LTspice simulations vs. PSB switching frequency in the cases without (blue) and with (orange) pre-distortion, for resistive load of P_{OUT}=15kW.

In both cases without pre-distortion, THD starts from a large value and significantly decreases with the increase of both fs_{PSB} and output power. The predistortion significantly mitigates the dependence of THD on fs_{PSB} and allows THD lower than 5% even at low output power. It is worth to outline that the predistortion modulation technique makes the THD practically independent of the switching frequency allowing very low values of THD even at relatively low switching frequencies with large advantages in terms of power devices energy dissipation.

The modulation technique was implemented as a MATLAB© routine whose results are supplied as input to both LTspice, for achieving circuit simulation of the PDLC, and an FPGA Altera board which provides the signals to the drivers of the switches guaranteeing the appropriate timing including the dead times. This latter feature will be described in the next chapter, providing more details of this particular implementation.

CHAPTER 5. EXPERIMENTAL CHARACTERIZATION OF PDLC PROTOTYPE

In the previous chapters the features of PDLC topology have been explained, focusing the attention on the interaction between the power stages that are used to realize this architecture. Based on this key feature, the PDLC was analysed from the topological point of view to provide general design guidelines as well as to show the essential role of the Active Clamp circuit, in many aspects of this converter. Then the modulation techniques have been analysed, starting from the effects of Pulsating DC link on the VSI stage operation and providing a complete overview of the techniques proposed in literature. In this chapter the experimental results of complete characterization of PDLC prototype, designed on specifications for auxiliary power supply for light railway vehicles, will be presented to verify the operation and features of the proposed architecture. Before presenting the results of the characterizations, the prototype of PDLC and its implementation will be described, providing details about the components used in every section of the power converter.

5.1 Description of the prototype

As said before, the proposed PDLC architecture was designed on the typical technical specifications used for an Auxiliary power supply for light railway vehicles, application that requires galvanic isolation between the DC source and the AC outputs as well as natural convention of air cooling system. In the Table 6 the used specifications are reported. The 1.7kV IGBT power modules were used in the first prototype to implement all the controlled power stages (PSB, VSI and Active Clamp), while 1.7kV SiC Schottky power diodes were used for the output rectifier. In the last years this first realization of the proposed PDLC architecture has been improved and optimised, thanks to the use of SiC power modules for the first stage, which has become an all-SiC converter, and the replacement of the magnetics components. With

the upgrade of the PSB stage with the SiC devices, it was necessary to redesign the layout of the power board since the previous one was optimised for Silicon devices and all the consequent constraints for the operation frequency. In particular the new power board has been designed using the busbar technique and the distribution of the dumping input capacitor, across the surface of the board, with the aim to minimize the leakage inductance. Instead, the implementations of the VSI stage and Active Clamp circuit were not modified since the aim of this work is to reduce the switching losses of these stages with a clever use of the ZPs of the Pulsating voltage. Consequently, the Si devices of the VSI stage were not replaced with more performing SiC devices, continuing to use low cost and reliable IGBT modules.

Table 6 Specific of Auxiliary power supply for railway vehicles application

Nominal Input voltage	**750 V**
Full Input voltage range	**(600-900) V**
Output voltage (RMS)	**400V ± 5%**
Nominal output power	**30kW**
Nominal apparent power	**37,5kVAr**
THD output voltage	**≤ 8%**
Cooling system	**Air natural convection**

Therefore two versions of the PDLC prototype were developed. Their main features can be synthetised in the following way:

- Quasi all-Si version: Except for the SiC Schottky barrier rectifier of the first stage, the other powers stage are implemented with the IGBT Power modules. The power boards and magnetic components are designed and realised to operate with switching frequency up to 20kHz.
- All-SiC PSB stage version: this second version of the prototype presents an all-SiC PSB stage as first stage while the VSI stage and Active Clamp are common with the first prototype.

To conclude the two versions of the PDLC prototype will be presented below, highlighting the semiconductor devices used and providing details about the realization.

5.1.1 Quasi all-Si version

As said before, this first version of the prototype makes use of 1.7kV Semikron IGBT half-bridge power modules in PSB stage [61], VSI stage and Active Clamp [62],

except the output diode rectifier of the PSB stage. This rectifiers are 1.7kV Wolfspeed SiC Schottky diode [63] which are connected in parallel (four diodes) to achieve the current rating requested by the application. Table 7 summarizes the semiconductor devices used for the implementation of the first prototype:

Table 7 Semiconductor devices of the Quasi all-Si version of the PDLC prototype

Power stage	Name of component
Full bridge PSB stage	**SKM 200GB176D**
Diode rectifier	**C3D25170H**
VSI stage and Active Clamp	**SKM 75GB17E4**

Figure 81 reports the picture of the full bridge of the first section, where the different components of the PCB are highlighted.

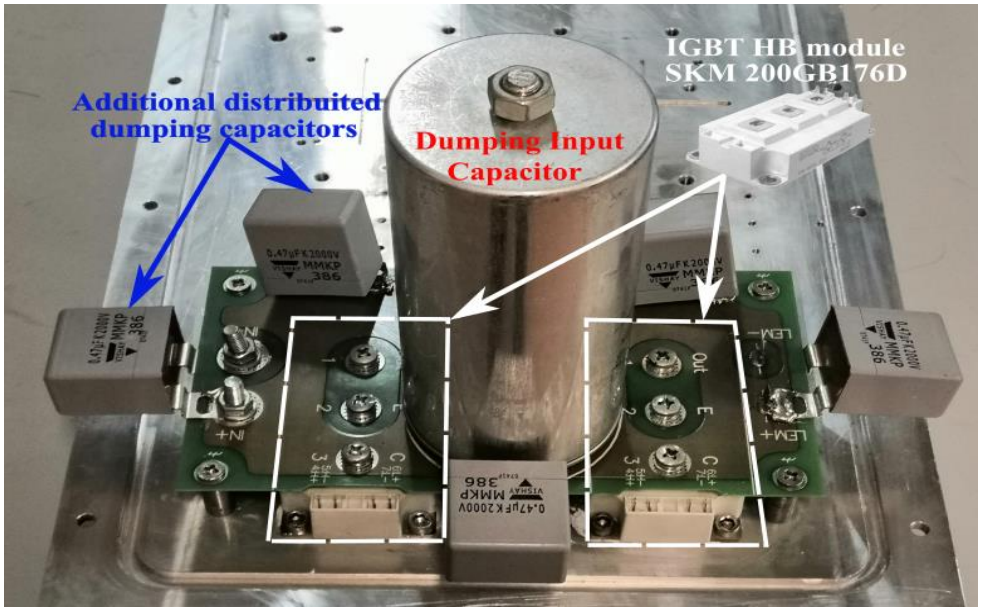

Figure 81 – Picture of the first version of full bridge of the PSB stage

From the figure, it can be noted that the power board presents two different types of dumping capacitors, one concentrated and the others distribute along the section of the board. These latter have been placed to minimize the leakage inductance of the circuit and, consequently, reduce the ringing during the commutations. Instead Figure 82 reports the picture of the power section that implements the VSI stage, the Active Clamp circuit and the output rectifier of the PSB stage on the same heatsink.

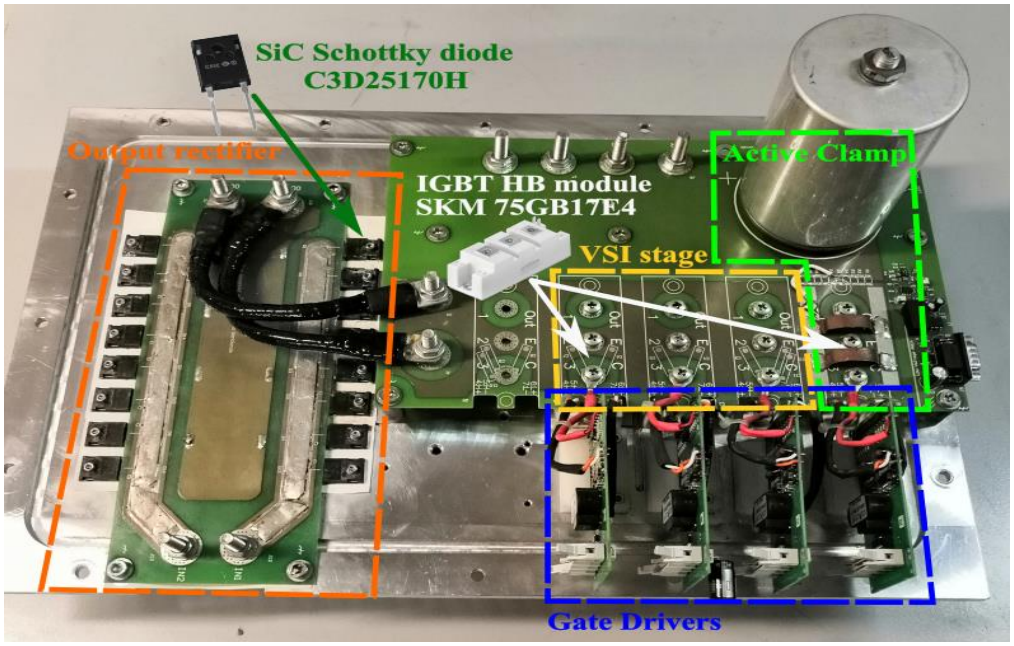

Figure 82 – Picture of the section that implements the VSI stage, the active Clamp circuit and the output rectifier of the PSB stage

The connection between the output rectifier of the first stage and the power board that implements the VSI stage and Active Clamp circuit was realised with power cables. In this way the problem of different heights of the sections, due to the packaging of the semiconductor devices is simply solved.

5.1.2 All-SiC PSB stage version

This second version of the prototype presents the same semiconductor devices and power boards for the VSI stage, active Clamp circuit and diodes rectifier. Instead the devices of the full bridge of the PSB stage are replaced with 1.7kV Wolfspeed SiC MOSFET half bridge power modules [64], to improve the performance at higher switching frequencies. Moreover the power board of the full bridge has been rebuild, to improve the quality of the layout in such a way to take advantage of the better performances of the new SiC devices. The semiconductor devices of the prototype upgrade are summarised In Table 8:

Table 8 Semiconductor devices of the Quasi all-SiC PSB stage version of the PDLC prototype

Power stage	Name of component
Full bridge PSB stage	**CAS300MA7BM2**
Diode rectifier	**C3D25170H**
VSI stage and Active Clamp	**SKM 200GB176D**

A picture of the new version of the full bridge of the PSB stage is reported in Figure 83, where the components used in this new version are evidenced.

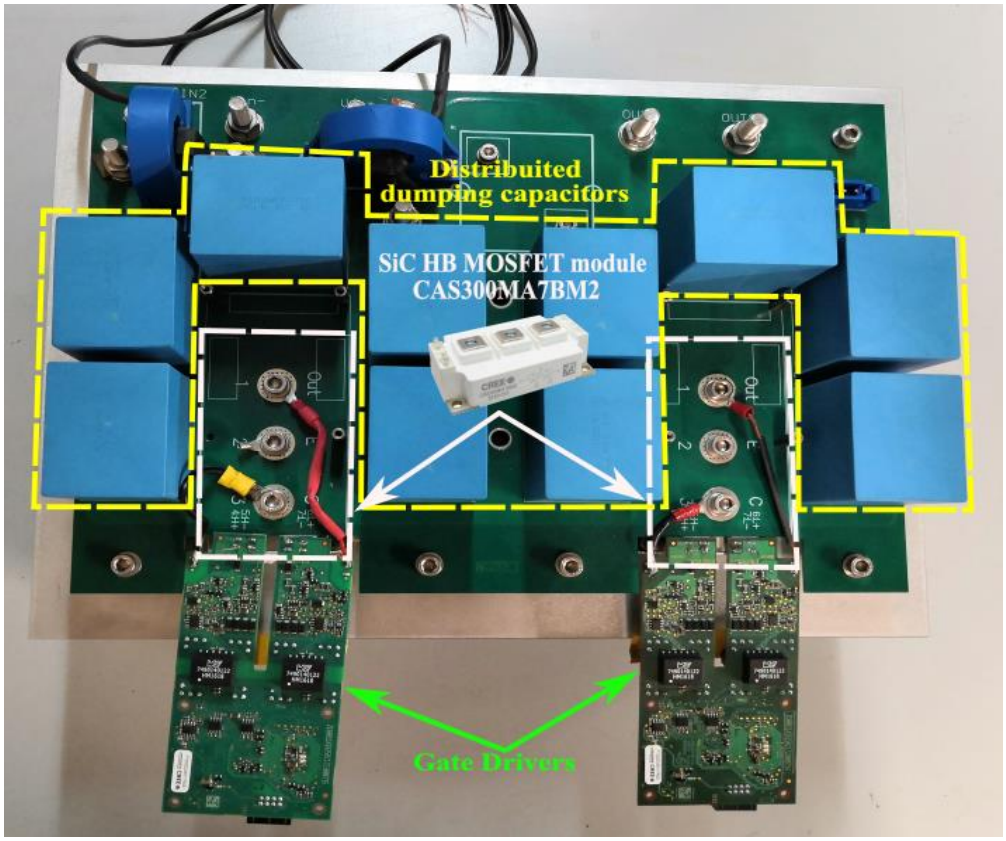

Figure 83 – Picture of the second version of the full bridge of the PSB stage, implemented with SiC MOSFET modules

The picture shows that ten dumping capacitors distributed on the board have been used to minimize the stray inductance of the board. In particular they are placed as close as possible to the SiC power modules, leaving just one side free for the connection of the Gate driver to the respective power module.

5.2 Characterization of the first prototype based on Si of PDLC topology

The first version of the PDLC prototype has been fully tested under different load and input conditions, to verify the main characteristics and performances of the analysed topology. In particular the characterization of the converter was completely executed on resistive load, to simplify the analysis. Figure 84 reports two pictures of

the first version of the prototype, where the main components and power stages are highlighted. Regarding the implementation of the modulation technique a FPGA Altera DE2 evaluation board has been used.

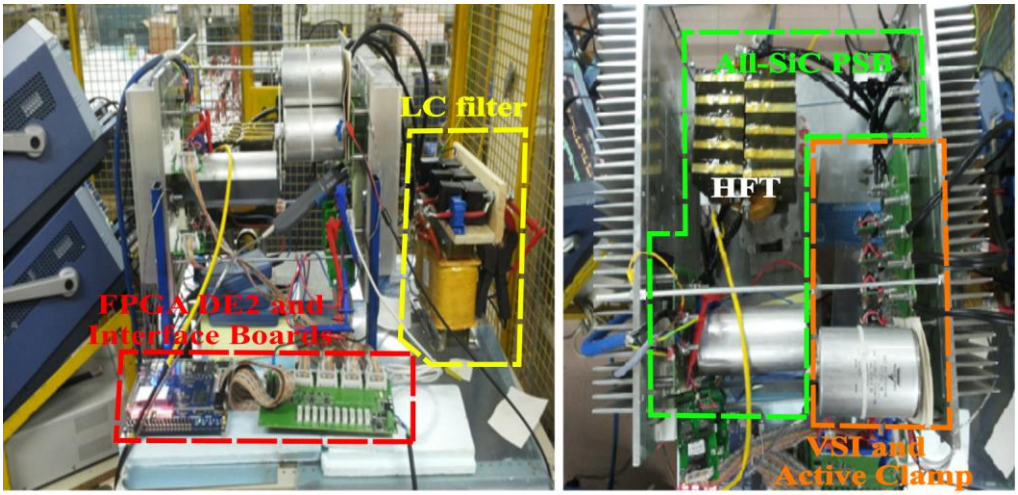

Figure 84 – Experimental setup for the characterization of the first version of PDLC prototype

Together with an interface board, the FPGA board controls and supervises the operation of the converter. In particular the interface board provides the driving signals to the Gate drivers of each power stage and manages the short-circuit protection of the drivers. For the driving of the half-bridge power modules, the gate drivers advised by the manufacture have been used. The modulation technique used for this characterization was the technique presented in [43] which is conceived to use the ZPs of the pulsating DC link for the commutations of the VSI stage. The experimental results reported in this section were achieved with a switching frequency of the first stage of 20 kHz, which thanks to the operating principle of the modulation technique set the frequency of the Inverter stage equals to 10 kHz. A conventional HF transformer realized with ferrite nucleuses was used in this first version of the prototype with a turn ratio of 7/6, a magnetising inductance of 20 mH and a leakage inductance of 20 uH. The output filter was realised with a three-phase 1 mH inductor for phase and a parallel of three capacitors with an equivalent 120 μF phase capacitance, connected in star connection. The experimental characterization of the PDLC was performed on several resistive loads, connected in star connection. The characterization was started with the measure and the analysis of the time evolution of transformer and Pulsating DC link characteristics. Since the characterization is the same for both the prototypes, the results are presented only for one case for brevity. In

particular the results reported in the following pages have been achieved with the second prototype, featured by transformer with a turn ratio of 1.3.

Figure 85 reports the measured waveforms of the Pulsating DC link voltage and the primary current of the transformer for V_{in}= 750 V and P_{out}= 5 kW.

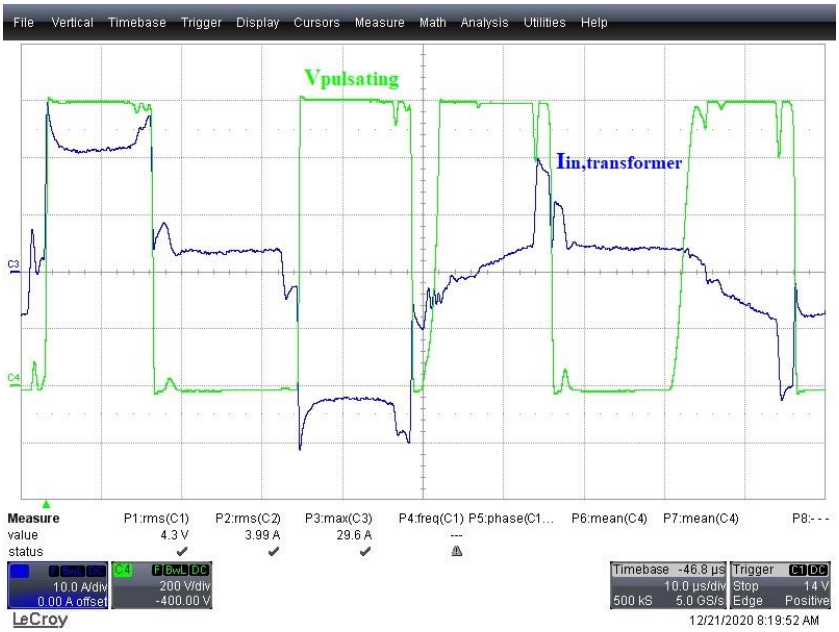

Figure 85 – Evolution of the Pulsating DC link voltage (green) and the primary current of the transformer (blue) for V_{in}= 750 V and P_{out}= 5 kW

We can note the expected pulsating evolution of the DC link with the fundamental ZPs distributed along the period as well as the evolution of the primary current that is quite symmetrical. Instead, Figure 86 shows the measured voltage and current waveforms on the HF transformer for the same input voltage V_{IN}= 700 V and P_{out}= 4.1 kW.

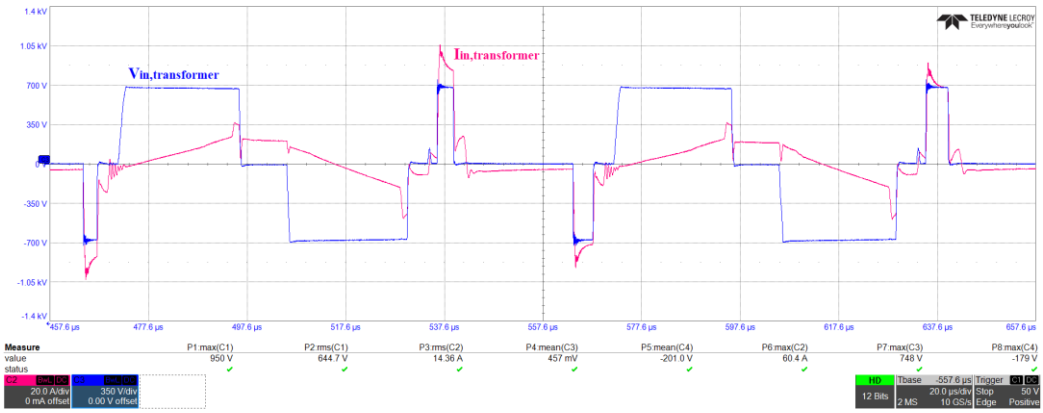

Figure 86 – Evolution of the input voltage (blue) and the primary current (magenta) of the transformer for V_{in}= 700 V and P_{out}= 4.1kW

We can recognise the typical voltage (blue curve) resulting from the H bridge phase shift operation and the corresponding current (magenta curve) flowing through the primary side of the transformer. Moreover, it can be observed how the width of the free-wheeling phases is not fixed but assumes different values. In particular the wide ZPs are used for the consecutive commutations of VSI stage leg, which are followed by narrow pulse due to limit values of duty cycle (minimum or maximum value). Instead the short ZPs are placed in correspondence of the single commutations of the VSI stage, which happen for average width of pulse. Consequently the voltage waveform of the transformer and the variable width of the ZPs demonstrates how the modulation technique controls the operation of the PSB stage to achieve the ZVT of the VSI stage.

Before focalizing the attention on the output voltages of the PDLC, the commutations of the first stage were investigated to see the differences between the behaviour of the two legs. Figure 87 reports the evolution of the voltages across the switches of the leading leg, the driving signal and the switched current of the lower switch in the case of V_{IN}= 700V and P_{OUT}= 4 kW.

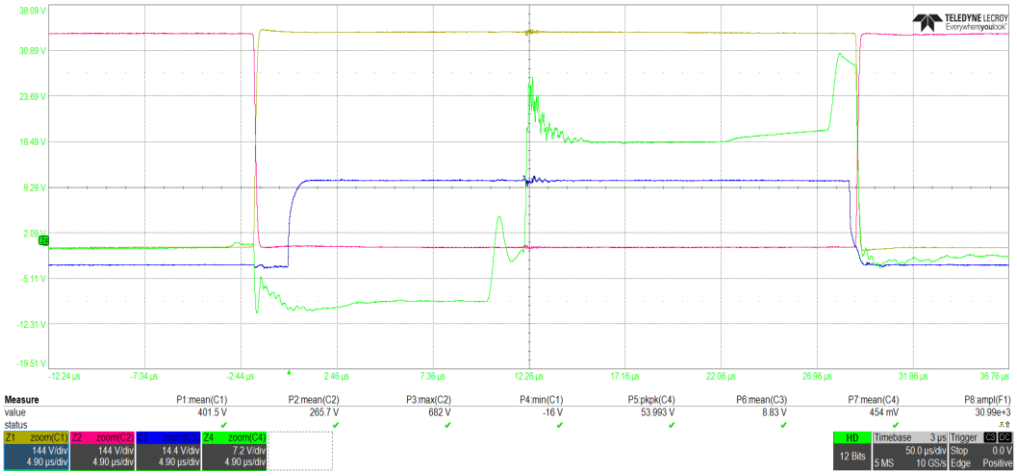

Figure 87 – Detail of commutations of Leading leg for V_{IN}= 700 V and P_{OUT}= 4kW (in yellow the V_{DS} of high switch, in red the V_{DS} of lower switch, in blue the V_{GS} of lower switch and in green the current of lower switch)

We can note that the turn-on of the low side switch is in ZVZCS condition since the voltage across it is zeroed and the current flows through the antiparallel diode, before the driving signal changes the state of the switch. Instead, Figure 88 reports the evolution of the voltages across the switches of the legging leg, the driving signal and the switched current of the low side switch in the case with V_{IN}= 700V and

P_{OUT} = 4 kW. In this case more commutations of the leading leg are reported, Only some of them are ZVS but some of them are hard switching. Indeed, the converter feeds a Inverter stage whose current significantly changes in time, then for some commutations the energy stored in the stray inductance is not enough to discharge the circuit capacitance to achieve ZVS conditions as shown in the following figure.

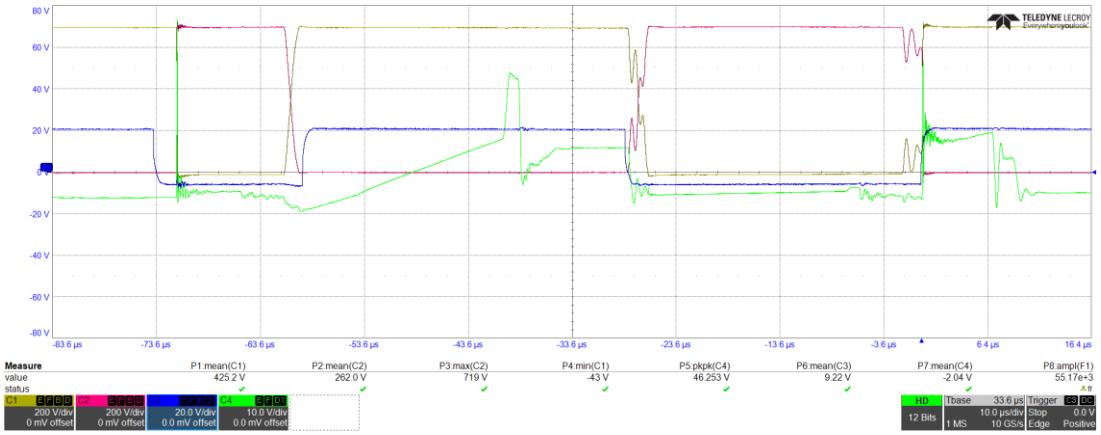

Figure 88 - Detail of commutations of Legging leg for V_{IN}= 700 V and P_{OUT}= 4kW (in yellow the V_{DS} of high side switch, in red the V_{DS} of low side switch, in blue the V_{GS} of low side switch and in green the current of low side switch)

Observing the above figure we can note two different turn-on of the low side switch, due essentially to the load. The first turn-on, on the left, happens in ZVZCS condition as the leading leg while the second turn-on is hard-switching since the stored energy in the stray inductance is not enough to satisfy the ZVS condition. To conclude from the point of view of the commutations, the first stage of the PDLC acts as common PSB stage with an output inductor due to the AC output filter of the VSI stage.

Figure 89 reports the evolution of the pulsating DC link voltage with a detailed zoom and the output three phase voltages for V_{in}=720V and P_{out}=4.1kW.

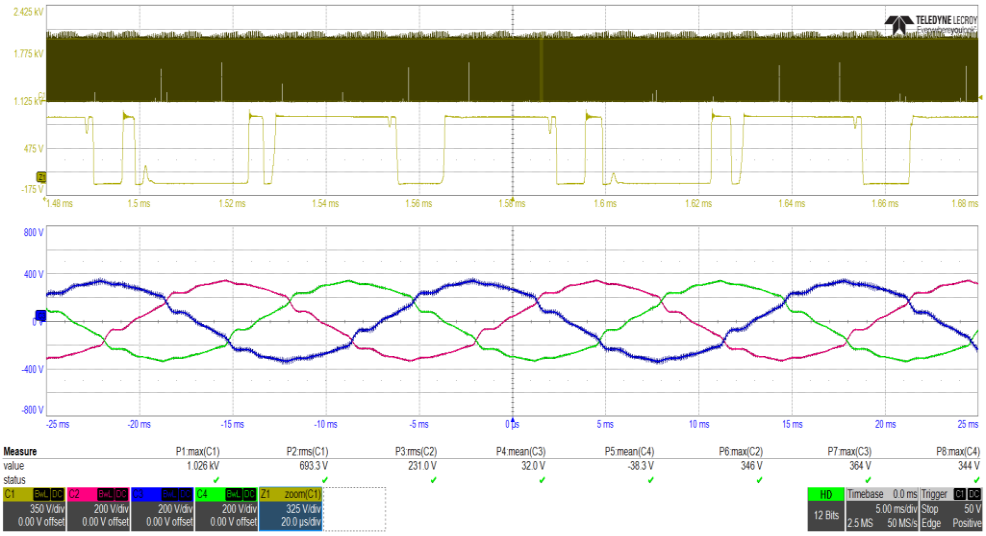

Figure 89 – Evolution of the Pulsating DC link voltage and detailed zoom (top plot) and the three output phase voltages (bottom plot) for P_{out}=4.1kW and V_{in}= 720 V

From the above figure confirms the feasibility of generating a three-phase voltage using a Pulsating DC link as DC bus, without negative effects of the ZPs of the pulsating voltage on the quality of the output voltages. This test was performed at low value of output power which is the worst case for this topology, since the dumping effect of the load is minimized. This influence of the output power on the quality output the voltage of the PDLC topology has been investigated for different values of the load and the results are reported below. Figure 90 reports the measured waveforms of the output phase voltage and current for V_{in}=750V and P_{out}=4.1kW.

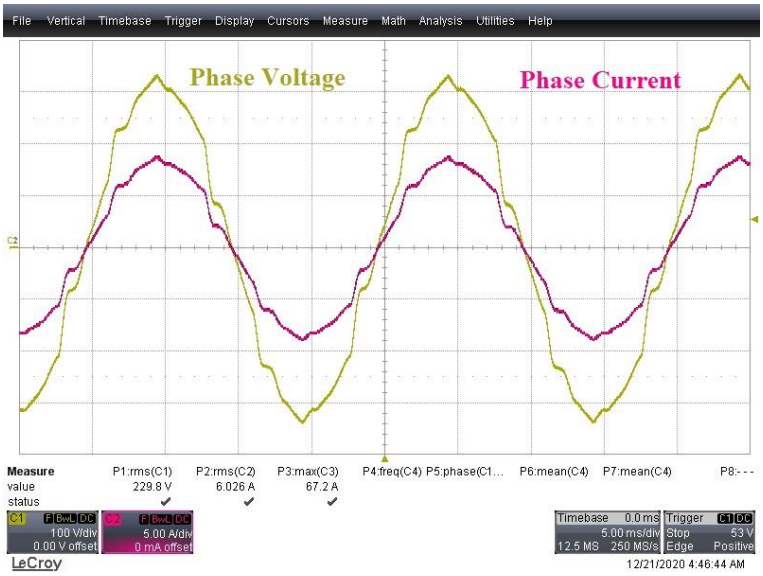

Figure 90 – Output phase voltage (yellow) and phase current (magenta) for input voltage of 750V and output power of 4.1 kW

The measure of the output waveforms was performed for different values of the output power, as shown in Figure 91 and Figure 92 which reports the measured waveforms for the same input voltage of 750 V and for P_{out}=11.9 kW and P_{out}=15.9 kW, respectively.

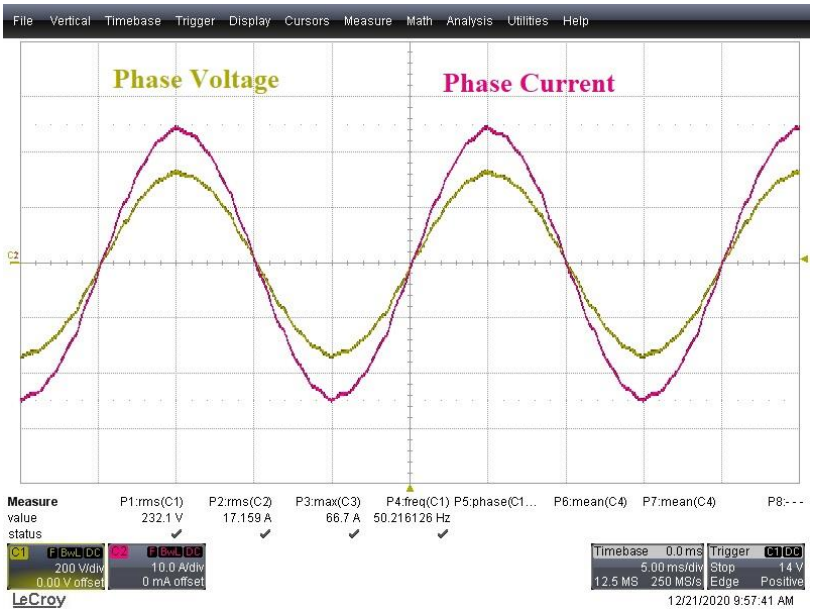

Figure 91 – Output phase voltage (yellow) and phase current (magenta) for input voltage of 750V and output power of 11.9 kW

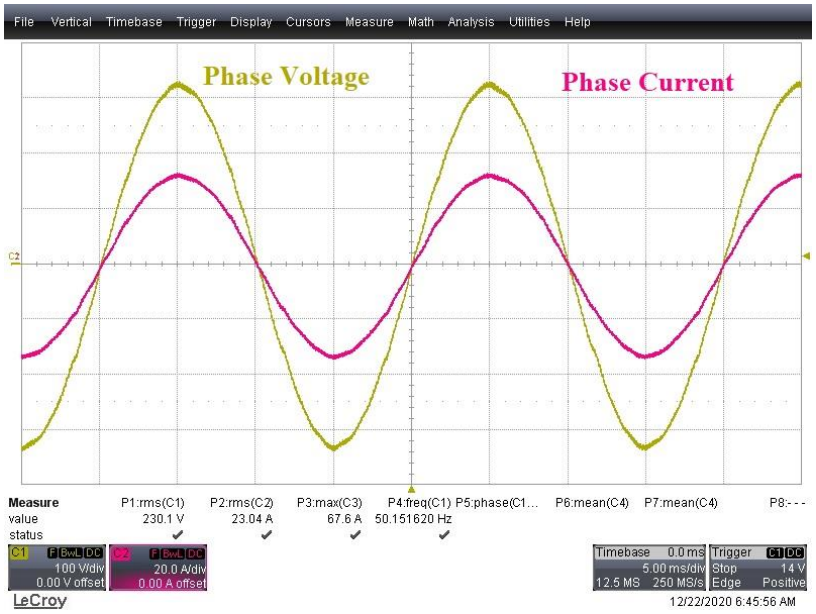

Figure 92 – Output phase voltage (yellow) and phase current (magenta) for input voltage of 750V and output power of 15.9kW

Comparing the evolution of the phase voltages, we can note that in all cases the power converter generates voltage with quite good shape and symmetry. Only in the case with reduced output power the quality of the phase voltage is quite poor, as visible in Figure 90. Fortunately the THD values of the voltage comply with the limits provided by the specifications and the European standard.

The efficiency and the THD value of the output voltage were then evaluated for different load conditions. The HIOKI 3193 power analyser/meter with 6 independent channels was used for the measures. One channel of this instrument was used to measure the input DC power. Instead other three channels of the instrument were used to measure the output power, using the same connection of the resistive three-phase load. To improve the quality of the measure, particular attention was paid to the connections to avoid that the voltage drops across the cables could affect the power measurement.

Figure 93 shows the converter efficiency as a function of the output power for different values of the resistive load and for the nominal input voltage. The maximum efficiency is about 92% and it is reached at high output power and in particular at about 20kW. At low output power (Pout<10kW) we observe a reduction of converter efficiency to a minimum value of 82% at Pout=3kW. This degradation of the efficiency can be explained considering that the control strategy has been optimized only for high

values of output power. Moreover the power devices energy losses have a larger impact at lower loads.

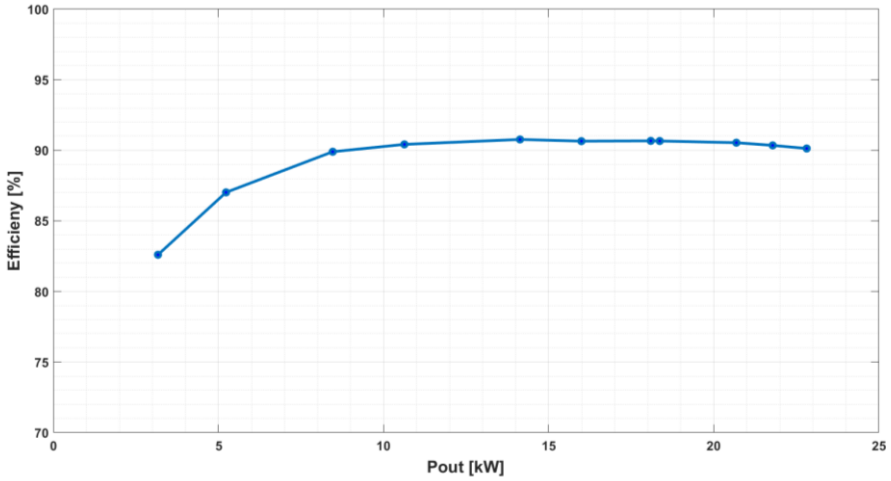

Figure 93 – Efficiency plot versus the output power

Figure 94 reports the trend of the harmonic distortion of the output voltage as a function of output power in the same test conditions of Figure 93. We can recognize that the THD is lower than 1.5% for output power higher than 15kW.

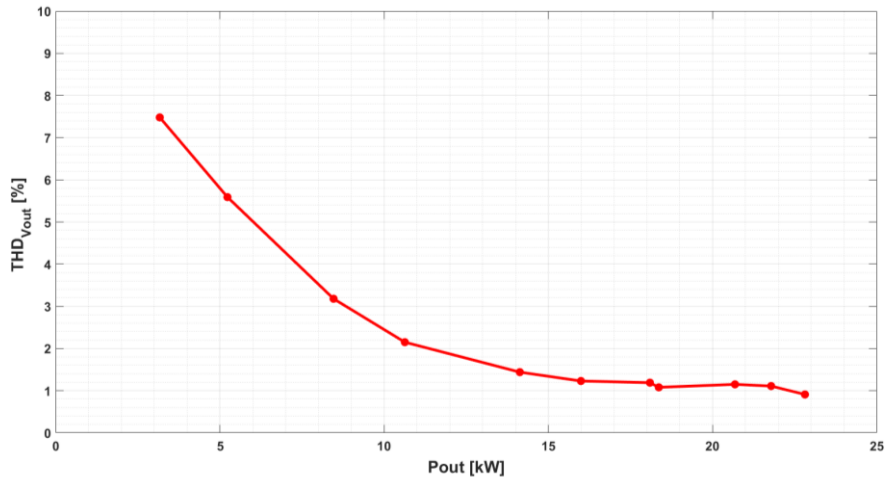

Figure 94 – Evolution of the THD value of output phase voltage for different values of the output power.

As observed for the efficiency, the distortion very rapidly worsens at low loads for reasons similar to those used to explain the efficiency reduction. Moreover, the decrease of the output power provides a reduction of the dumping effect of the resistive load on the output filter, causing an increase of the harmonic voltage amplitudes and consequently the increase of the THD value. However, considering that the industrial

standards require a THD value of the voltage lower than the 8%, we can note that the trend of the distortion is below this limit. To validate the efficiency results and to measure the distribution of the losses in every power stage, several thermal and electrical measures were executed. These latter were executed after several hours of continuous operation required by the converter to reach its thermal steady state conditions. As an example Figure 95 shows the power losses in the various sections of the system for the output power of 10.5kW, for which the converter exhibits an efficiency of 89.4%, corresponding to a total energy loses of 1240W. We can see that the main losses are located on primary H bridge and in the transformer while the secondary section that operates in total soft switching has only 16% of the total losses.

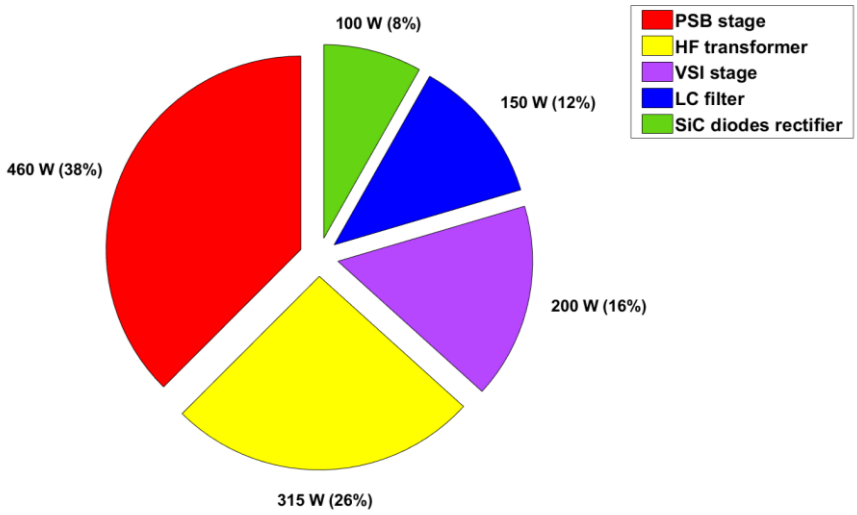

Figure 95 – Pie representation of the measured power losses for output power of 10.5kW

From the above pie plot, we can note that the 72% of the overall losses are due to the PSB stage and in particular to the IGBT based full bridge and the high frequency transformer. So we can conclude that the main causes of the excessive losses of the PSB stage are due to:

- The switching and conduction losses of the IGBT modules used for the full bridge which are not so performing at the switching frequency of 20 kHz, making the PSB stage the worst stage in terms of efficiency.
- The HF transformer which is not optimised for the particular features of the PDLC topology, causing extra power losses.

Starting from these considerations the new version of the PDLC prototype was developed. Its performances are described in the next section.

5.3 Characterization of the second version of the prototype based an all-SiC PSB stage

The second version of the PDLC prototype has been characterised in the same test conditions of the previous version, focusing the attention on the operation of the Active Clamp circuit. The role and the features of this power stage are fundamental for the PDLC topology, as showed in the previous chapters where the interaction with the other stage are analysed. Moreover, the evolutions of the primary current of the transformer and the Pulsating DC link voltage have been evaluated for different test conditions and different values of Clamp capacitor, to analyse the interaction and relationship between them. The aim of the characterization, whose results are reported below is to verify and validate the design guidelines provided in the third chapter. In Figure 96 the picture of the experimental setup is reported. It was realised for the full characterization of the second version of the PDLC topology prototype.

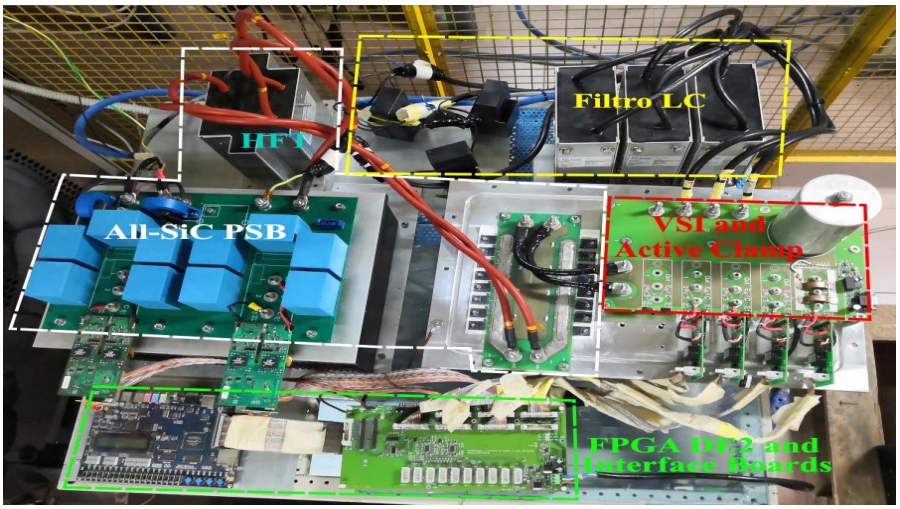

Figure 96 – Experimental setup for the test of all-SiC PSB stage version of the prototype

Observing the above figure and comparing it with the setup of Figure 84, we can note that a new transformer and a new low-pass LC output filter has been used in the new setup to improve the overall performances of the converter. In particular, a turn ratio of 1.3 was set for the new transformer for which a magnetising inductance of 0.8 mH and leakage inductance of 6 uH where assigned. The same capacitors of the previous version and a new filter inductor with 280 uH for phase were used in the output filter.

A first characterization was executed on the prototype where the first modulation technique with soft switching of the VSI stage, described in paragraph 4.1.5, was used.

To illustrate the operation of the clamp circuit, the top plot of Figure 97 shows the waveforms of Collector-Emitter voltage (magenta), Collector current (yellow) and Base-Emitter voltage (blue) of clamp S_{ac} in the case with $C_{ac} = 220\mu F$, and in the test conditions: $V_{in} = 650$ V and $P_{out} = 5$ kW. The bottom plot of the figure shows the zoom in the region of the top plot marked with the red dashed rectangle.

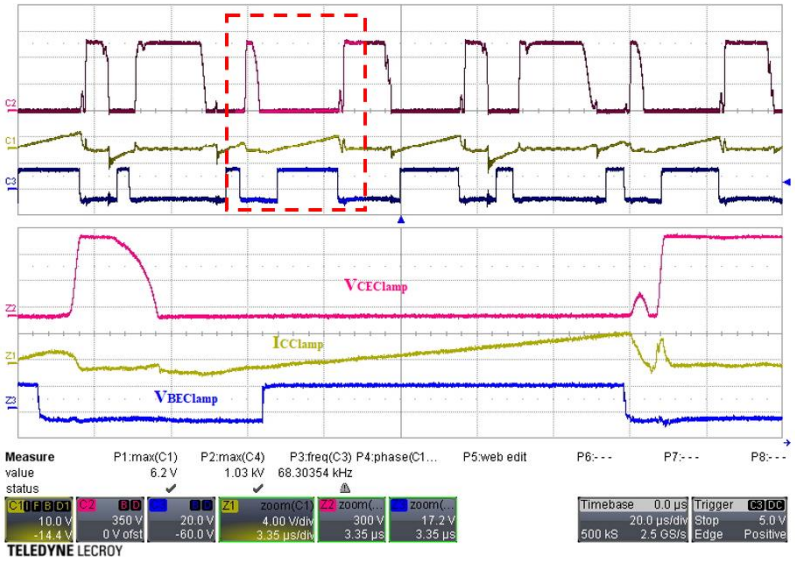

Figure 97 – Top plot: Collector-Emitter voltage (magenta), collector current (yellow) and Base-Emitter voltage (blue) of clamp Sac for Cac=220μF, Vin =650V and Pout =5kW. Bottom plot: zoom in the region of the top plot marked with the dashed red rectangle.

The gate voltage of the IGBT used as S_{ac} indicates that the clamp is turned on and off twice in the period of the PSB switch (50 μs) where two energizing phases took place. For completeness, we have to say that the IGBTs of the VSI stage are commutated with a period of 100 μs during the freewheeling phase of the PSB stage. The clamp current waveform of the bottom plot indicates that the current initially is negative and flows in the diode in antiparallel to S_{ac}. Then the clamp is turned on in ZVZCT conditions and the current becomes positive flowing through the switch. The associated energy to the clamping phase of the circuit is used to feed the VSI during the energizing phase. The turn off of S_{ac} is at low dissipated energy due to the low value of the involved circuit stray inductor which limits the voltage across the switch. In order to evaluate the effects of the Active Clamp capacitor C_{ac} on the transformer peak current and overvoltage on the DC link, some different tests have been performed on the prototype. Figure 98 reports the waveform of Pulsating DC link voltage ($V_{Pulsating}$), primary side transformer current (I_{Lstray}) and Base-Emitter voltage

($V_{BEClamp}$) of S_{ac} with the Active Clamp capacitor $C_{ac} = 220\ \mu F$ and in the test conditions: $V_{in} = 650$ V and $P_{out} = 5$ kW. During the on state of S_{ac}, the DC link peak voltage approximately reaches the value of 1100 V and then it is kept constant to 845 V, thanks to the large value of C_{ac}. Moreover, the primary side transformer peak current reaches the value of 25.7 A.

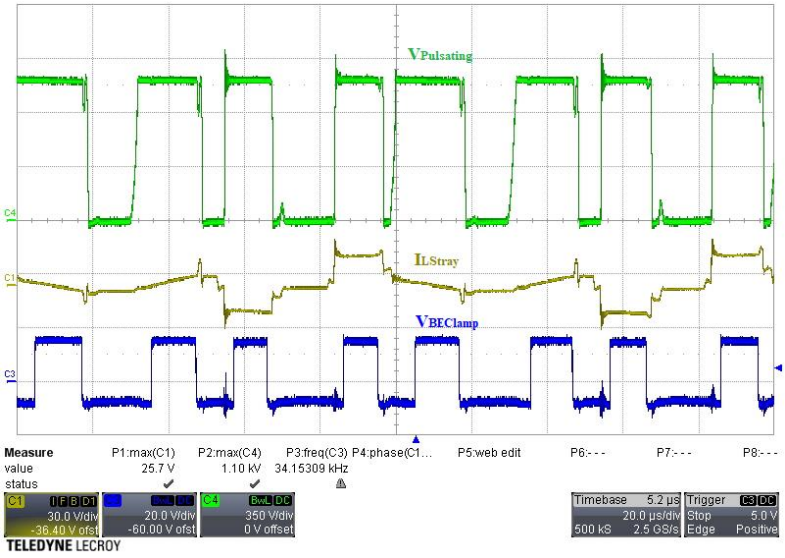

Figure 98 – Pulsating voltage (green), transformer primary current (yellow) and Base-Emitter voltage (blue) of Sac for Cac=220µF, Vin=650V and Pout=5kW.

To show the effects of C_{ac} reduction, the experiment of Figure 98 was repeated with C_{ac}= 470 nF obtaining the results of Figure 99.

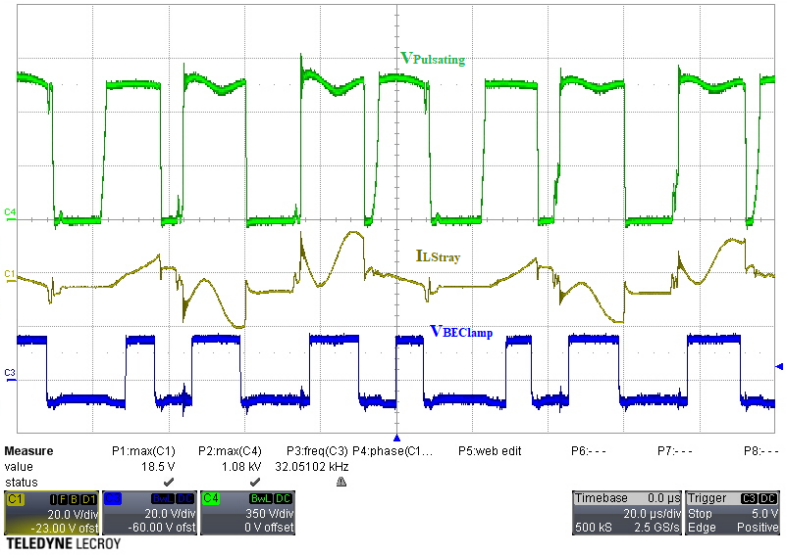

Figure 99 – Pulsating voltage (green), transformer primary current (yellow) and Base-Emitter voltage (blue) of Sac for Cac=470nF, Vin=650V and Pout=5kW.

It is worth to note that in the second case the DC link peak voltage reaches a slightly higher value ≈1130 V, measured in a time interval different from the one shown in the figure, but the peak of the current flowing through the transformer is significantly reduced to 18.5A. Figure 99 shows that the capacitance C_{ac} causes a second resonance on $V_{Pulsating}$ and I_{LStray} at a frequency lower than the frequency associated with the resonance involving parasitic capacitances and inductance which is responsible for the overvoltage we discussed in paragraph 3.1. This second resonance involves L_{Stray} and C_{ac} and manifests itself on the high values of $V_{Pulsating}$ in the case with $C_{ac} = 470\ nF$ because in this case its period is comparable with the switching period of S_{ac}. Instead, for $C_{ac} = 220\ \mu F$, the oscillation period of the second resonance is much greater and its characteristic impedance is much lower so $V_{Pulsating}$ is flat after the initial high frequency oscillations (see Figure 98).

As a further example, Figure 100 reports the waveforms of Pulsating DC link voltage, primary side transformer current and Base-Emitter voltage of clamp switch for $C_{ac} = 470$ nF, in the test conditions: $V_{in} = 650$ V and $P_{out} = 2.3$ kW.

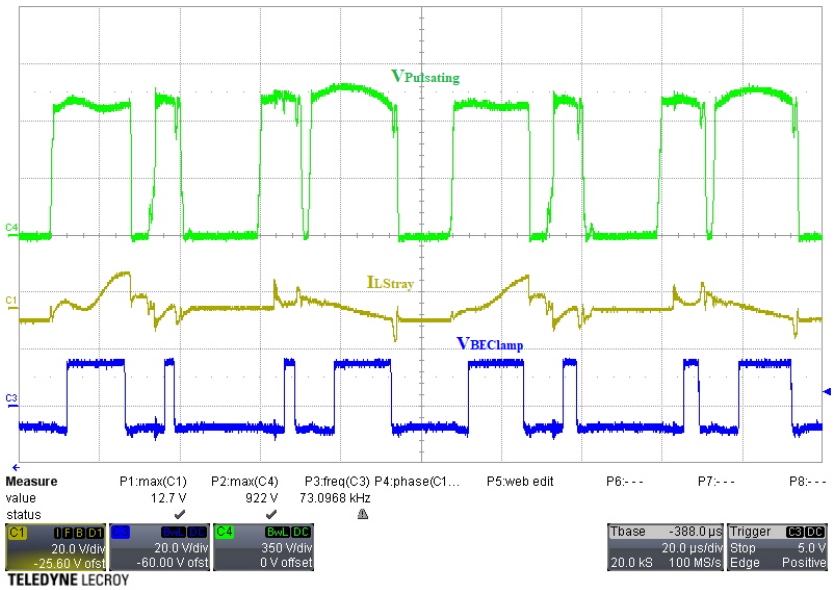

Figure 100 – Pulsating voltage (green), transformer primary current (yellow) and Base-Emitter voltage (blue) of Sac for Cac=470nF, Vin=650V and Pout=2.3kW.

The comparison between Figure 99 and Figure 100 shows that there is no significant difference in the aspect of the two waveforms, except that the load reduction causes the reduction of the current flowing through the converter, resulting in the reduction of rms and peak values of the transformer current.

To complete the analysis, a characterization of the impact of the Active Clamp capacitor C_{ac} on the converter behavior in different operating conditions has been performed. In particular, Figure 101 shows the trend of current peak, I_{Lpk}, in the primary side of the transformer (left plot) and overvoltage, OV_{DCLink}, on the DC link (right plot) as a function of C_{ac}, for two values of the load power, namely 2.3 kW and 4.1 kW. OV_{DCLink} is calculated as the difference between the peak and the flat values of the DC Link voltage.

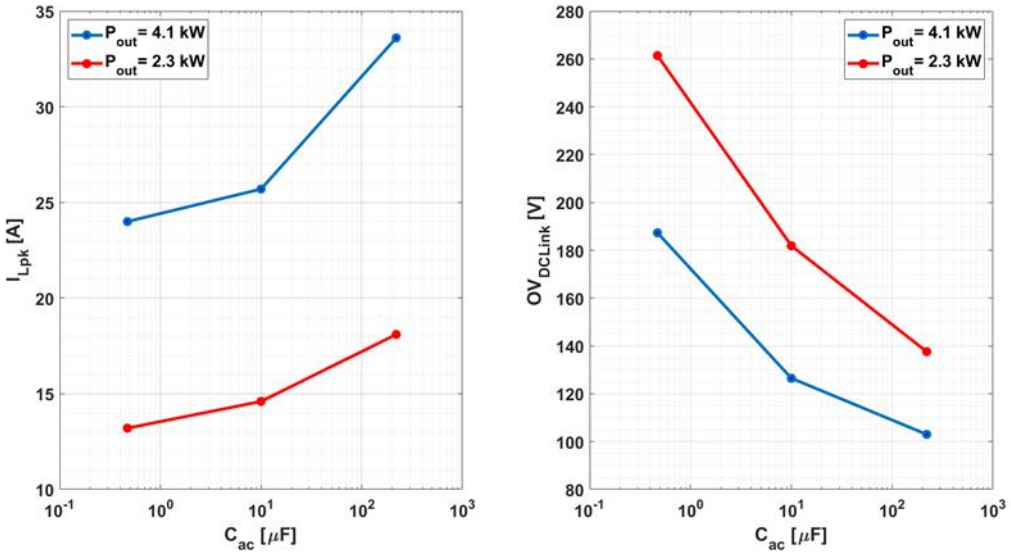

Figure 101 – Peak current in the transformer (left plot) and DC link overvoltage (right plot) vs Cac for two values of the load power P_{out}, namely 2.3 kW and 4.1 kW

The experimental results confirm the trend observed in the simulation analysis, since the current peak in the transformer rises with the increase of capacitor value and load power. On the contrary, the overvoltage on the pulsating DC link decreases with the increase of the Clamp capacitor and the load power.

To conclude the characterization of the new prototype, its efficiency has been measured with the power meter up to the output power of 16 kW, in the test conditions already used for the previous characterization. The trend of the measured efficiency is reported in Figure 102 as a function of the output power, together with the efficiency measured on the first prototype already reported in Figure 93. The figure quantifies the improvement in efficiency due to the use of new magnetic components and the replacement of the IGBT modules of the PSB stage with more performing SiC MOSFET modules. The efficiency of the new version of the prototype is at least 3% higher than the first one in all range of the output power. At the maximum load of

16 kW, a reduction of more than 600 W in the dissipated power has been achieved corresponding an efficiency increase of about 4%.

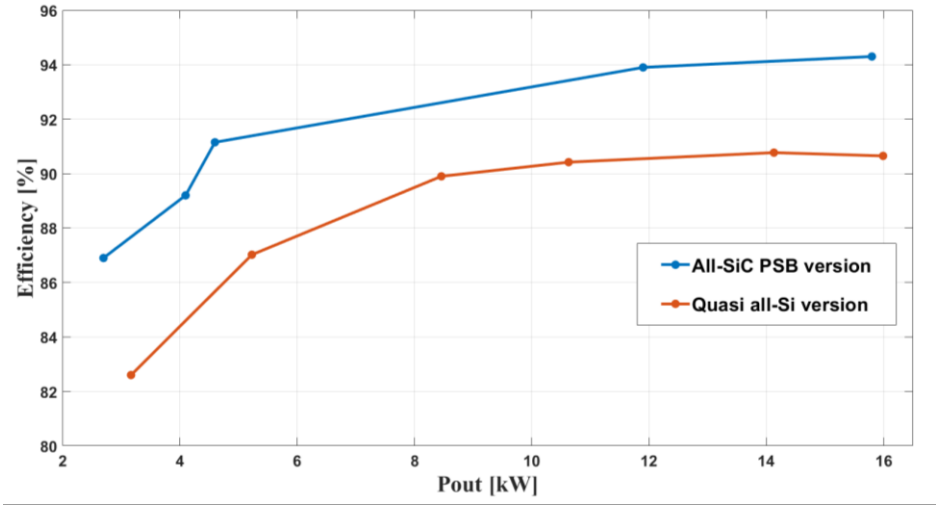

Figure 102 – Efficiency plots of the All-SiC PSB stage version(blue plot) and Quasi all-Si version (orange plot) of the PDLC prototype

5.4 Experimental characterization of the PDLC with modulation technique based on unrelated frequencies

The aim of this paragraph is to present and discuss the experimental results achieved on the second version of the prototype with the new modulation technique, based on unrelated and independent switching frequencies. The benefit of this technique is the absence of a strict constraint on the ratio of the switching frequencies, which allows the choice of each switching frequency to optimise the features of each single stage. The characterization of this technique has been only performed on the new version of the prototype, since the power board and the semiconductor devices of old version are designed for low switching frequency (maximum 20kHz). Consequently this latter is unsuitable for the test of the main features of the new modulation technique for PDLC topology. For the hardware implementation of the modulation technique and the control of the prototype, the same FPGA evaluation and interface boards of the old version of the prototype were used. However due to the complexity of the new modulation technique, it was not implemented directly on the FPGA board but a

procedure based on the use of the same driving signals of the simulation has been conceived and realised. In particular, the driving signals, used for the simulation analysis of the topology are computed with a MATLAB routine and saved and formatted in such a way to be allocated in the memories of the FPGA board. A routine is implemented on the FPGA board, starting from the data saved offline in the FPGA memory. The firmware is able to rebuild the driving signals of the converter without loss of information as dead times and synchronization between the operation of the PSB stage and Active Clamp circuit. Moreover, the custom program handles the short circuit protection signals of the Gate driver to implement the software protection of the converter against the short-circuit of the power modules. The described procedure is the easiest way to implement the new modulation technique, avoiding the direct implementation on the FPGA board in VHDL which could get quite complicated.

The analysis of the converter was started with the study of the pulsating DC link voltage and current in the primary side of the transformer for different values of switching frequency of the PSB stage. Figure 103 reports the measured waveforms of the Pulsating DC link voltage and transformer current with V_{in}=600V and P_{out}=2.6kW for the switching frequency of PSB stage of 60kHz and 80kHz, respectively.

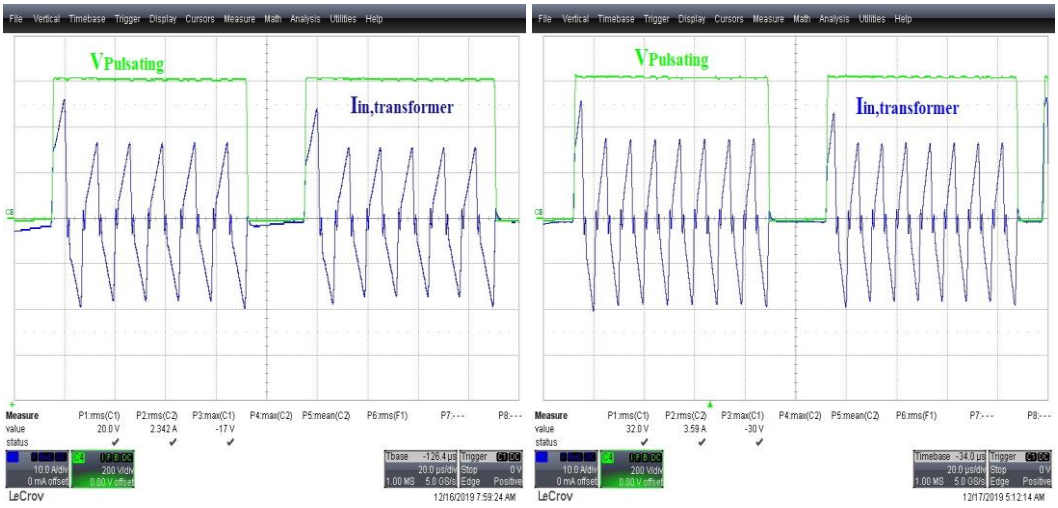

Figure 103 – Pulsating voltage (green) and primary transformer current (blue) in the case Vin=600V, POUT=2.6kW for a switching frequency of the PSB stage equal to 60kHz (left) and to 80kHz (right).

The above figure clarifies the operating principle of the modulation technique and highlights the different switching frequencies of the converter. In particular the number of complete energising phases of transformers corresponds to the average value of the switching frequency of the PSB stage while the period between two consecutive ZPs

defines the switching frequency of VSI stage whose switches are commutated during these ZPs. A complete energising phase of the transformer is achieved performing two energising phases of the PSB stage, which allow a symmetrical current on the transformer without DC components. The first and last energising phases are featured by a width greater than the others to allow the turn-on and turn-off of the switch of the Active Clamp circuit.

To show the ZVT conditions of the VSI switches, achieved thanks to the modulation technique, the commutation of inverter leg R is analysed in detail. Figure 104 reports the waveforms of the low side IGBT of the phase R, when the phase R is requested to supply the intermediate voltage and the corresponding leg is switched. Specifically the figure reports: Collector-Emitter voltage V_{CE}, Gate voltage V_{GE} , the Collector current I_C and the Pulsating DC Link voltage $V_{Pulsating}$. It is worth to outline that the power switch is turned-on and off during ZPs of the DC link voltage, in such a way that both the transitions of the switch are performed in ZVT.

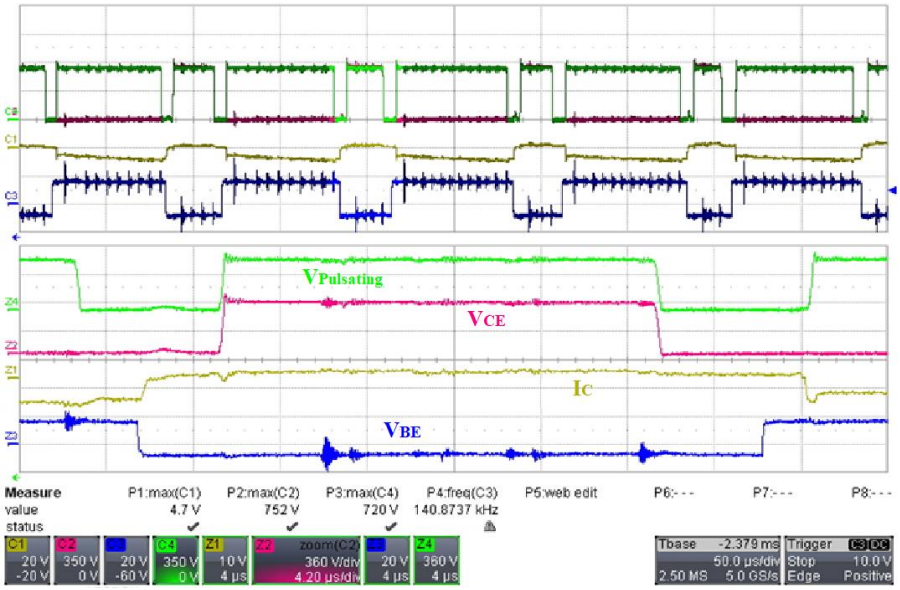

Figure 104 – Top plot: commutations of switch Rn during the intermediate state of phase R: DC link voltage, $V_{Pulsating}$, in green, Collector-Emitter voltage, V_{CE}, in red, Collector current, I_C, in yellow, Base-Emitter voltage, V_{BE}, in blue. Bottom plot: details of the waveforms in the highlighted area.

Moreover, we can note that the voltage V_{CE} follows the evolution of the pulsating DC link voltage when the switch is off. Consequently, the switching losses of the VSI stage are minimized thanks to the synchronization between the ZPs of the Pulsating DC link and the transitions of the switches of the inverter stage. Therefore also considering the ZVZCT turn-on and off at low energies of the active Clamp, the power

stages based on IGBT modules are affected only by conduction losses thanks to the modulation technique and the operation of the Clamp.

As seen in the section 4.2.1 the Clamp capacitor is connected to the output of the first stage for the entire energising phase, influencing the commutations of both legs of this latter. For this reason the commutations of both legs have been analysed, focusing the attention on the consecutive energy pulses in the whole energising phase. Figure 105 reports the evolution of the voltage across the low side switch of the leading leg, the current on the primary side of the transformer, the driving signal and the switched current of the low side switch in the case of V_{IN}= 670V and P_{OUT}= 4 kW.

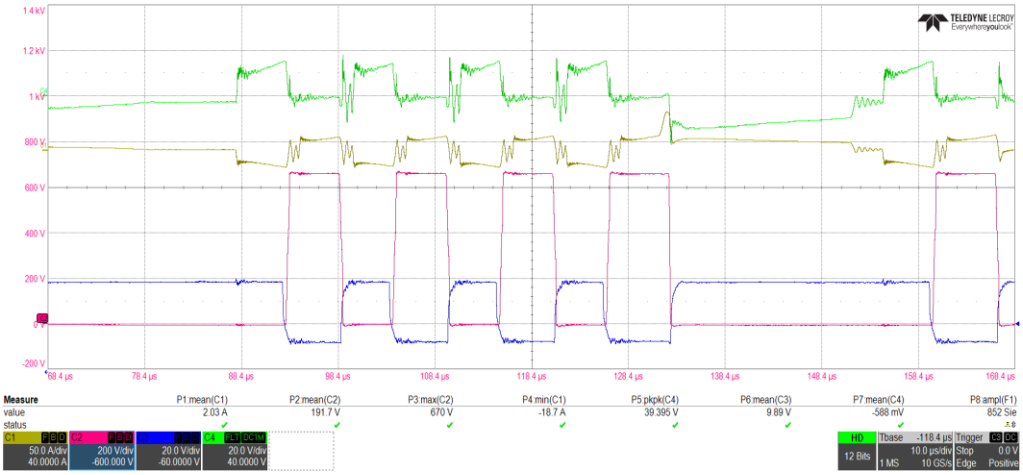

Figure 105 – Detail of the commutations of leading leg for V_{IN}= 670 V and P_{OUT}= 4kW (in yellow the primary current on the transformer, in red the V_{DS} of low side switch, in blue the V_{GS} of low side switch and in green the current of lower switch)

We can note that only the turn-on of the low side switch happens in ZVZCS condition while the other are not soft due essentially to the commutation on the Clamp capacitor. The current on the primary is used to show the different energising phases of the first stage and simplify the analysis. Figure 106 reports the evolution of the voltage across the low side switch of the legging leg, the current on the primary transformer, the driving signal and the switched current of the low side switch in the case of V_{IN}= 670V and P_{OUT}= 4 kW.

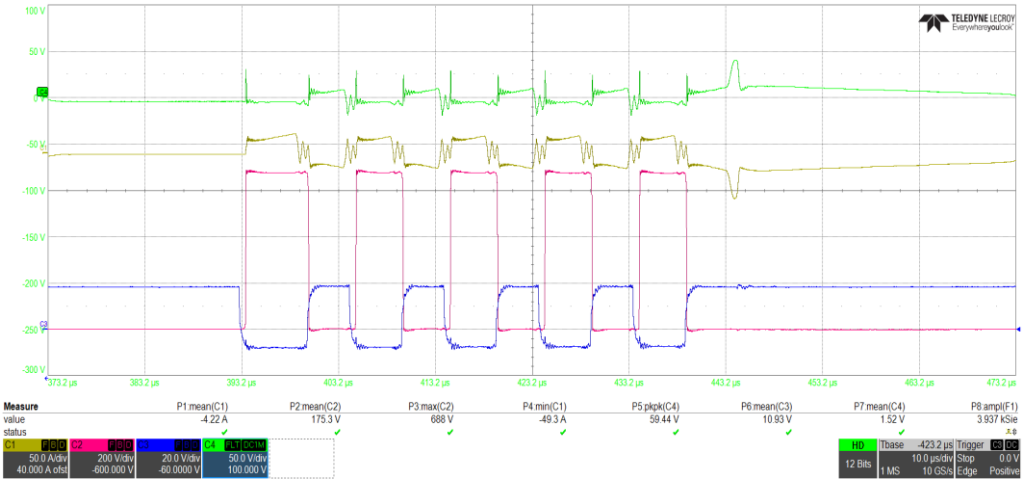

Figure 106 - Detail of the commutations of legging for V_{IN}= 670 V and P_{OUT}= 4kW (in yellow the primary current on the transformer, in red the V_{DS} of lower switch, in blue the V_{GS} of lower switch and in green the current of lower switch)

The above figure shows that the legging leg doesn't present any commutations in soft-switching condition due to the particular operation of the Active Clamp in the proposed modulation technique.

5.4.1 Analysis output voltage quality and effects of the predistortion technique

The characterization of the prototype was continued with the analysis of the output phase voltage for different load conditions, to see the effects of the Pulsating DC link voltage on the output distortion. Moreover, the predistortion technique of the modulating references has been implemented and tested to show the beneficial effects on the voltage distortion, specifically for low values of the output power. The achieved results are presented below for each load conditions in the following conditions:

- Without predistortion of modulating signals: In this case purely sinusoidal references are used for modulating the switches of the VSI stage.
- With predistortion of modulating signals: In this case the references are pre-distorted, through the injection of weighted harmonic voltages to compensate the distortion of the output voltage. As presented in the fourth chapter, the harmonic voltage and the relative weights are selected using an iterative procedure based on simulations and frequency analysis of the output voltage.

The measured waveforms of line to line voltage and phase current are reported in Figure 107 for V_{in}=700V and P_{OUT}=4.1 kW without and with the predistortion of the modulating references.

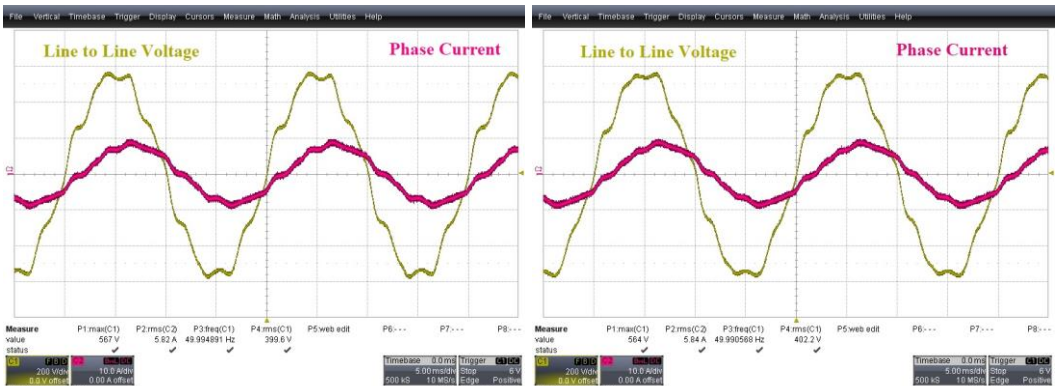

Figure 107 – Output voltage (yellow) and phase current(red) for resistive load of P_{OUT}=4.1kW, VIN=700V and fs_{PSB}=60kHz without predistortion (left) and with predistortion (right) of modulating signals

Figure 108 and Figure 109 show the waveforms of line to line voltage and phase current for V_{IN}=600V without and with the predistortion of modulating signals, for P_{OUT}=10 kW and P_{OUT}=20 kW, respectively.

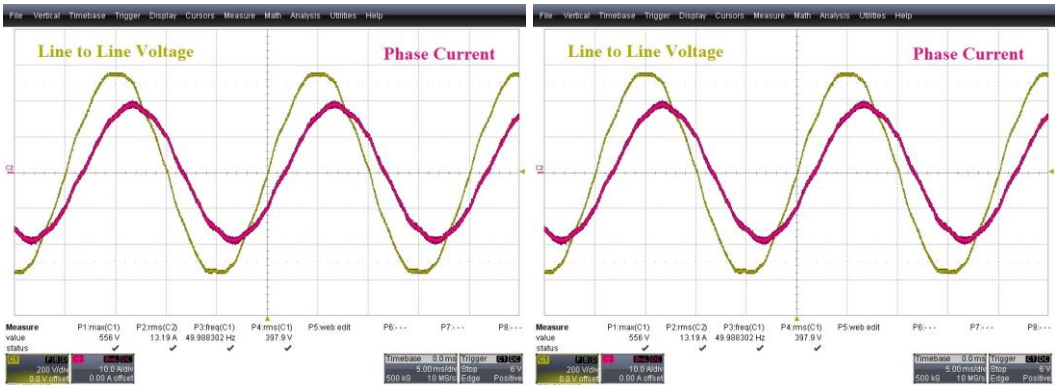

Figure 108 – Output voltage (yellow) and phase current(red) for resistive load of P_{OUT}=10kW, VIN=600V and fs_{PSB}=60kHz without predistortion (left) and with predistortion (right) of modulating signals

Comparing the evolution of the waveforms reported in the figures, we can note that the predistortion technique is fundamental to improve the quality and shape of the

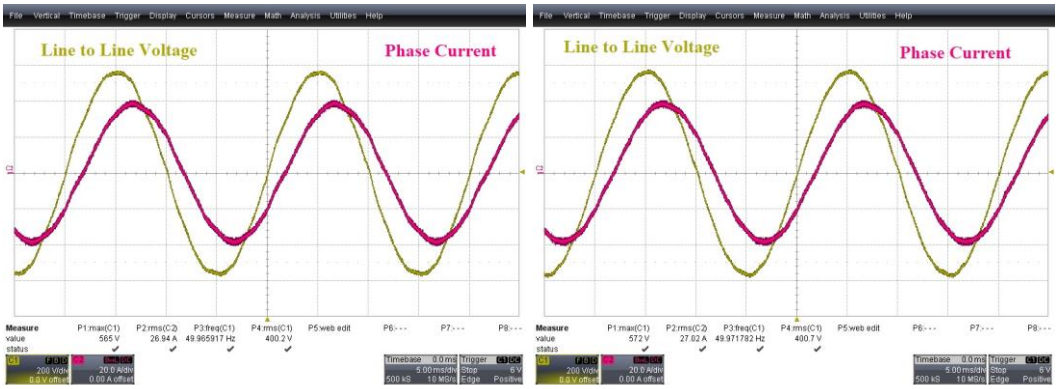

Figure 109 – Output voltage (yellow) and phase current(red) for resistive load of P_{OUT}=20kW, VIN=600V and fs_{PSB}=60kHz without predistortion (left) and with predistortion (right) of modulating signals

voltages, mostly for low output power. Moreover, the proposed method also improves the performances and the shape of the voltage for high output power, as shown in the figures. To evaluate the impact of the proposed modulation technique and the effects of the predistortion on the harmonic content of the output voltage, a frequency analysis has been performed for the experimental tests analysed previously. Then the results of the frequency analysis have been compared with the harmonic voltage limits of the EN 50160 standard, which defines the maximum value of each harmonic expressed in percent of the fundamental amplitude. The voltage constraints of the EN 50160 standard, classified as function of the harmonic types, are highlighted in Figure 110. Usually the frequency analysis and the verification of the compliance with the limits of the standard are extended up to the 50th, since beyond this harmonic the voltage amplitudes are negligible.

Odd harmonics				Even Harmonics	
Not triplen		Triplen			
Harmonic order (n)	Relative Voltage (L_i)	Harmonic order (n)	Relative Voltage (L_i)	Harmonic order (n)	Relative Voltage(L_i)
5	6%	3	5%	2	2%
7	5%	9	1.5%	4	1%
11	3.5%	15	0,5%	6…10	0.5%
13	3%	21	0.5%	>10	0.2%
17	2%	>21	0.2%		
19	1.5%				
23	1.5%				
25	1.5%				
>25	0.2+32.5/n				

Figure 110 – Voltage harmonic limits of the standard EN 50160

The results of the frequency analysis are reported in Figure 111, Figure 112 and Figure 113, where the measured harmonic components of the output voltage are compared with the mask of EN 50160 standard to verify their compliance.

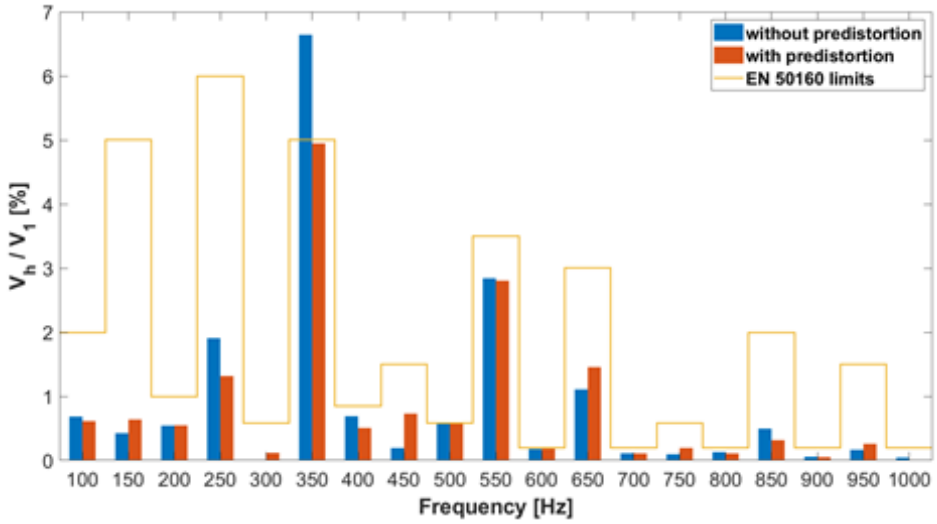

Figure 111 – Frequency analysis of the output voltage and compliance with harmonic limits for resistive load of P_{OUT}=4.1kW, V_{IN}=700V and fs_{PSB}=60kHz without predistortion and with predistortion.

The analysis was made up to 1kHz since the amplitude of the higher harmonics can be neglected due to the lowest values. Moreover, the harmonics that give problems to the proposed modulation technique are in the low frequency range (i.e. 5^{th}, 7^{th}, 11^{th} and 13^{th}). Analysing the experimental results, we can observe that the harmonic spectrum for the high output power is compliant with the limits both with and without the predistortion. In the high power cases the predistortion has a beneficial effect on the low frequency harmonics (up to 500Hz), feature required in applications as electrical drives to reduce the noise and mechanical stress of the system.

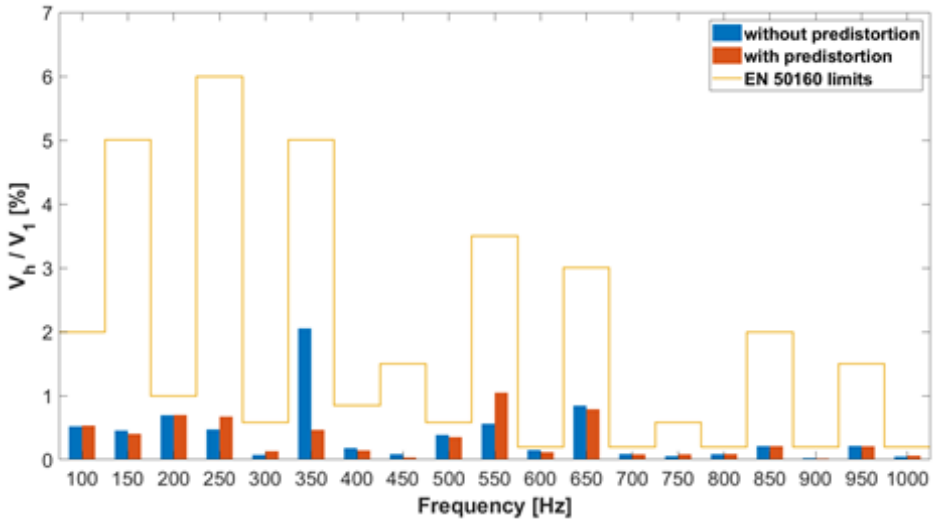

Figure 112 – Frequency analysis of the output voltage and compliance with harmonic limits for resistive load of P_{OUT}=10kW, V_{IN}=600V and fs_{PSB}=60kHz without predistortion and with predistortion.

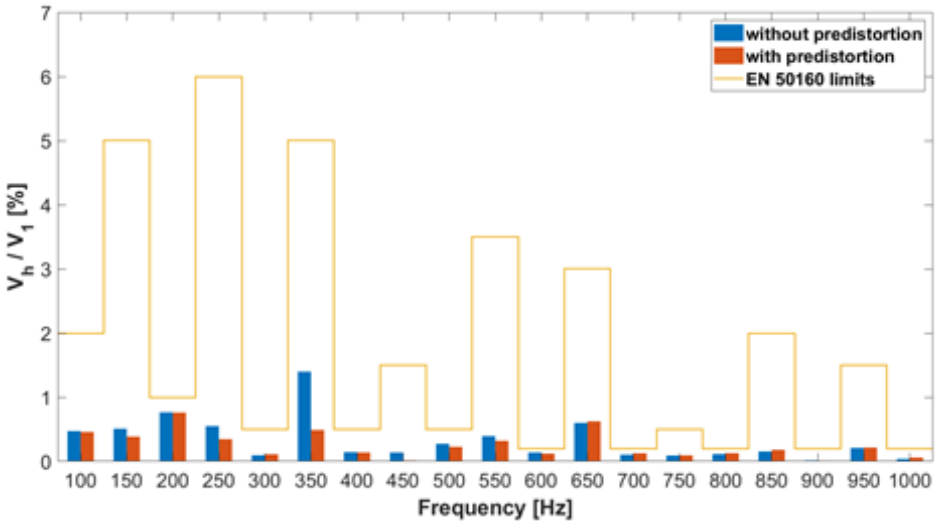

Figure 113 – Frequency analysis of the output voltage and compliance with harmonic limits for resistive load of P_{OUT}=20kW, V_{IN}=600V and fs_{PSB}=60kHz without predistortion and with predistortion.

Instead in the case of low output power the predistortion technique and its effects are essential to be compliant with the pollution limits as shown in Figure 111, where the predistortion allows the reduction of the 7th harmonic amplitude making it compliant with corresponding standard limit.

To complete the analysis we have to outline that the results of proposed modulation technique are largely affected by the characteristics of the output three phase filter

which was optimised for higher output power. Consequently the characteristics of this filter negatively affect the harmonic response of the converter at low output power. The negative effects of the filter is attenuated by the modulation technique and particularly the predistortion technique which were used just to comply with the pollution limits.

CONCLUSIONS

This thesis proposes an innovative multistage DC/AC topology based on the Pulsating DC link principle that, thanks to the elimination of intermediate filter and the use of an opportune modulation technique, allows the improvements of the overall reliability and efficiency. First of all the DC/AC topology is reviewed, focusing the attention on the architecture based on two power stages connected through a fixed DC link and subsequently on the new topologies. Moreover, all the challenges relative to the improvements of the features of this application field are presented and discussed, highlighting the role of the WBG devices. Then the proposed architecture of PDLC has been presented and analysed, focusing the attention on its main features. A complete analysis of the topology during the energising phases was presented, providing the equivalent simplified circuit of the PDLC and the relative differential equation system. To analyse the main characteristics of the converter and the interaction between the power stages during the energising phases, a multiparametric analysis based on LTspice simulation has been performed for different combinations of the main influence parameters. The achieved results have been used to provide some design guidelines of the main components, as the transformer and the Active Clamp circuit.

An overview of the desired features of modulation techniques for topology based on Pulsating DC link principle was presented as well as the review of the different techniques presented in the literature. More space was given to the techniques based on ZVT of the Inverter stage thanks to the interesting effects on the efficiency of the power converter. Specifically two different modulation techniques based on the ZVT of the VSI stage and their implementations are presented, highlighting the different operating principles and the relationship between the switching frequencies of the power stages. Two different versions of the proposed topology prototype were presented, providing details on the power devices used and showing the experimental setup used for their test. Finally the experimental results of the complete characterization of the prototype were presented, to validate the previous analysis and simulation results. In particular, the experimental results have confirmed the

fundamental role of the Active Clamp in the operation of the PDLC topology, thanks to the mitigation of the overvoltage and the interaction with the other power stages. Moreover, the achieved results with both the modulation techniques, have demonstrated the feasibility to use the ZPs of the intermediate DC link for the ZVT of the VSI stage. Regarding the quality of the output voltages, both the analysed technique have provided excellent results in terms of the distortion thanks to optimisation of the operating principle and/or the use of the predistortion technique.

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