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RESEARCH ARTICLE

On the Vulnerability of UMOSFETs in Terrestrial Radiation Environments

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ABSTRACT The vulnerability of prominent silicon-based U-shaped Metal-Oxide-Semiconductor Field Effect Transistors (UMOSFETs) to destructive radiation effects when operating in terrestrial atmospheric environments is investigated. Secondary particles from nuclear reactions between atmospheric neutrons and the constituent materials of electronic devices can trigger Single-Event Burnout (SEB), a destructive failure in power MOSFETs. The susceptibility of UMOSFETs to SEBs induced by atmospheric neutrons in accelerated tests is compared to that of similarly rated traditional Double-diffused MOSFETs (DMOSFETs) counterparts. Computational simulations are conducted to elucidate the failure mechanisms and propose strategies to potentially enhance the survivability of next-generation UMOSFETs in high-reliability power systems operating on Earth.

INDEX TERMS Radiation effects, power transistor, UMOSFET, trench MOSFET, DMOSFET, atmospheric neutrons, single-event effect, single-event burnout, single-event gate rupture.

I. INTRODUCTION

The U-shaped Metal-Oxide-Semiconductor Field Effect Transistor (UMOS or trench FET) is currently one of the most widely used semiconductor power devices worldwide [1]. The UMOS technology is continuously supplanting and is often preferred over the traditional Double-diffused MOS (DMOS) technology due to advantages such as higher transistor cell density, uniform epitaxial current distribution, lower on-resistance, and reduced gate charge [1], [2]. Figure 1 illustrates the structural differences between DMOS and UMOS devices. However, the behavior of UMOS devices under ionizing radiation has not yet been extensively studied. Radiation, including photons, neutrons, electrons, protons, and heavy ions, can damage these devices through total ionizing dose, displacement damage, or charge deposition by single particles, known as Single-Event Effects (SEEs) [3]. Destructive SEE failure modes in power MOSFETs include Single-Event Gate Rupture (SEGR) and Single-Event Burnout (SEB) [4].

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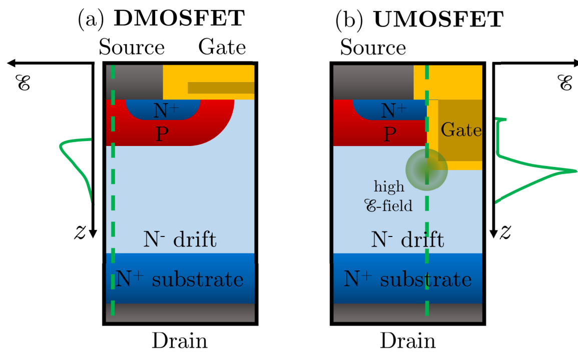

FIGURE 1. Half-cell cross sections of (a) planar DMOS and (b) UMOS power FETs. Electric field distributions at the positions marked by the dashed green lines are also depicted.

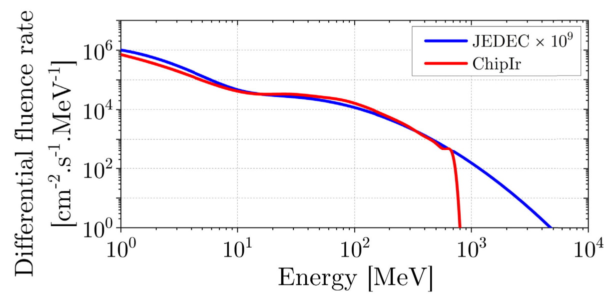

FIGURE 2. JEDEC and ChipIr neutron differential fluence rate as a function of neutron kinetic energy. After [22] and [24].

In terrestrial environments, SEB induced by atmospheric neutrons poses a critical challenge for modern power electronics reliability at ground level and flight altitudes [5], [6]. Although substantial research has been conducted on destructive radiation effects in DMOS transistors [7], [8], relatively few studies have addressed power FETs with alternative technologies. Over the past decade, the lack of comparative studies on similarly rated UMOS and DMOS devices has been highlighted as a critical gap in the literature [9]. Existing research on SEB in silicon (Si)-based UMOSFETs has primarily focused on space applications, relying on computational simulations [10], [11], [12], [13] and limited experimental data [14], [15]. An existing computational study concluded that Si UMOS devices might be more resistant to SEB than DMOSFETs [10]. Detailed comparative SEB studies in silicon-carbide (SiC) UMOS and DMOS power FETs have been recently published, concluding that UMOSFETs exhibit higher SEB tolerance when exposed to protons and neutrons [16], [17]. Despite these advances, detailed and comparative studies of SEB in Si-based UMOS and DMOS power FETs are still lacking.

The apparent robustness of SiC UMOSFETs cannot be directly extrapolated to Si UMOSFETs, as the SEB mechanism in SiC devices is still under debate. It has been argued that the charge multiplication mechanisms responsible for SEB in Si MOSFETs may be suppressed in SiC devices [16]. Preliminary comparative studies on Si-based devices have revealed that UMOSFETs may prematurely exhibit enhanced charge multiplication effects, compared to DMOS counterparts, under monoenergetic fast neutron irradiation [18], [19], [20]. These findings suggest that UMOSFETs might be more prone to SEB mode than previously predicted by computational simulations, emphasizing the need for further experimental investigations. Assessing potential failure risks in the UMOS technology under atmospheric neutrons is crucial before its incorporation into avionics systems and ground-level applications demanding high reliability. Moreover, the prominence of UMOS devices in modern power electronics and the ubiquity of atmospheric neutrons underscore the significance of the present investigation.

In this study, the relative vulnerability of Si-based UMOSFETs to SEBs induced by quasi-atmospheric neutrons compared to DMOSFET counterparts is experimentally assessed. Failure rates are estimated from experimental data and implications for ground-level and avionics applications are discussed. Simulations provide insights into the neutron-induced SEB mechanism and potential reinforcement improvements.

II. MATERIALS AND METHODS

Currently, only a limited number of specialized spallation facilities worldwide are capable of providing neutron beams that replicate atmospheric neutron conditions for accelerated radiation testing. Experimental investigations were conducted by using the ChipIr instrument, at the ISIS Neutron and Muon Source facility, UK. ChipIr provides an intense neutron beam with an energy spectrum similar to that measured in terrestrial environments under reference conditions [21], [22], as specified by the JEDEC standard JESD89B (sea level, cutoff = 2.08 GV, mid-level solar activity, outdoors) [23], [24]. Figure 2 compares the neutron energy spectra of the quasi-atmospheric ChipIr beam and the JEDEC atmospheric standard. Although the spectra are similar, the ChipIr spectrum is limited to energies below 800 MeV due to the maximum energy allowed by the ISIS synchrotron.

Computational simulations using the G4SEE toolkit [25] were conducted to verify the impact of the ISIS synchrotron energy cutoff on emulating the JEDEC spectrum, and to identify the nuclear reaction secondaries most responsible for SEB occurrence. Figure 3 presents simulations of the energy deposition distributions from neutron-induced secondary particles within the epitaxial region of a generic Si-based 150 V MOSFET. The hypothetical MOSFET was defined with a 5 μm Al metallization layer, a 13.5 μm epitaxial layer, and a 286.5 μm substrate. The similarity of deposited energy distributions per nuclear reaction channel confirms that the ISIS synchrotron energy cutoff has minimal impact on accurately emulating the atmospheric neutron environment with the ChipIr neutron beam. Additionally, technology computer-aided design (TCAD) simulations using ECORCE software [26] were conducted to analyze the experimental findings and support the interpretation of

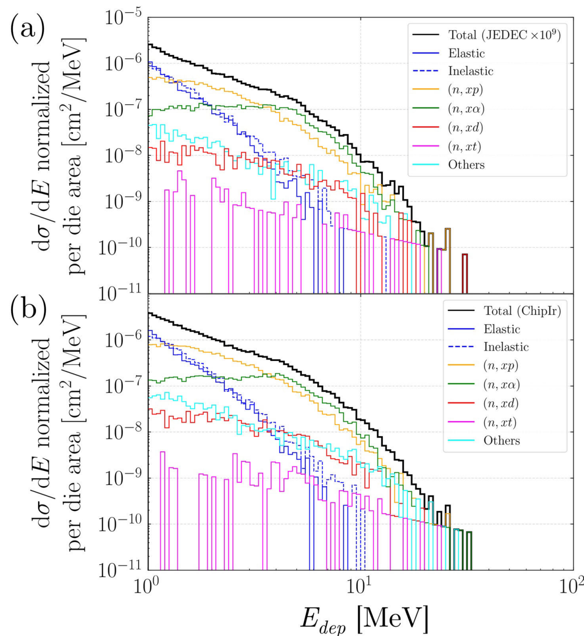

FIGURE 3. Differential cross section distributions of energy deposition within the epitaxial region of a generic 150 V-rated MOSFET resulting from nuclear reactions induced by JEDEC and ChipIr neutrons. In our classification, (n, xd) and (n, xt) denote reactions producing at least one deuteron (d) and triton (t), respectively. Channels (n, xp) and ($n, x\alpha$) represent reactions in which protons (p) and alpha particles (α), respectively, are the predominant ejectiles. Simulated using G4SEE [25].

the underlying mechanisms of neutron-induced SEB in Si UMOSFETs. For simplicity, simulations were performed on generic 150 V-rated UMOS and DMOS structures with representative parameters. Design parameters of the drift layer were estimated according to well-established semi-empirical expressions derived from Baliga's power law, whereas taking into account the influence of edge termination in practical power MOSFETs [27]. Other design parameters were adapted from numerical examples presented in [28] for similarly rated UMOS and DMOS devices. The physics models used in the simulations account for impact ionization and band-to-band tunneling generation; Shockley-Read-Hall and Auger recombination; effective separation of electron-hole pairs generated by irradiation (yield function); band-gap narrowing; and carrier mobility dependencies on electric field, doping concentration, and free carrier density [26].

Several n-type UMOS and DMOS power FETs with nominal voltage ratings of 40 V, 60 V, and 150 V were irradiated from the front side at neutron fluences of up to 10^{10} neutrons/cm^2. The devices under test (DUTs) were irradiated as a function of the drain-source voltage (V_{DS}), supplied by a source measure unit (Keithley 2410), while operating in the non-negative gate OFF-state regime ($V_{GS} = 0$ V and $V_{DS} > 0$ V). At least two devices of each part were tested following a standard method for protective evaluation of SEB by using the current limiting technique [29]. The current-limiting technique is the primary

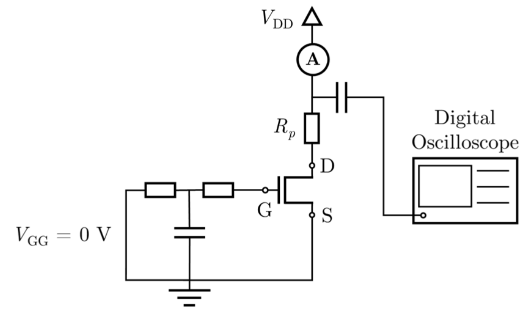

FIGURE 4. Schematic circuit diagram for protective SEB cross section measurements in power devices. Based on [29].

method for protective SEB testing [7], [29], [30], enabling statistical assessment of reliability metrics, such as failure-in-time (FIT) rates and mean time to failure (MTTF) [31], within a feasible experimental timeframe. Figure 4 shows the schematic diagram of the SEB protective circuit, which basically consists of a *R-C-R* network to prevent gate damage and a protection resistor on the drain to limit overcurrent [7]. SEB causes a transition from the OFF-state to a temporary ON-state, and the SEB-type pulses can be captured by using an oscilloscope. The adopted failure criterion is similar to that presented in [32], with the SEB signals monitored with a digital oscilloscope (InfiniiVision DSOx4024A) configured with a −30 mV trigger level. Figure 5 exhibits the experimental setup.

III. RESULTS AND DISCUSSION

Under the OFF-state bias conditions adopted in our study, SEB was verified to be the dominant neutron-induced destructive failure mode. Except for 150 V UMOSFETs, all other devices exhibited successful protection against SEB, maintaining low drain-source leakage current (I_{DSS}) and nominal gate-source threshold voltages (V_{th}). However, for the 150 V UMOSFETs operating at high voltage, the protective circuitry was occasionally ineffective, resulting in sudden increases in I_{DSS} to the milliampere range (fatal events). Post-irradiation characterization confirmed permanent drain-source damage in some 150 V UMOSFETs, with the gate remaining functional, although V_{th} was increased. In other cases, both drain and gate damage were observed in 150 V UMOSFETs, suggesting combined SEB and SEGR occurrence. No such combined SEB and SEGR effects were observed in DMOSFETs. Figure 6 compares recorded signals of a successfully protected SEB (black) with a fatal event (red), highlighting that both signals are nearly identical except for the drain-source damage in the latter. In cases where the circuit failed to protect against neutron-induced destructive failures, the damaged devices were replaced, and voltage levels were reset before resuming measurements.

The SEB sensitivity of the DUTs was evaluated in terms of the SEB cross section [8]:

$$\sigma_{SEB} = \frac{N_{SEB}}{\Phi}, \quad (1)$$

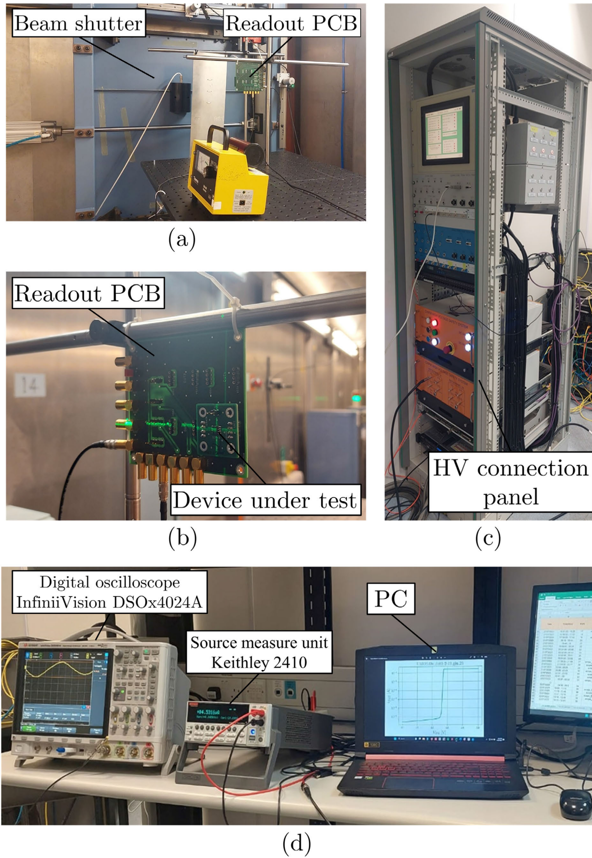

FIGURE 5. Experimental setup for quasi-atmospheric neutron irradiation of power transistors by using the ChipIr instrument, UK. (a) Overview of the setup with a device under test (DUT) positioned for frontal irradiation in the experimental room. (b) Laser alignment of the DUT and readout printed circuit board (PCB) along the neutron beam axis. (c) Connection panel linking the control and experimental rooms, including the high-voltage safety system. (d) Control room equipment connected to the DUT via the connection panel.

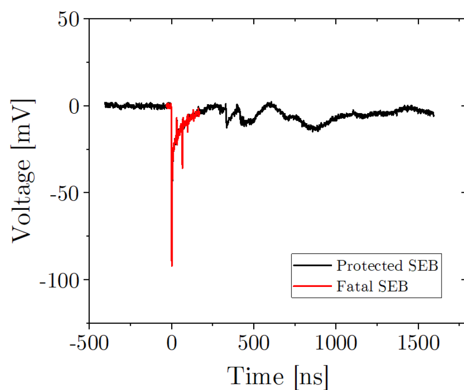

FIGURE 6. Representative SEB signals recorded on the oscilloscope. The black line represents a neutron-induced SEB successfully protected by the test circuit, allowing the device under test to remain operational and withstand high voltage. The red line represents a fatal SEB, where the protective circuitry fails to prevent drain-source damage, resulting in an I_{DSS} increase to the milliampere range.

defined as the ratio of the total number of detected SEB signals (N_{SEB}) to the particle beam fluence (Φ) for each

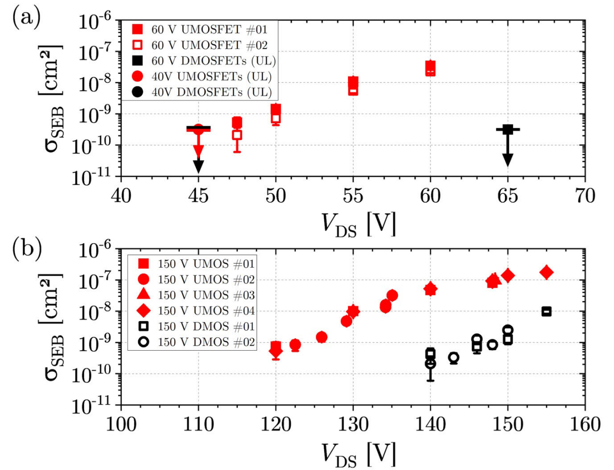

FIGURE 7. SEB cross section measurements of 40 V-, 60 V-, and 150 V-rated UMOS and DMOS power FETs irradiated with quasi-atmospheric neutrons at ChipIr, UK. The arrows denote the upper limits (UL) at the 90% confidence level where no SEBs were observed. (a) 40 V and 60 V-rated devices. (b) 150 V-rated devices. Tested devices are identified by enumeration label.

test run. The SEB cross section quantifies the likelihood of SEB occurrence, reflecting the cross-sectional area of the device's sensitive volume that effectively contributes to triggering SEBs. As shown in Fig 7, the σ_{SEB} measurements as a function of V_{DS} are plotted for SEBs induced by quasi-atmospheric neutrons in UMOS and DMOS power FETs. No SEBs were observed in either 40 V UMOS, 40 V DMOS, or 60 V DMOS devices, even when irradiated at drain-source voltages very close to their actual breakdown voltages (BV_{DS}). Consequently, 90% confidence level upper limits (UL) for σ_{SEB} are indicated by arrows in Fig 7(a) for these cases. In contrast, SEBs were observed in 60 V UMOSFETs at voltages as low as $V_{DS} = 47.5$ V. The maximum SEB cross section measured for the 60 V UMOSFET was approximately two orders of magnitude higher than the upper limit estimated for the 60 V DMOSFET. Figure 7(b) shows a similar trend for 150 V devices, with SEBs being triggered from approximately $V_{DS} = 120$ V in UMOSFETs, compared to about $V_{DS} = 140$ V in DMOSFETs. Comparatively, SEB cross sections are higher for 150 V UMOSFETs.

In order to accurately determine safe operating voltages across technologies and directly compare their SEB susceptibilities, it is advantageous to evaluate the σ_{SEB} values normalized per die area as a function of the V_{DS} values normalized per the actual breakdown voltage BV_{DS}. Figure 8 presents the dependence of the normalized SEB cross sections on the applied voltage ratio of the DUTs. By fitting Weibull statistical distributions to experimental data, the SEB threshold voltages are determined. Results reveal that SEB can initiate in UMOSFETs at voltage ratios as low as approximately 66% of BV_{DS}, compared to a threshold of around 88% for DMOSFETs. As shown in Fig 8, the typical security derating level of 75% [33] is insufficient to completely prevent SEB in UMOSFET parts rated as

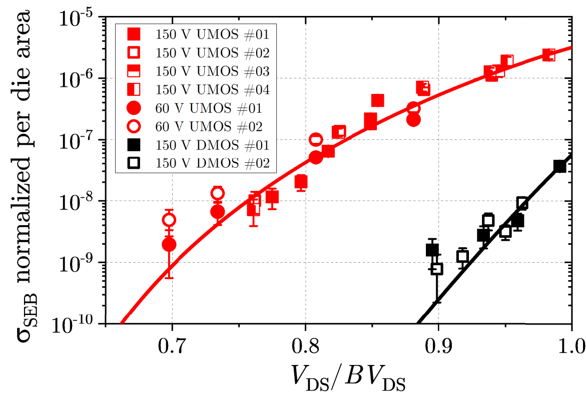

FIGURE 8. SEB cross section measurements normalized per die area as a function of the applied drain-source voltage normalized per actual breakdown voltage, according to precision measurements. Tested devices are identified by enumeration label. Solid curves represent the Weibull curve fits to experimental data.

low as 60 V. Furthermore, near the maximum operational voltage level, normalized SEB cross sections of UMOS and DMOS differ by two orders of magnitude, confirming the intrinsic vulnerability of UMOSFETs regardless of die area dimensions.

Assuming the ChipIr neutron spectrum closely resembles the JEDEC reference spectrum, SEB failure rates induced by atmospheric neutrons can be estimated for any location and condition on Earth by re-scaling the reference neutron fluence rate [23], [24]. Under reference conditions, the average Single-Event Rate (SER) can be computed as follows [23]:

$$\mathrm{SER} = \int \sigma(E)\, \frac{d\phi(E)}{dE}\, dE \; = \sigma_{\mathrm{SEB}}\, \phi_{ref} \,, \tag{2}$$

where $d\phi/dE$ is the reference neutron differential fluence rate, as shown in Fig 2, and $\phi_{ref} = 12.95$ neutrons.cm^{-2}.h^{-1} is the reference neutron fluence rate, according to the JEDEC standard [23]. For instance, when expressed in conventional FIT units (failures per 10^9 h), the estimated SEB failure rates for the 60 V UMOS, 150 V DMOS, and 150 V UMOS devices operating at nominal voltage and reference sea level are 450(60) FIT, 32(7) FIT, and $1.8(3) \times 10^3$ FIT, respectively. The UMOS devices exceed the specific 100 FIT reliability requirement stipulated by the JEDEC standard JEP151A [34], whereas the 150 V DMOS does not. The MTTF for SEB occurrence in these 60 V and 150 V UMOSFETs operating at nominal voltage and sea level are 250(30) years and 63(11) years, respectively. At a commercial aviation altitude of 12 km, where the neutron fluence rate increases by about 500 times [24], the corresponding MTTF values reduce to 0.51(7) year and 0.127(22) year, respectively. According to JEDEC standards, these UMOS failure rates are unacceptable for avionics and inadequate for traction and automotive applications at ground level.

The SEB mechanism in Si-based power devices involves impact ionization and carrier tunneling, which are strongly dependent on the local electric field intensity [35]. This fact suggests that the UMOS vulnerability is likely due to electric field stresses present near its trench corner (see Fig 1), which are substantially more intense than those found in similarly rated DMOS structures [28]. These intense fields can enhance multiplication of charge carriers produced by neutron-induced secondary particles, triggering avalanche multiplication, activating the parasitic bipolar junction transistor (BTJ), and, under critical conditions, ultimately lead to SEB. The neutron-induced SEB can be interpreted in terms of the Egawa effect [36] and current-induced avalanche breakdown [37]. According to the Poisson equation, the electric field ($\mathscr{E}$) gradient is affected by the effective charge carrier distribution within the epitaxial region [37]:

$$\frac{d\mathscr{E}}{dx} = \frac{q}{\varepsilon}[N_d - n(x)] = \frac{q}{\varepsilon}\left(N_{epi} - \frac{J}{q\, v_{sat}}\right), \tag{3}$$

where $N_d = N_{epi}$ is the epitaxial region doping concentration, and $J \cong q\, v_{sat}\, n(x)$ is the drift current density of carriers induced by secondaries. Under avalanche conditions, $n(x)$ increases due to ionization impact. When $n(x) \gg N_{epi}$, the electric field peak is shifted toward the epitaxial-substrate interface due to the Egawa effect [38]. Whether the maximum electric field intensity exceeds the semiconductor critical field ($\mathscr{E}_{max} > \mathscr{E}_{crit}$), a SEB occurs [37]. For silicon, $\mathscr{E}_{crit} \approx 3 \times 10^5$ V/cm [37].

Coupled G4SEE and TCAD simulations were conducted to exemplify the previously mentioned mechanism, elucidating the experimentally observed UMOSFET vulnerability. Based on Fig 3, post-processing analysis indicates that high-energy protons generally escape the epitaxial volume with minimal energy deposition, whereas the most energetic events usually involve residual heavy nuclei and alpha particles. For instance, one of the highest-energy events was initiated by a 243.2 MeV primary neutron, which produced a 70.1 MeV secondary neutron, a 128 MeV proton, and a 25.7 MeV ^{27}Al ion. These secondary particles deposited energies of 0 keV, 5 keV, and 23.9 MeV, respectively. Due to the negligible energy deposition by high-energy protons, this particular event has been selected as the simplest representative worst-case scenario for atmospheric neutron-induced SEB, where only the ^{27}Al ion can be considered in the TCAD simulations for convenience. The simulated doping profiles followed the geometry shown in Fig 9, with doping concentrations defined as specified in Table 1. Figure 9 shows the distributions of peak electric field after neutron-induced SEE in 150 V-rated devices for the representative case described earlier. In both UMOS and DMOS operating at $V_{\mathrm{DS}} = 150$ V, the electric field peak shifts toward the epitaxial-substrate interface, exceeding $\mathscr{E}_{crit}$ and initiating SEB. Complementary TCAD simulations at $V_{\mathrm{DS}} = 130$ V align with the experimental results shown in Fig 7(b), where neutron-induced SEB occurs in the 150 V UMOS but not in the 150 V DMOS under the same condition. Being consistent with experimental results and the analytical

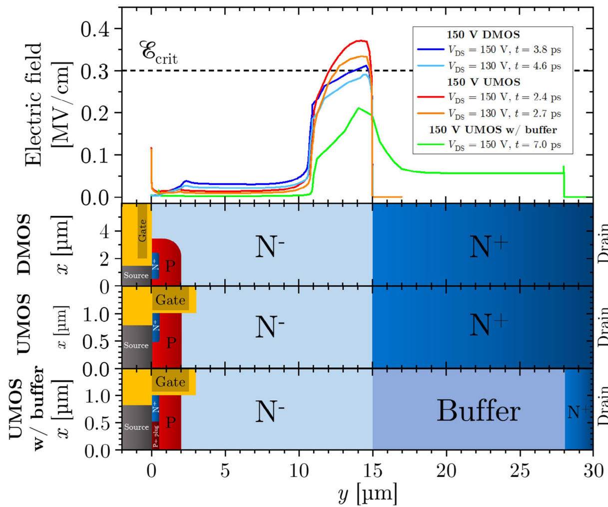

FIGURE 9. Spatial distributions of the peak electric field after neutron-induced SEE in 150 V-rated DMOS, UMOS, and UMOS with buffer layer devices. Based on G4SEE simulation, a secondary 25.7 MeV ^{27}Al ion, created at $x = 0.5$ μm, $y = 0$ μm, is emitted in the y direction at $t = 0.2$ ps. Given the minimal energy deposition of the accompanying 128 MeV proton, only the ^{27}Al ion is considered in simulations using ECORCE [26].

interpretation (3), the TCAD simulations corroborate that UMOS devices are indeed more vulnerable to SEBs.

Experimental results demonstrate that current UMOSFET designs are inadequate for high-reliability applications in atmospheric radiation environments. However, simulations suggest that incorporating a properly doped buffer layer [39] can mitigate neutron-induced SEB by reducing peak electric fields after a particle strike, as shown in Fig 9. It is shown that the buffer layer reduces the electric field peak to safe levels after particle strike, effectively preventing premature SEB occurrence in the UMOSFET structure. Previous studies have shown that buffer layers significantly improve SEB performance of DMOSFETs [39], [40], [41]. Recent investigations also confirm that buffer layers enhance SEB hardness in split-gate UMOSFETs under 2 GeV tantalum irradiation [15]. Although such high-energy heavy-ion irradiation conditions are not representative of nuclear reaction secondaries in atmospheric environments, these results suggest that similar radiation hardness can be achieved in next-generation UMOSFETs incorporating buffer layers. Further research is required to optimize buffer layer design for power UMOSFETs and evaluate its effectiveness against neutron-induced SEB in atmospheric environments.

Although not the primary focus of this work, other failure mechanisms, such as gate degradation [38], [42] or SEGR [4], can affect the reliability of MOSFETs. Nevertheless, some insights can be drawn by relating these failure modes to our findings on the vulnerability of UMOSFETs to atmospheric neutrons. Recent experimental results have demonstrated that monoenergetic fast neutrons from Deuterium-Tritium (D-T) neutron generators can prematurely induce avalanche multiplication in Si-based power UMOSFETs [18], [19], [20]. In atmospheric environments, due to the greater ionization coefficient of electrons compared to holes, it is likely that ionized electrons produced by nuclear reaction secondaries can enhance the risk of gate degradation through hot-carrier injection during avalanche conditions [2].

TABLE 1. Doping concentrations, in units of cm^{-3}, adopted in TCAD simulations with ECORCE software [26].

Region	150 V DMOS	150 V UMOS	150 V UMOS with buffer
n^+-source	1.00×10^{19}	1.00×10^{19}	1.00×10^{19}
n^+-drain	1.00×10^{20}	1.00×10^{20}	1.00×10^{20}
n^--drift	1.47×10^{15}	1.47×10^{15}	1.47×10^{15}
p-base	1.00×10^{17}	1.00×10^{17}	1.00×10^{17}
p^+-plug	-	-	1.00×10^{19}
n-buffer	-	-	1.00×10^{16}

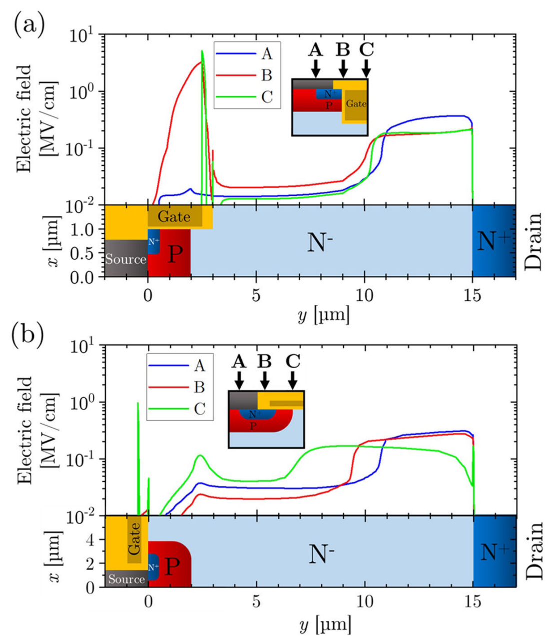

FIGURE 10. Spatial distributions of the peak electric field in 150 V-rated (a) UMOS and (b) DMOS devices following secondary ion impacts at distinct positions. Graphs presented in logarithmic scale. Simulated using ECORCE [26].

Furthermore, the increased risk of SEGR is illustrated in Fig 10, which presents TCAD simulations of peak electric field distributions in generic 150 V-rated UMOS and DMOS devices for different secondary ion impact positions. Depending on the location of the nuclear reaction secondary incidence, intense electric field spikes can form across the gate oxide. Whether the peak electric field exceeds the dielectric strength of SiO_2 (approximately 10 MV/cm [43]), SEGR can occur, leading to catastrophic gate oxide rupture.

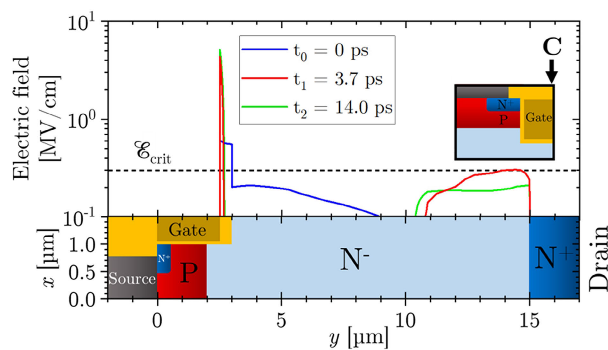

FIGURE 11. Temporal evolution of the electric field distributions in 150 V-rated UMOS following secondary ion impact over the trench gate column (position C) at $t = 0.2$ ps. Simulated using ECORCE [26].

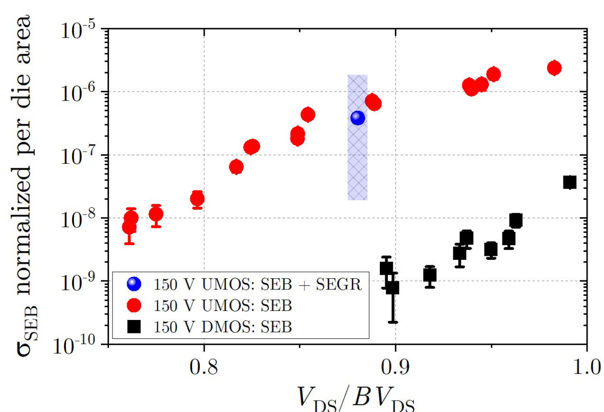

FIGURE 12. Normalized cross section of combined SEB and SEGR failure in 150 V-rated UMOSFETs compared to the pure SEB cross section measurements. The blue region indicates the 90% confidence interval.

For instance, Fig 10 indicates that electric field intensities exceeding 5 MV/cm can occur across the gate oxide of the 150 V UMOSFET, which is of the same order of magnitude as the dielectric strength of SiO_2. In contrast, peak electric fields lower than 1 MV/cm are observed across the gate oxide of the 150 V DMOSFET, highlighting the increased vulnerability of UMOSFETs to the neutron-induced SEGR failure compared to DMOSFETs. Similar to how intense electric fields in UMOSFETs promote SEB, it is plausible that neutron-induced SEEs followed by avalanche multiplication can also, in extreme cases, promote SEGR. Figure 11 shows the temporal evolution of the electric field distribution in the 150 V UMOSFET for secondary ion impact occurring over the trench gate column at $t = 0.2$ ps. Simulations reveal that the electric field in the gate oxide continues to increase after the peak electric field in the drift-substrate junction exceeds the critical field of Si at approximately 3.7 ps. These results suggest that the dynamics of combined SEB and SEGR failures, as experimentally observed in some 150 V UMOSFETs, are primarily governed by the SEB mechanism, which is triggered first. This conclusion aligns with experimental data presented in Fig 12, showing the average cross section of combined SEB and SEGR failure for 150 V UMOSFETs. The blue region indicates the 90% confidence interval. Although representing distinct failure mechanisms, the normalized cross section of combined SEB and SEGR failure is statistically compatible with pure SEB cross sections for 150 V UMOSFETs.

IV. CONCLUSION

Unlike SiC-based power FETs and contrary to early computational predictions, experimental results demonstrate that Si-based UMOSFETs are generally more vulnerable and experience SEBs prematurely in terrestrial radiation environments compared to their DMOSFET counterparts. This increased vulnerability is likely attributed to the high local electric fields near the trench corners of UMOSFETs, which favor avalanche multiplication that ultimately initiates SEBs. Failure rates at both reference sea level and flight altitudes indicate that current UMOSFET designs are unsuitable for high-reliability atmospheric applications. Nevertheless, simulations suggest that incorporating a buffer layer in next-generation UMOSFETs can mitigate SEBs induced by atmospheric neutrons, improving device reliability. Experimental and computational findings indicate that SEB is the primary destructive failure mechanism in Si UMOSFETs operating in the non-negative OFF-state regime, whereas SEGR may occur as a secondary effect in combination with SEB under extreme conditions.

REFERENCES

[1] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET: Part I—History, technology, and prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 674–691, Mar. 2017, doi: 10.1109/TED.2017.2653239.

[2] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET—Part II: Application specific VDMOS, LDMOS, packaging, and reliability," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 692–712, Mar. 2017, doi: 10.1109/TED.2017.2655149.

[3] V. A. P. Aguiar, N. H. Medina, N. Added, S. G. Alberton, E. L. A. Macchione, M. A. Guazzelli, M. A. A. Melo, J. A. Oliveira, R. C. Giacomini, F. R. Aguirre, P. R. P. Allegro, H. C. S. Zaggato, and I. J. Sayeg, "Evaluation of funnel models on calculation of ion-induced collected charge," *IEEE Trans. Electron Devices*, vol. 72, no. 1, pp. 31–36, Jan. 2025, doi: 10.1109/TED.2024.3497927.

[4] F. W. Sexton, "Destructive single-event effects in semiconductor devices and ICs," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 603–621, Jun. 2003, doi: 10.1109/TNS.2003.813137.

[5] E. Normand, J. L. Wert, D. L. Oberg, P. R. Majewski, P. Voss, and S. A. Wender, "Neutron-induced single event burnout in high voltage electronics," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 2358–2366, Dec. 1997, doi: 10.1109/23.659062.

[6] F. Zhou, L. Mo, Z. Hu, Q. Yu, C. Zou, W. Xu, F. Ren, D. Zhou, D. Chen, Y. Zheng, R. Zhang, and H. Lu, "1.5-kV AlGaN/GaN MIS-HEMT with 3-D stacking pad-connected Schottky structure demonstrating radiation robustness against atmospheric neutrons," *IEEE Electron Device Lett.*, vol. 45, no. 7, pp. 1129–1132, Jul. 2024, doi: 10.1109/LED.2024.3403682.

[7] J. L. Titus, "An updated perspective of single event gate rupture and single event burnout in power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1912–1928, Jun. 2013, doi: 10.1109/TNS.2013.2252194.

[8] F.-K. Liu, Z.-L. Liu, and X.-J. Li, "Impact of ^{60}Co-γ irradiation pre-treatment on single-event burnout in N-channel power VDMOS transistors," *IEEE Electron Device Lett.*, vol. 45, no. 7, pp. 1105–1108, Jul. 2024, doi: 10.1109/LED.2024.3403570.

[9] K. Galloway, "A brief review of heavy-ion radiation degradation and failure of silicon UMOS power transistors," *Electronics*, vol. 3, no. 4, pp. 582–593, Sep. 2014, doi: 10.3390/electronics3040582.

[10] Y. Wang, Y. Zhang, and C. Yu, "Research of single-event burnout in power UMOSFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 887–892, Feb. 2013, doi: 10.1109/TED.2012.2234126.

[11] Y. Wang, Y. Zhang, L.-G. Wang, and C. Yu, "Single-event burnout hardening of power UMOSFETs with optimized structure," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 2001–2007, Jun. 2013, doi: 10.1109/TED.2013.2256426.

[12] Y. Wang, C.-H. Yu, Z. Dou, and W. Xue, "Single-event burnout hardening of power UMOSFETs with integrated Schottky diode," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1464–1469, May 2014, doi: 10.1109/TED.2014.2312948.

[13] Y. Wang, C.-H. Yu, M.-S. Li, F. Cao, and Y.-J. Liu, "High-performance split-gate-enhanced UMOSFET with dual channels," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1455–1460, Apr. 2017, doi: 10.1109/TED.2017.2665589.

[14] Y. Wang, C.-H. Yu, X.-J. Li, and J.-Q. Yang, "A comparative study on heavy-ion irradiation impact on p-channel and n-channel power UMOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 6, pp. 1249–1256, Jun. 2022, doi: 10.1109/TNS.2022.3175954.

[15] C.-H. Yu, Y. Wang, M.-T. Bao, X.-J. Li, J.-Q. Yang, and F. Cao, "Impact of heavy-ion irradiation in an 80-V radiation-hardened split-gate trench power UMOSFET," *IEEE Trans. Electron Devices*, vol. 69, no. 2, pp. 664–668, Feb. 2022, doi: 10.1109/TED.2021.3135369.

[16] C. Martinella, R. G. Alia, R. Stark, A. Coronetti, C. Cazzaniga, M. Kastriotou, Y. Kadi, R. Gaillard, U. Grossner, and A. Javanainen, "Impact of terrestrial neutrons on the reliability of SiC VD-MOSFET technologies," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 634–641, May 2021, doi: 10.1109/TNS.2021.3065122.

[17] C. Martinella, S. Race, R. Stark, R. G. Alia, A. Javanainen, and U. Grossner, "High-energy proton and atmospheric-neutron irradiations of SiC power MOSFETs: SEB study and impact on channel and drift resistances," *IEEE Trans. Nucl. Sci.*, vol. 70, no. 8, pp. 1844–1851, Aug. 2023, doi: 10.1109/TNS.2023.3267144.

[18] S. G. Alberton, A. C. V. Bôas, M. A. Guazzelli, V. A. P. Aguiar, N. Added, C. A. Federico, T. C. Cavalcante, E. C. F. P. Júnior, R. G. Vaz, O. L. Gonçalez, J. Wyss, A. Paccagnella, and N. H. Medina, "Single-event effects induced by monoenergetic fast neutrons in silicon power UMOSFETs," *TechRxiv*, vol. 2024, pp. 1–9, Dec. 2024, doi: 10.36227/TECHRXIV.173496316.61556618/v1.

[19] S. G. Alberton, A. C. V. Bôas, N. H. Medina, M. A. Guazzelli, V. A. P. Aguiar, N. Added, C. A. Federico, O. L. Gonçalez, T. C. Cavalcante, E. C. F. Pereira Júnior, and R. G. Vaz, "Alpha particle- and neutron-induced single-event effects in COTS power FETS," in *Proc. 22nd Eur. Conf. Radiat. Effects Compon. Syst. (RADECS)*, Oct. 2022, pp. 1–4, doi: 10.1109/RADECS55911.2022.10412582.

[20] S. G. Alberton, A. C. V. Bôas, M. A. Guazzelli, J. Wyss, V. A. P. Aguiar, N. Added, C. A. Federico, T. C. Cavalcante, E. C. F. Pereira Júnior, R. G. Vaz, O. L. Gonçalez, L. Silvestrin, S. Mattiazzo, C. Cazzaniga, M. Kastriotou, C. Frost, A. Paccagnella, and N. Medina, "Studies on the reliability of power UMOSFETs in the terrestrial radiation environment," in *Proc. 24th Eur. Conf. Radiat. Effects Compon. Syst. (RADECS)*, 2024.

[21] C. Cazzaniga, M. Bagatin, S. Gerardin, A. Costantino, and C. D. Frost, "First tests of a new facility for device-level, board-level and system-level neutron irradiation of microelectronics," *IEEE Trans. Emerg. Topics Comput.*, vol. 9, no. 1, pp. 104–108, Jan. 2021, doi: 10.1109/TETC.2018.2879027.

[22] D. Chiesa, M. Nastasi, C. Cazzaniga, M. Rebai, L. Arcidiacono, E. Previtali, G. Gorini, and C. D. Frost, "Measurement of the neutron flux at spallation sources using multi-foil activation," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 902, pp. 14–24, Sep. 2018, doi: 10.1016/j.nima.2018.06.016.

[23] "Measurement and reporting of alpha particle and terrestrial cosmic ray induced soft errors in semiconductor devices," JEDEC Solid State Technol. Assoc., Arlington County, VA, USA, Tech. Rep. JESD89B, 2021. [Online]. Available: https://www.jedec.org/standards-documents/docs/jesd-89a

[24] M. S. Gordon, P. Goldhagen, K. P. Rodbell, T. H. Zabel, H. H. K. Tang, J. M. Clem, and P. Bailey, "Measurement of the flux and energy spectrum of cosmic-ray induced neutrons on the ground," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3427–3434, Dec. 2004, doi: 10.1109/TNS.2004.839134.

[25] D. Lucsányi, R. G. Alía, K. Bilko, M. Cecchetto, S. Fiore, and E. Pirovano, "G4SEE: A geant4-based single event effect simulation toolkit and its validation through monoenergetic neutron measurements," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 3, pp. 273–281, Mar. 2022, doi: 10.1109/TNS.2022.3149989.

[26] A. Michez, S. Dhombres, and J. Boch, "ECORCE: A TCAD tool for total ionizing dose and single event effect modeling," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1516–1527, Aug. 2015, doi: 10.1109/TNS.2015.2449281.

[27] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 2nd ed., Cham, Swizerland: Springer, 2018.

[28] B. J. Baliga, *Advanced Power MOSFET Concepts*. Cham, Swizerland: Springer, 2010.

[29] "Test method standard: Test methods for semiconductor devices," Dept. Agencies, Dept. Defense, Tech. Rep. MIL-STD-750E, 2006. [Online]. Available: https://quicksearch.dla.mil

[30] S. Liu, R. Marec, P. Sherman, J. L. Titus, F. Bezerra, V. Ferlet-Cavois, M. Marin, N. Sukhaseum, F. Widmer, M. Muschitiello, L. Gouyet, R. Ecoffet, and M. Zafrani, "Evaluation on protective single event burnout test method for power DMOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 1125–1129, Aug. 2012, doi: 10.1109/TNS.2011.2177863.

[31] J. C. Lee and N. J. McCormick, *Risk and Safety Analysis of Nuclear Systems*. Hoboken, NJ, USA: Wiley, 2011.

[32] S. G. Alberton, V. A. P. Aguiar, N. H. Medina, N. Added, E. L. A. Macchione, R. Menegasso, G. J. Cesário, H. C. Santos, V. B. Scarduelli, J. A. Alcántara-Núñez, M. A. Guazzelli, R. B. B. Santos, and D. Flechas, "Charge deposition analysis of heavy-ion-induced single-event burnout in low-voltage power VDMOSFET," *Microelectron. Rel.*, vol. 137, Oct. 2022, Art. no. 114784, doi: 10.1016/j.microrel.2022.114784.

[33] K. Sahu, "EEE-INST-002: Instructions for EEE parts selection, screening, qualification, and derating," Goddard Space Flight Center, Greenbelt, MD, USA, Tech. Rep. NASA/TP-2003-212242, 2003. [Online]. Available: https://nepp.nasa.gov/pages/EEE-INST-002.cfm

[34] "Test procedure for the measurement of terrestrial cosmic ray induced destructive effects in power semiconductor devices," JEDEC Solid State Technol. Assoc., Arlington County, VA, USA, Tech. Rep. JEDEC-JEP151A, 2022. [Online]. Available: https://www.jedec.org/standards-documents/docs/jep151

[35] S. Kuboyama, N. Ikeda, T. Hirao, and S. Matsuda, "Improved model for single-event burnout mechanism," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3336–3341, Dec. 2004, doi: 10.1109/TNS.2004.839512.

[36] H. Egawa, "Avalanche characteristics and failure mechanism of high voltage diodes," *IEEE Trans. Electron Devices*, vol. ED-13, no. 11, pp. 754–758, Nov. 1966, doi: 10.1109/T-ED.1966.15838.

[37] T. F. Wrobel, F. N. Coppage, G. L. Hash, and A. J. Smith, "Current induced avalanche in epitaxial structures," *IEEE Trans. Nucl. Sci.*, vol. NS-32, no. 6, pp. 3991–3995, Dec. 1985, doi: 10.1109/TNS.1985.4334056.

[38] R. Tambone, A. Ferrara, R. Siemieniec, A. Wood, F. Magrini, and R. J. E. Hueting, "Ruggedness of silicon power MOSFETs—Part I: Cell structure design related failure: A review," *IEEE Trans. Electron Devices*, vol. 71, no. 6, pp. 3445–3457, Jun. 2024, doi: 10.1109/TED.2024.3394452.

[39] S. Liu, J. L. Titus, and M. Boden, "Effect of buffer layer on single-event burnout of power DMOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2554–2560, Dec. 2007, doi: 10.1109/TNS.2007.910869.

[40] S. Liu, M. Boden, D. A. Girdhar, and J. L. Titus, "Single-event burnout and avalanche characteristics of power DMOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3379–3385, Dec. 2006, doi: 10.1109/TNS.2006.884971.

[41] V. Ferlet-Cavrois, F. Sturesson, A. Zadeh, G. Santin, P. Truscott, C. Poivey, J. R. Schwank, D. Peyre, C. Binois, T. Beutier, A. Luu, M. Poizat, G. Chaumont, R. Harboe-Sørensen, F. Bezerra, and R. Ecoffet, "Charge collection in power MOSFETs for SEB characterisation—Evidence of energy effects," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3515–3527, Dec. 2010, doi: 10.1109/TNS.2010.2086077.

[42] T. Grasser, *Hot Carrier Degradation in Semiconductor Devices*. Cham, Swizerland: Springer, 2014.

[43] S. M. Sze, Y. Li, and K. K. Ng, *Physics of Semiconductor Devices*, 4th ed., Hoboken, NJ, USA: Wiley, 2021.

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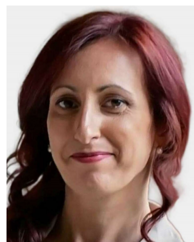

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