

# Short-Circuit operation of a 650-V/60-A GaN-based Half-Bridge

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**Abstract.** The Short-Circuit (SC) robustness of GaN HEMTs represents a relevant issue for their use in power electronics. The research only focused on type I SC behavior of the single GaN transistor, in addition using large gate resistors during experimental tests. Here, we investigate the real case of a GaN-based Half-Bridge operating in SC conditions, focusing on the impact that another identical device can have on the SC. After designing and realizing a prototype test board with two 650-V/60-A GaN HEMTs, experimental SC tests confirm the theoretical analysis and highlight the effects of the DC-link voltage, demonstrating that both the presence of a second device and the use of large gate resistor can strongly alter the expected SC behavior.

**Keywords:** GaN HEMT, Short-Circuit, Half-bridge, Reliability.

## 1 Introduction

Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) can lead to high-frequency operation of power converters, ensuring at the same time high power density and efficiency [1]. However, considering the 650-V voltage rating, GaN HEMTs still present some limitations, such as the low Short-Circuit (SC) ruggedness [2].

In recent years, many studies and findings were conducted on the SC behavior of GaN devices: from the capability, degradation and withstand time tests [2]-[5], to instability [6], [7], failure mechanisms analysis [8], measurement techniques [9] and modelling aspects [10].

The SC characterizations presented in the literature are often carried out focusing on the single device, performing a SC directly on the DC-link capacitors or with another protection device with much higher current rating. However, these test conditions do not reflect the real case in practical applications, where the problem of the SC event can occur in converters based on Half Bridge (HB) configuration. Even the presence of the protection device placed in series to the GaN HEMT under test is far from the real SC event, because it always works in its linear region and never undergoes an electro-thermal stress [10], [11]. On the contrary, in the practical case the power devices of the bridge are equal and therefore the SC involves two identical devices, whose behavior should be analyzed. Moreover, very large values of turn-on gate resistance are often used to perform the SC tests, both to slow down the switching transients and to prevent

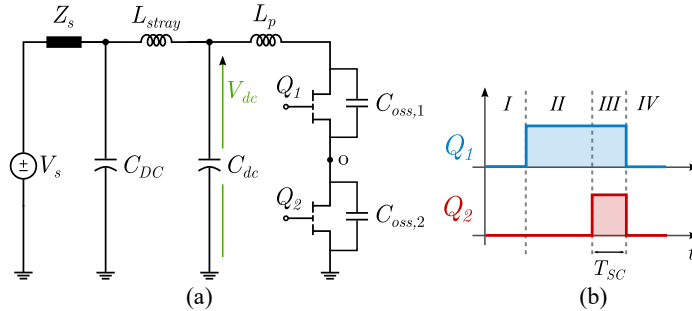
instabilities. In fact, in [4] the authors use a  $38 \Omega$  gate resistor, while a  $50 \Omega$  resistor is used in [5]. In [3] 46-, 100-, 460- $\Omega$  values are used. In [2] the value is not provided, but it can be obtained from the experimental data of the gate current and voltage and it is about  $60 \Omega$ .

In this work, we study the SC operation of a HB with 650-V/60-A p-doped gate GaN HEMTs [12]. After a theoretical analysis, illustrated in section 2, we performed experimental SC tests using a designed prototype in section 3, evaluating the impact of DC-link voltage ( $V_{dc}$ ), gate resistor ( $R_g$ ) and the mismatch in the circuit loops of the two devices. Finally, section 4 provides the conclusions of the work.

## 2 Theoretical operation

The circuit scheme of Fig. 1(a) can be considered to study the SC operation of a HB, where  $V_s$  represents a real DC voltage source with its impedance  $Z_s$ ,  $C_{DC}$  is the main DC-link capacitance,  $C_{dc}$  is the decoupling capacitance,  $L_{stray}$  represents the stray inductance between the main DC-link and  $C_{dc}$  and  $Q_1, Q_2$  are two identical GaN HEMTs. In first approximation, all the power loop parasitic inductance is lumped in  $L_p$ .

To create the SC on the HB, the gates of  $Q_1$  and  $Q_2$  are driven by the logic signals shown in Fig. 1(b).

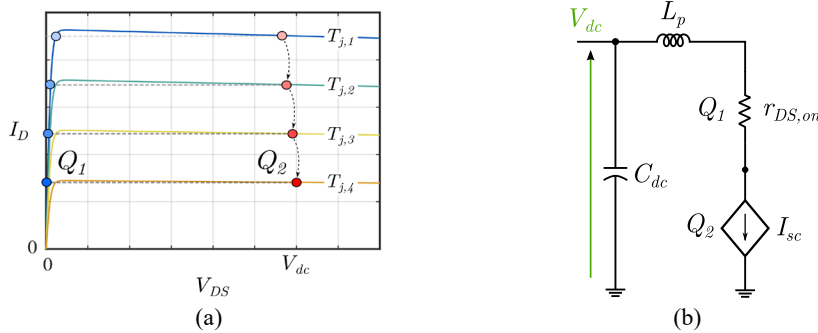


**Fig. 1** Basic circuit scheme of HB with GaN HEMTs (a) and driving signals (b) for the study of the SC behavior.

In phase II  $Q_1$  is turned on and all  $V_{dc}$  is applied at the drain of  $Q_2$ . In phase III  $Q_2$  is also turned on while  $Q_1$  is already on and the HB operates in SC conditions for the time duration  $T_{SC}$ . This situation, in which  $Q_2$  suffers from a type I SC and  $Q_1$  from a type II one, is certainly of applicative interest. In fact, it often occurs during debugging of a converter when it is possible that the control circuit commands by mistake the turning on of the two switches at the same time or when one of the two switches should be off and turns on due to noise on its gate while the other is on.

The SC current  $I_{SC}$  is determined by the operating point on the output characteristic of device  $Q_2$ , visible in Fig. 2(a) for increasing junction temperatures ( $T_j$ ).  $Q_2$  works in the saturation region and behaves like a controlled current source while it is still blocking almost all  $V_{dc}$ , suffering from a high instantaneous power dissipation that causes the increase of  $T_j$ . Instead, the operating point of  $Q_1$ , assuming that its  $T_j$  is always lower

than the one of  $Q_2$ , is located in the linear region of its output characteristic, and therefore it behaves like a current-controlled resistance defined by its  $R_{DS,on}$ , as graphically shown in Fig. 2(a). Hence, during the SC event the behavior of the two HEMTs is not the same and the electro-thermal stresses are also different. In the described condition,  $Q_2$  can be considered the device which leads the SC current, as it works in the saturation region, and  $Q_1$  “follows” the current by varying its voltage drop acting as a variable resistor. Consequently, the equivalent scheme of the HB during the SC event is the one shown in Fig. 2(b), with a controlled current source and the on-resistance of the other device. In general, all the SC stress is borne by the device which turns on after its block-



**Fig. 2.** Operating points of  $Q_1$  and  $Q_2$  on the drain I–V plane (a) and equivalent scheme of the Half-Bridge (b) during SC.

ing phase: in fact, the same reasoning could be conducted swapping the driving signals of the two devices, turning on  $Q_2$  first and  $Q_1$  afterwards. In this case, the roles of the switches would be inverted, with  $Q_1$  operating in the saturation region and bearing all the SC stress.

## 2.1 Simulation Analysis

The effect of various circuit parameters, including  $V_{dc}$ , the gate driver voltage and the SC pulse width  $T_{SC}$ , has been already investigated in many works [2], [4], [5]. No unexpected behaviors can be observed when evaluating the SC operation of the HB instead of the single device. The peak SC current is directly dependent on the gate voltage, while it undergoes a higher reduction as  $V_{dc}$  increases, while a larger  $T_{SC}$  is related to a higher dissipated SC energy, that can bring the device to the failure [2].

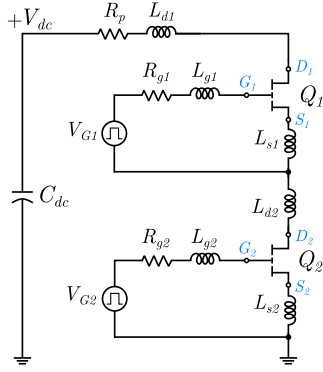
However, when a mismatch in the common-source inductance ( $L_s$ ) of the devices is present in the circuit, the behavior of the two GaN HEMTs can be swapped and  $Q_1$  can work in saturation region, even if it is turned on before  $Q_2$  and should work in linear region. As a demonstration, a LTSpice simulation was conducted considering the circuit in Fig. 3, that includes the main parasitic elements in the gate and power loops of the HB. The parameters used for the simulation are listed in Table 1, while  $V_{dc}$  was varied from 100 V to 400 V. The LTSpice model supplied by the manufacture was used for the GS66516T GaN HEMT [12]. With  $L_{s1}$  on the gate loop of  $Q_1$  20% higher than  $L_{s2}$ , the behavior of the two HEMTs can be swapped, as visible from the SC loci of Fig. 4, derived from the simulated drain current and voltage of the two transistors. When  $V_{DS,1}$ , that starts from 0 V, becomes higher than  $V_{DS,2}$ , that starts from  $V_{dc}$ , the behaviors of

**Table 1.** Parameters used in LTSpice simulation.

Symbol	Value	Unit	Symbol	Value	Unit
$Q_1, Q_2$	GS66516T	-	$L_{g1}, L_{g2}$	1.0	nH
$C_{dc}$	80	$\mu\text{F}$	$L_{d1}, L_{d2}$	3.0	nH
$T_{SC}$	5	$\mu\text{s}$	$L_{s1}$	0.5	nH
$V_{G1}, V_{G2}$	5	V	$L_{s2}$	0.6	nH
$R_{g1}, R_{g2}$	10	$\Omega$	$R_p$	10	m $\Omega$

the two GaN HEMTs are swapped and  $V_{DS,1}$  tends to  $V_{dc}$  while  $V_{DS,2}$  goes to its on-state voltage. This happens when  $V_{dc}$  is lower than 300 V in the simulated test conditions. In this case, the power dissipation of  $Q_1$  is higher than in  $Q_2$ , since it is subjected to high  $V_{DS}$ . When  $V_{dc}$  is higher than 300 V  $V_{DS,1}$  and  $V_{DS,2}$ , even showing a transient increase and decrease respectively, do not overlap anymore and  $V_{DS,1}$  tends to its on-state voltage drop, while  $V_{DS,2}$  tends to  $V_{dc}$ .

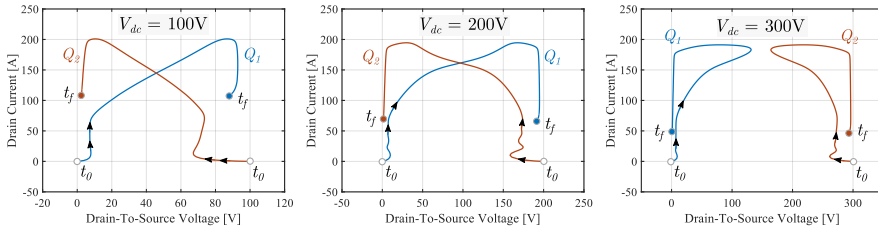
Hence, for  $V_{dc} < 300$  V,  $Q_1$  works in saturation and  $Q_2$  in the linear region, even if  $Q_2$  turns on after its blocking phase. This can be explained considering the output characteristics and the drain voltage and temperature waveforms. After the transient turn-on phase of device  $Q_2$ , the steady-state equilibrium point is determined by the intersection of the output characteristics of the transistors. The difference in the stray inductances on the source path is responsible for the transient variation of  $V_{DS,2}$ , that becomes lower than  $V_{DS,1}$  for  $V_{dc} < 300$  V, as highlighted in Fig. 5(a).

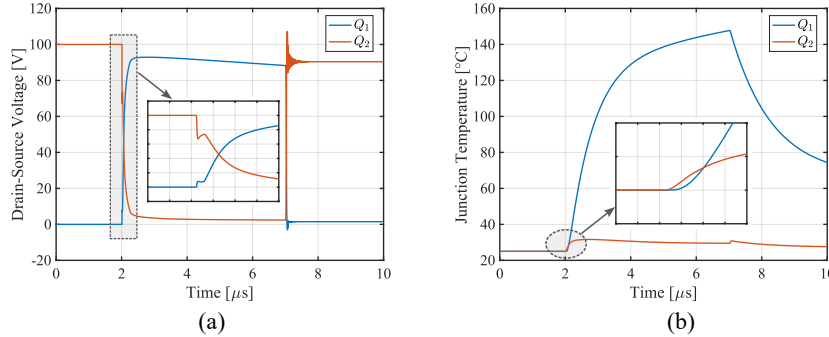
**Fig. 3.** Circuit simulated in LTSpice.

These facts lead  $Q_1$  to dissipate more power than  $Q_2$ , increasing its junction temperature  $T_{j,1}$ , that becomes higher than  $T_{j,2}$  of  $Q_2$ , as shown in Fig. 5(b). Since  $T_{j,1} > T_{j,2}$ , the output characteristic of  $Q_1$  intersects the one of  $Q_2$  in the linear region of this latter one, leading  $Q_1$  to operate in the saturation region and  $Q_2$  to work in the linear region at the steady state. For  $V_{dc}$  higher than 300 V, whose waveforms are not reported here for brevity, the opposite situation is established, as  $Q_1$  shows a lower drain voltage at the beginning of the SC and, even if it goes in the saturation region during the transient,  $V_{DS,2}$  of  $Q_2$  is always

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**Fig. 4.** SC loci of the two GaN HEMTs in the presence of mismatch in common-source inductance, with  $L_{s1} > L_{s2}$ .



**Fig. 5.** Simulated waveforms at  $V_{dc} = 100$  V:  $V_{DS}$  (a) and  $T_j$  (b) of the two GaN HEMTs.

higher, leading to a higher power dissipation and temperature increase. So, in the steady state it works in the saturation region, while  $Q_1$  works in the linear region.

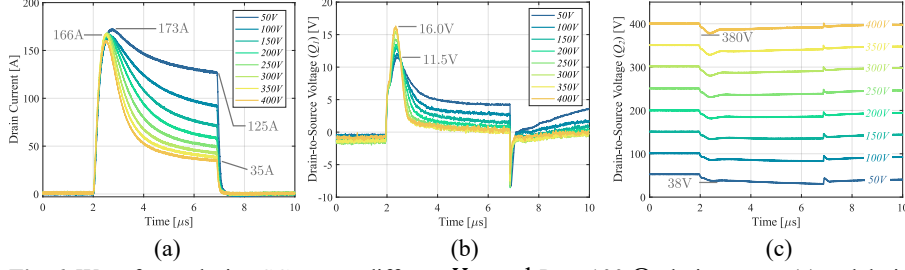
### 3 Experimental Short-Circuit tests

The experimental SC tests were conducted on a designed prototype at different  $V_{dc}$ , from 50 V to 400 V, using two values for  $R_g$ , namely 100  $\Omega$  and 22  $\Omega$ . These values for  $R_g$  were selected to show the possible impact that the proper choice of  $R_g$  can have in practical applications. In fact, as stated before, in most of experimental SC characterizations presented in the literature large gate resistors are used (cf. 1). This condition has no impact on the type I SC of the single device, but it may affect the SC behavior of the HB, and for this reason two very different values of gate resistance are used here. In fact, the 22  $\Omega$  resistor is practically used when working with GaN HEMTs in normal operations at high frequency, at the opposite of the 100  $\Omega$  resistor which is never used in a real converter.

The SC pulse-width was set to 5  $\mu$ s and the gate drivers voltage levels are +5 V and 0 V for *on* and *off* states, respectively. This choice ensures the full turn-off of the device, that has a typical threshold voltage of 1.6 V.

The SC waveform with  $R_g = 100$   $\Omega$  are depicted in Fig. 6, showing the drain current  $I_D$  (corresponding to  $I_{SC}$ , equal for the two devices) and  $V_{DS}$  of both GaN HEMTs. It must be clarified that the drain-source voltage of  $Q_1$  ( $V_{DS1}$ ) was not directly measured during the tests, but it was obtained from the voltage balance in the output loop, referring to Fig. 1, as  $V_{dc} - V_{DS2} - L_p dI_D/dt$ . The contribution of  $L_p$  was numerically included during the computation of  $V_{DS1}$  and although this fact causes some numerical errors when evaluating  $V_{DS1}$ , especially at the turn-on and turn-off transients, the waveforms of  $V_{DS1}$  during the SC event are reliable and can be used to evaluate the SC behavior of the device.

The drain current waveforms show the typical behavior during the SC, reaching a peak value in about 900 ns and then decreasing to lower values because of the increase of  $T_j$ . In particular,  $I_D$  reaches a peak of 173 A and then decreases to about 125 A at  $V_{dc} = 50$  V (see Fig. 6(a)). As  $V_{dc}$  increases, the peak of the SC current slightly decreases to about 166 A, while its final value undergoes a huge drop, that becomes larger



**Fig. 6.** Waveforms during SC tests at different  $V_{dc}$  and  $R_g = 100 \Omega$ : drain current (a) and drain voltage of  $Q_1$  (b) and  $Q_2$  (c).

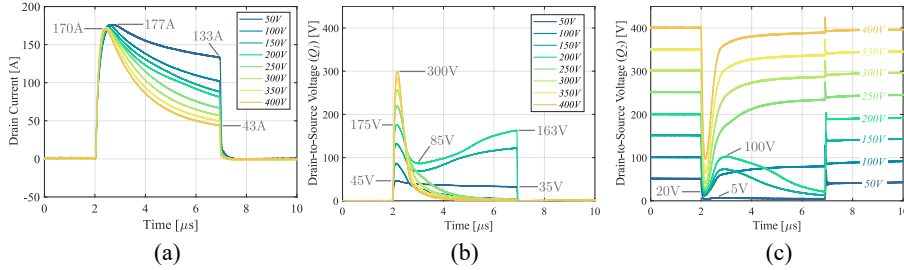
with increasing  $V_{dc}$ . At  $V_{dc} = 400 \text{ V}$  the peak SC current is about 160 A and it is reduced by 70% after 2  $\mu\text{s}$ , becoming equal to about 50 A. At the end of the SC, the final value is 35 A, indicating that the current decreased by 80% with respect the initial value (see Fig. 6(a)).

The drain voltage waveforms are indicative of the roles played by the two devices during the SC event. Almost all  $V_{dc}$  is applied to  $Q_2$ , that works in the saturation region for all the SC duration. On the contrary,  $Q_1$  starts from 0 V and in 1  $\mu\text{s}$  reaches a peak value, that increases with  $V_{dc}$  but remains between 11.5 V and 16.0 V. After that, its value decreases to less than 5 V and at  $V_{dc} = 400 \text{ V}$  it goes to about 0.3 V (see Fig. 6(b)). In correspondence of the peak value of  $V_{DS1}$ ,  $V_{DS2}$  experiences the largest voltage drop, reaching 380 V and 38 V in the extreme cases of  $V_{dc} = 400 \text{ V}$  and  $V_{dc} = 50 \text{ V}$ , respectively (see Fig. 6(c)). Therefore, the behavior of the two devices complies with the theoretical analysis introduced in section 2. In fact,  $Q_2$  works in the saturation region and  $Q_1$ , after a transient working point in the saturation region operates in its linear region.

The common-source inductance measured on the real prototype is 0.8 nH for  $Q_1$  and 0.4 nH for  $Q_2$ . However, even if a mismatch in the common-source inductance in the two gate loops is present, no effect is visible in the waveforms, meaning that the large  $R_g$  helps in reducing the effect of  $L_s$  on the two devices.

The waveforms with  $R_g = 22 \Omega$ , derived from experimental SC tests conducted on new devices, are shown in Fig. 7. The drain current reaches a peak value of about 177 A at  $V_{dc} = 50 \text{ V}$  and then it slightly decreases, with the increase of  $V_{dc}$ , down to 170 A at 400 V. Instead, the  $I_D$  value at the end of the SC reaches 133 A at  $V_{dc} = 50 \text{ V}$  and 43 A at  $V_{dc} = 400 \text{ V}$ , that represent a drop of the 25% and 75% with respect the peak value, respectively (see Fig. 7(a)). These final values of  $I_D$  are quite higher than the final values in the previous case.

In this condition the behaviors of  $Q_1$  and  $Q_2$  are swapped for  $V_{dc} < 250 \text{ V}$ , as visible from the  $V_{DS}$  waveforms of Fig. 7(b) and Fig. 7(c). In fact, except for  $V_{dc} = 100 \text{ V}$ ,  $Q_1$  blocks a higher voltage than  $Q_2$ , even if, from a theoretical point of view,  $Q_2$  should block a higher percentage of  $V_{dc}$ . At  $V_{dc} = 50 \text{ V}$   $V_{DS1}$  reaches 45 V and then decreases to 35 V, because  $V_{dc}$  also decreases (see Fig. 7(b)), while  $V_{DS2}$  remains at about 4.5 V (see Fig. 7(c)). This means that the roles of the two devices are swapped and  $Q_1$  operates in the saturation region, while  $Q_2$  is in its linear region. The behavior is inverted at  $V_{dc} = 100 \text{ V}$ , where  $Q_2$  blocks almost all  $V_{dc}$ . However, at 150 V and 200 V, both  $Q_1$  and  $Q_2$  operate at high  $V_{DS}$  for a long period of the SC event. In fact, at  $V_{dc} = 200 \text{ V}$ ,



**Fig. 7.** Waveforms during SC tests at different  $V_{dc}$  and  $R_g = 22 \Omega$ : drain current (a) and drain voltage of  $Q_1$  (b) and  $Q_2$  (c).

$V_{DS1}$  shows a peak of 175 V, then it has a drop to 85 V and then increases again up to 163 V.  $V_{DS2}$  shows the opposite behavior, with a drop from 200 V to 20 V at the beginning of the SC, a consequent increase up to 100 V and, then, a further reduction to 20 V at the end of the SC. For  $V_{dc}$  higher than 200 V, the two devices return to operate as expected, with  $Q_2$  blocking almost all  $V_{dc}$  for a large part of the SC pulse-width. However, it is worth noting a strong voltage dip in  $V_{DS2}$  at the beginning of the SC, caused by the high  $di/dt$ , that is responsible also for the transient increase of  $V_{DS1}$ .

To provide an overall indication about the SC, the energy ( $E_{SC}$ ) dissipated by both devices was computed between the start and final time instants of the SC, indicated with  $t_i$  and  $t_f$ , respectively, starting from the experimental drain current and voltage, according to (1):

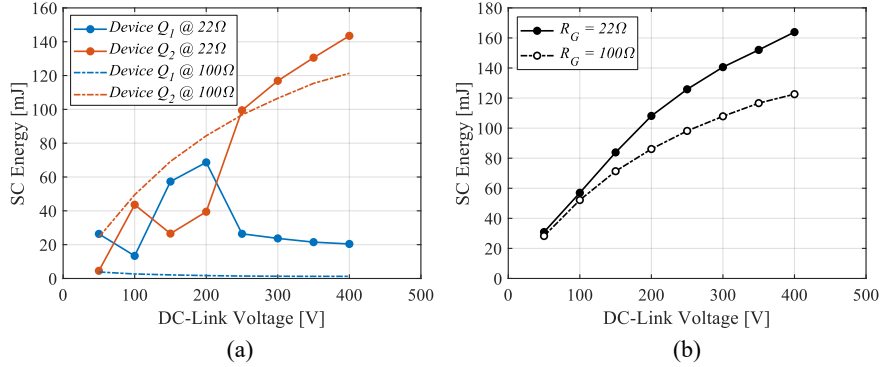
$$E_{SC} = \int_{t_i}^{t_f} I_D(t) V_{DS}(t) dt \quad (1)$$

The SC energy for the two GaN HEMTs is plotted in Fig. 8(a) as a function of  $V_{dc}$  for both cases  $R_g = 100 \Omega$  and  $R_g = 22 \Omega$ . As expected and clearly visible, the SC energy of  $Q_2$  is much higher than  $Q_1$  for  $R_g = 100 \Omega$  and for  $R_g = 22 \Omega$  for all  $V_{dc}$  values higher than 250 V. The non-monotonic trend in the SC energy for  $R_g = 22 \Omega$  and  $V_{dc} < 250$  V, observed in the figure, is due to the different behavior of the two devices when  $V_{dc}$  is lower than 250 V, as previously described.

A global comparison between the total SC energy, computed as the sum of  $Q_1$  and  $Q_2$  energies, for the two values of  $R_g$  is shown in Fig. 8(b), where it can be noted that the total SC energy is higher for  $R_g = 22 \Omega$  in all  $V_{dc}$  conditions, and the difference between the total energies becomes larger as  $V_{dc}$  increases. This fact can be explained considering that the  $I_D$  values in the case  $R_g = 22 \Omega$  were higher than the ones with  $R_g = 100 \Omega$ , leading to a higher mean power dissipation during the SC event.

## 4 Conclusion

The Short-Circuit analysis of GaN HEMTs should be performed in real operating conditions to obtain reliable and meaningful results. In this work the SC is performed on a Half-Bridge with 650-V/60-A GaN HEMTs, evaluating the impact that another device can have on the SC behavior of the transistor. The theoretical analysis showed that under ideal conditions the device that turns on after the blocking phase undergoes



**Fig. 8.** SC energy of device  $Q_1$  and  $Q_2$  (a) and total SC energy (b) versus  $V_{dc}$  in comparison between  $R_g = 22 \Omega$  and  $R_g = 100 \Omega$ , in the condition  $V_G = 5$  V.

a type I SC, while the other one undergoes a type II SC. However, a mismatch in the common-source inductance in the loops of the two devices can swap the behavior of the two transistors, as highlighted by the simulations. The experimental results confirm the theoretical analysis and show the impact of the gate resistor in characterizing the SC robustness of GaN HEMTs. In fact, the use of large gate resistor, besides having low practical usefulness, leads to an underestimation of the SC energy and its electro-thermal stress, even if it eliminates the possible parasitic effects due to the common-source inductance. Therefore, an accurate SC analysis must be performed on a realistic configuration, as a HB, and with practical operating conditions to obtain consistent and reliable results.

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